Next generation microelectronics require increased performance and integration, advanced chip technology and miniaturization. Samtec’s extensive microelectronics and high-speed interconnect expertise, along with our proven methods for package integration, miniaturization, wafer level processing and signal integrity optimization, enable us to provide a unique level of support for advanced microelectronics applications.

www.samtec.com/microelectronics
# TABLE OF CONTENTS

## ADVANCED PACKAGE DESIGN 4-7
- Development, Prototyping, Production
- IC Packaging & Assembly Capabilities
- Enabling Technologies / Roadmap
- IC Packaging & Assembly Design Guidelines

## GLASS CORE TECHNOLOGY 8-11
- Through-Glass Via (TGV) Metalization
- Redistribution Layer (RDL) Circuit Formation
- High Performance Glass-Based Electronics
- Glass Core Technology Design Guidelines

## MICROELECTRONICS SYSTEM SUPPORT 12-13
- Support for Full Channel Challenges
- Package & PCB Design
- Modeling & Simulation
- Analysis, Testing & Validation

## TECHNOLOGY CENTERS 14-15
- Samtec Microelectronics Group
- Samtec Teraspeed Consulting
- Signal Integrity Group
- Samtec Optical Group
- Advanced Interconnect Design
- High-Speed Cable Plant
ADVANCED PACKAGE DESIGN

COMPLETE DESIGN & SUPPORT FOR ADVANCED PACKAGING APPLICATIONS

Development
Complete support is available from the early stages of the design process, including:
- Advanced IC Package Design
- Material Selection & Procurement
- Assembly Processing / Compatibility
- Package Reliability / Testing

Prototyping
To help get your design to market faster, we offer quick-turn prototyping, along with:
- Initial Concept Builds
- Reasonable NREs
- Industry-Leading Lead-Times
- Minimized Iterations Save Time-to-Market

Production
Full production capabilities support a variety of order volumes and cost-levels:
- High Yield Automation / Production
- Repeatability / Process Control
- Transfer Molding Capabilities
- Asian Subcontractors Provide Flexibility
CORE PACKAGING CAPABILITIES

PRECISION DIE PLACEMENT
High-speed, high accuracy die placement (to +/- 3 microns)

WIRE BONDING
Ultra-fine pitch, ultra-low profile ball bond, wedge bond or ribbon bond

FINE PITCH FLIP CHIP & JET UNDERFILL
Ultra-high bump count; tight keep-out regions between die

ENCAPSULATION
Encapsulating with dam and fill, glob top or transfer molding

ADVANCED PACKAGING & ASSEMBLY
Advanced substrates, inspection & metrology
Glass substrate manufacturing, fan out technology
2.5D / 3D TxV technology
Wafer Dicing - 2" to 8" capabilities; thicknesses down to 25 μm
Solder Ball Attach for tight pitches down to 0.4 mm
Lid Attach - AuSn solder, glass frit, hermetic, fluidic, optical, custom materials

SEE PAGES 6-7 FOR TYPICAL DESIGN GUIDELINES.

COMPLEX WIRE BOND  FLIP CHIP & UNDERFILL  PRECISION DIE ATTACH  FINISHING CAPABILITIES

KEY ENABLING TECHNOLOGIES | ROADMAP

Samtec is invested in the development of innovative products and technologies to meet the density and performance demands of next generation microelectronics. Some of our current technologies in development include:

- Thermocompression Bonding
- Gold Stud Bumping
- Anodic Bonding (Wafer-to-Wafer)
- Transfer Molding (conventional and optically clear mold compounds)
- Silicon Photonics and Optics with Ultra-Tight Tolerances

Contact the specialists at Samtec Microelectronics to discuss solutions for your IC Packaging application.
### Precision Die Attach

- Minimum distance between surrounding square of fiducial and neighboring objects must be 0.048 mm
- Gray level contrast between background and fiducial must be a minimum of 100 gray levels out of 256
- Background of fiducial must not have a structure and background must be single-colored gray level
- Max. die size for dipping: 50 mm x 50 mm
- No waffle-pack handling for die < 1 mm²
- Maximum length to width ratio for components: 5:1
- Saw kerfs must be at least 25 μm and into the dicing tape (through the entire wafer thickness)
- Die attach materials can be non-conductive or conductive pastes, die attach films (DAF) and solder preforms; other processes can be discussed per customer requirements

### Typical Wire Bond Specifications

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>ORGANIC (min)</th>
<th>CERAMIC (min)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A Wire Bond Pad</td>
<td>0.004* (100 μm)</td>
<td>0.003* (75 μm)</td>
</tr>
<tr>
<td>B Wire Bond Pad Pitch</td>
<td>0.008* (200 μm)</td>
<td>0.006* (150 μm)</td>
</tr>
<tr>
<td>C Overlap of Wire Bond Lead Edge to Via</td>
<td>0.008* (200 μm)</td>
<td>0.007* (175 μm)</td>
</tr>
<tr>
<td>D Space Solder Mask to Wire Bond Lead Edge</td>
<td>0.004* (100 μm)</td>
<td>-</td>
</tr>
<tr>
<td>E Overlap of Wire Bond Lead Edge to Solder Mask</td>
<td>0.008* (200 μm)</td>
<td>-</td>
</tr>
<tr>
<td>F Space of Die Edge to Wire Bond Lead Edge (assumes no ground plane for die attach)</td>
<td>0.015* (375 μm) or 2x Die Thickness (whichever is greater)</td>
<td>-</td>
</tr>
<tr>
<td>G Maximum Wire Length</td>
<td>0.250* (6350 μm)</td>
<td></td>
</tr>
<tr>
<td>H Maximum Wire Height</td>
<td>0.100* (2540 μm)</td>
<td></td>
</tr>
</tbody>
</table>

### Low Profile & Fine Pitch Wire Bond

Plating and layout requirements for substrate pad design as well as wire parameters:

- Wedge Bond - ENIG plating is acceptable; typical wire types include Al, Au and Pt
- Ball Bond - ENEPIG plating is recommended; typical wire types include Au & Cu

Processes that use Au ball bond, require Gold plate per MIL-G-45204, Type III, Grade A, Class 1:

- 99.9% purity minimum
- < 90 Knoop hardness
- 50 μ" thick, minimum
NOTE

These dimensions are guidelines designed to help release product to manufacturing as quickly as possible. Full capabilities are not limited to the specifications included in this document. Please contact SME@samtec.com for applications with tighter requirements.

FLIP CHIP & UNDERFILL

Package Size (approximate):
- Min: 10 mm x 10 mm
- Max: 63 mm x 63 mm

Flux:
- No-clean fluxes
- Water-soluble fluxes
- RMA-based fluxes

Substrate BGA Solder Ball:
- Min Size: 0.018” dia (approx.)
- Max Size: 0.025” dia (approx.)
- Material: Eutectic Pb:Sn (37:63) or Pb-Free

Substrate BGA Pad:
- Shortest BGA Ball Pitch: 0.80 mm x 0.80 mm
- Furthest Pitch: No constraint
- Pad Layout: Any configuration is acceptable

ENCAPSULATION

- Maximum encapsulation thickness (board surface to top of encapsulation): 0.024” (600)
- Automated dispense tool heated work area: 12” x 16”
- Total work area: 20” x 30”
- Machine positioning accuracy and repeatability: +/- 0.001”

TYPICAL PACKAGE DESIGN RULES

<table>
<thead>
<tr>
<th>ITEM</th>
<th>DESCRIPTION</th>
<th>ORGANIC (min) INCHES (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Dam Width</td>
<td>0.012” (300)</td>
</tr>
<tr>
<td>B</td>
<td>Space of Dam to Wire Bond Lead Edge</td>
<td>0.012” (300)</td>
</tr>
<tr>
<td>C</td>
<td>Space of Fiducial to Dam*</td>
<td>0.007” (175)</td>
</tr>
<tr>
<td>D</td>
<td>Overlap of Encapsulation to Top of Wire Bond Loop</td>
<td>0.007” (175)</td>
</tr>
<tr>
<td>E</td>
<td>Height of Encapsulation**</td>
<td>= A / 2</td>
</tr>
</tbody>
</table>

*Must be outside encapsulated region
**Board surface to top of encapsulation
GLASS CORE TECHNOLOGY

ULTRA-MINIATURIZED | HIGHLY INTEGRATED | HIGH PERFORMANCE

Through-Glass Vias (TGVs) in Glass Substrates
The industry’s only proven process for metalization and hermetic sealing of ultra-high-density Through-Glass Vias (TGVs) enables:
- Extreme Miniaturization & Integration
- High Performance Electronics
- High Reliability Packaging Solutions

Redistribution Layer (RDL) Circuit Patterning on Glass
RDL’s unique thin-film process enables circuit formation on glass substrates, providing for:
- Low Loss Fan-Out of Chip and Package Interconnects
- Lower Cost Compared to Traditional Silicon-Based Interposers

Channels and Shaped Vias in Glass Substrates
Glass is ideal for applications requiring shaped vias and channels, including:
- Microfluidic & Fluidic Devices
- 3D Structures
- Integrated Passive Devices, Filters
- Endless IoT Applications
HIGH PERFORMANCE ELECTRONICS

<table>
<thead>
<tr>
<th>DESIRED PROPERTIES</th>
<th>GLASS</th>
<th>SILICON</th>
<th>ORGANIC LAMINATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Thickness Variation (TTV)</td>
<td>&lt; 5 µm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Warp</td>
<td>&lt; 2 µm / 20 mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Insulation Resistance</td>
<td>High</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Optical Transparency</td>
<td>Optical I/O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Surface Roughness</td>
<td>&lt; 5 nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Coefficient of Thermal Expansion (CTE)</td>
<td>3.2 ppm / °C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hermetic Vias</td>
<td>Mil-Spec.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Glass substrates offer high structural integrity, resistance to vibration and temperature, environmental ruggedness, and low electrical loss, making them ideal for next generation microelectronics demands.

Samtec’s proprietary Glass Core Technology process leverages the performance benefits of glass to enable performance optimized, ultra-miniaturized substrates for next generation designs.

SEE PAGES 10-11 FOR TYPICAL DESIGN GUIDELINES.

GLASS CORE TECHNOLOGY PRACTICAL APPLICATIONS

- **Automotive MEMS and Sensors**
- **Smart Building Sensor Modules**
- **RF Components and Modules**
  - Advanced RF SiP
  - Automotive RF
- **CMOS Image Sensor (CIS)**
  - Automotive Camera Modules
  - Active Imaging & LiDAR
- **Microfluidics & Lab-on-Chip**
  - Solid State Medical Imaging
  - Medical Robotics Sensors

GLASS CORE TECHNOLOGY | ROADMAP

With a wide market reach and broad range of flow speeds, fused silica-based substrates are an ideal solution for microfluidic devices, a growing market sector within the biomedical industry. Applications include:

- Fluidic structures for electronics cooling designs
- Microfluidic structures for biomedical devices and lab-on-chip application designs

Microstructuring possibilities also include formation of microchannels, cavities, larger cooling channels, mixing channels, 180-degree bends, as well as ferrule openings for optical fibers and v-grooves, among others.

Contact the specialists at Samtec Microelectronics to discuss solutions for your next generation system design.
THROUGH-GLASS VIA (TGV) ENABLED GLASS INTERPOSERS

Samtec’s Through-Glass Vias (TGVs) enable Glass Core Technology (i.e., glass interposers, smart glass substrates and microstructured glass substrates). TGV-enabled glass substrates permit the integration of glass and metal into a single wafer, while interposers promote more efficient package interconnects and manufacturing cycle times.

The hermetically sealed TGVs are manufactured from both high quality borosilicate glass, fused silica (aka quartz), and sapphire. Through the use of high quality glass wafer material, combined with advanced interconnect technologies (e.g., Redistribution Layer), Samtec’s Glass Core Technology enables a one-of-a-kind packaging product.

**THROUGH-GLASS VIA CROSS-SECTION VIEW**

**GLASS CHARACTERISTICS & APPLICATIONS**

**BOROSILICATE GLASS**
- Excellent clarity & rigidity
- High thermal shock resistance
- CTE matched to Silicon
- Applications include:
  - Biomedical
  - 2.5D / 3D Packaging
  - Displays
  - Optoelectronics

**FUSED SILICA**
- High purity material
- Low dielectric constant & loss factor
- Very low thermal expansion
- Wide operating temp range
- Applications include:
  - Biomedical
  - Microfluidics & Lab-on-a-Chip
  - RF MEMS
  - Optics, Imaging & Photonics

**BOROSILICATE GLASS & FUSED SILICA**

<table>
<thead>
<tr>
<th>DETAIL</th>
<th>UNITS (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A Nominal Glass Thickness*</td>
<td>200 300 400</td>
</tr>
<tr>
<td>B Top Via Diameter</td>
<td>40 to 65 ±5 45 to 70 ±5</td>
</tr>
<tr>
<td>C Bottom Via Diameter</td>
<td>&lt; 0.4 Maximum</td>
</tr>
<tr>
<td>Total Thickness Variation (TTV)</td>
<td>15 20</td>
</tr>
</tbody>
</table>

**STRUCTURE FUSED SILICA (ISLE)**

<table>
<thead>
<tr>
<th>DETAIL</th>
<th>UNITS (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal Glass Thickness*</td>
<td>200 to 500</td>
</tr>
<tr>
<td>Top Via Diameter</td>
<td>25 to 70 ±5</td>
</tr>
<tr>
<td>Bottom Via Diameter</td>
<td>2 x B</td>
</tr>
<tr>
<td>Via Pitch</td>
<td></td>
</tr>
<tr>
<td>Total Thickness Variation (TTV)</td>
<td>20</td>
</tr>
<tr>
<td>Via Positional Accuracy</td>
<td>±25</td>
</tr>
<tr>
<td>Slot Depth</td>
<td>25 ±5 Minimum</td>
</tr>
</tbody>
</table>

*Custom nominal thicknesses also available.*
RDL provides a unique thin-film approach for interfacing to TGVs. The technique enables circuit formation on various glass substrates.

### REDISTRIBUTION LAYER (RDL) TECHNOLOGY

These dimensions are guidelines designed to help release product to manufacturing as quickly as possible. Full capabilities are not limited to the specifications included in this document. Please contact SME@samtec.com for applications with tighter requirements.

### GLASS CORE TECHNOLOGY CAPABILITIES

<table>
<thead>
<tr>
<th>SPECIFICATIONS</th>
<th>CURRENT</th>
<th>ROADMAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Metal Layers per Side</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>A Glass Core Thickness</td>
<td>300 to 700 µm</td>
<td>100 µm</td>
</tr>
<tr>
<td>Core Via Diameter</td>
<td>40 µm</td>
<td>10 µm</td>
</tr>
<tr>
<td>Core Via Pitch</td>
<td>80 µm</td>
<td>40 µm</td>
</tr>
<tr>
<td>G, H Line / Spacing</td>
<td>15 µm / 15 µm</td>
<td>10 µm / 10 µm</td>
</tr>
<tr>
<td>L Copper Thickness</td>
<td>1-10 µm</td>
<td></td>
</tr>
<tr>
<td>M Polyimide Thickness 1 &amp; 2</td>
<td>5-10 µm</td>
<td></td>
</tr>
<tr>
<td>Solder Ball Types</td>
<td>Sn63Pb37, PbSn5, PbSn10, SAC</td>
<td>Cu / Sn Pillars</td>
</tr>
<tr>
<td>Under Bump Metalization (UBM)</td>
<td>ENIG</td>
<td></td>
</tr>
</tbody>
</table>

### TOP VIEW OF CIRCUIT FOR TOP / BOTTOM RDL

### CROSS SECTION - 2 METAL LAYERS (CURRENT CAPABILITY)

### CROSS SECTION - 4 METAL LAYERS (FUTURE CAPABILITY)
| **MINIATURIZATION AND INTEGRATION** |
| **IC PACKAGE, PCB ROUTING AND BREAKOUT REGIONS** |
| **MATERIALS SELECTION** |
| **PROTOCOL COMPLIANCE** |
| **COST CONTROL** |
| **POWER AND THERMAL MANAGEMENT** |

| **PACKAGE AND PCB DESIGN** |
| - Bumpout / ballout optimization |
| - Ballout transition structures |
| - Layout & routing |
| - Materials recommendations |

| **MODELING AND SIMULATION** |
| - Validate implementation and signaling requirements for critical channels |
| - High bandwidth full-wave simulations |
| - Design rules for package and PCB designs |
| - Simulations via High-Performance Computing (HPC) |

| **ANALYSIS, TESTING & VALIDATION** |
| - Characterization at frequencies to 67 GHz and beyond |
| - Package, PCB and system-level Signal Integrity / Power Integrity |
| - Material characterization |
| - Post-design test, simulation and measurement |
| - Measurement of test structures for Signal / Power Integrity optimization |
Support and services are available at any level required: from early stages of the design process including package design, material selection and PCB routing, through in-depth analysis, modeling and simulation, with measurement validation services available to 67 GHz, Samtec Teraspeed Consulting and Signal Integrity Group engineers help optimize and validate high-performance systems.
Samtec isn’t just another connector company. By integrating specialized Technology Centers led by industry experts working side-by-side, Samtec fosters a unique environment conducive to true innovation and collaboration, along with the ability to provide the most complete level of service and support for interconnect system design, development and production in the industry.
Dedicated Optical Engineering Team for Design, Development & Application Support

In-house R&D and Manufacturing of Precision Extruded Micro Coax & Twinax Cable

Development of High Performance Cable Solutions for 56 Gbps and Beyond

Expertise in Micro Optical Engines & Active Optics

SAMTEC OPTICAL GROUP

HIGH-SPEED CABLE PLANT

26-38 AWG, 50Ω / 75Ω / 85Ω and 100Ω Systems

Application Specific Interconnect Design & Development

Precision Stamping, Plating, Molding & Automated Assembly

Advanced Interconnect Design

High-Performance Interconnect Design

PCB Layout, Routing and Breakout Region Design Recommendations

Engineering of Solutions for Design Flexibility, Ease of Processing & Supply Chain Risk Management

Design Support for High-Performance Interconnects

For more information, please visit: www.samtec.com/tech-centers