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Tips and Advanced Techniques for Characterizing a 28 Gb/s Transceiver

Jack Carrel, Xilinx

Robert Sleigh, Agilent Technologies

Heidi Barnes, Agilent Technologies

Hoss Hakimi, Xilinx

Mike Resso, Agilent Technologies

Abstract

SERDES links screaming along at 28Gb/s are not trivial to validate and measure. The entire serial transmission and measurement eco-system must be considered to accurately characterize the waveform and jitter performance at the device pin. Even the best of characterization boards will end up with signal degrading vias, transmission lines, and connectors on the path from the device to the measuring instrument. Accurate de-embedding requires careful selection and measurement of calibration structures. Measurement based model building enables verification and optimization of the measurement reference planes. Additionally, the PLL, bandwidth, and peaking enable the recovery of accurate and compliant jitter measurements with sub-picosecond resolution. The design and de-embedding of the test fixture path along with the instrument set-up play an important part in the ability of an oscilloscope to recover the undistorted waveform from a transmitter pumping out bits every 36 pS.

Author(s) Biography

Heidi Barnes, is a Senior Application Engineer for High Speed Digital applications in the EEs of EDA Group of Agilent Technologies. Past experience includes over 6 years in signal integrity for ATE test fixtures for Verigy, an Advantest Group, and 6 years in RF/Microwave microcircuit packaging for Agilent Technologies. She recently rejoined Agilent Technologies in April, and holds a Bachelor of Science degree in electrical engineering from the California Institute of Technology.

Mike Resso, the Signal Integrity Applications Expert in the Component Test Division of Agilent Technologies, has over twenty years of experience in the test and measurement industry. His background includes the design and development of electro-optic test instrumentation for aerospace and commercial applications. His most recent activity has focused on the complete multiport characterization of high speed digital interconnects utilizing Time Domain Reflectometry (TDR) and Vector Network Analysis (VNA). Mike has twice received the Agilent Technologies Spark of Insight award for his contributions to the company. Mike received a Bachelor of Science degree in Electrical and Computer Engineering from University of California.

Rob Sleight is a Product Marketing Engineer for sampling scopes in Agilent Technologies' Oscilloscope Products Division. He is responsible for product development for the division's high-speed electrical and optical digital communications analyzer and jitter test products. Rob's experience at Agilent Technologies/Hewlett-Packard includes 5 years in technical support, and over 8 years in sales and technical marketing. Prior to working at Agilent Technologies/HP, Rob worked for 10 years at Westel Telecommunications in Vancouver, British Columbia, Canada, designing microwave and optical telecommunication networks. Rob earned his B.S.E.E. degree from the University of Victoria.

Jack Carrel is an Applications Engineer at Xilinx. He has over 25 years of experience in product development and design in the fields of Instrumentation, Test and Measurement, and Telecommunications. His background includes development of electro-optic modules, Multi-gigabit transceiver boards, high speed and high resolution data acquisition systems for government and commercial applications. Most recently he has been involved in product design using multi-gigabit transceivers with specific focus on PCB design issues. He has published in several professional publications. Jack received his Bachelor of Science degree in Electrical Engineering from the University of Oklahoma.

Hoss Hakimi is a Principal Engineer at Xilinx. He has 20+ years of experience at various Telecom, semiconductor, and computer industries specializing on high level behavior modeling and top-down design methodology in ASIC/FPGA design, synthesis, Substrate Design, 3D Interconnect Parasitic Extraction, Understanding of high speed signal integrity and PCB power integrity and simulation. Hoss holds an Electrical Engineering from San Jose State University, and he has completed MS courses in the EE department at University of California Berkeley.

Introduction

With the increased use of data services, the performance demand at every level of the network is increasing. Just a few years ago, the state of the art was 11 Gigabits per second (Gb/s) serial channel data transmission. New standards such as OTU4 and 100 GbE, now require greater rates of data throughput, while at the same time demanding lower power and a smaller physical footprint. These new standards now call for transceiver rates in excess of 25Gb/s per channel. As a result of this demand, engineers must now design, develop and validate boards and systems that have multiple 28Gb/s transceiver channels⁽¹⁾. With transceivers running at these rates, the entire serial transmission and measurement eco-system is challenged. The serial transmission channel must be designed to support these significantly greater bandwidths. Additionally, the task of designing, developing, qualifying and validating the physical hardware layer must adapt to these new challenges. Not only does this mean that the test equipment hardware must be able to support the increased bandwidth and dynamic range, but now the instrument software must also be able to remove the unwanted effects of the interconnecting structures between the DUT and the test equipment input ports.

Xilinx has manufactured and assembled a printed circuit board test vehicle for the purpose of demonstrating and characterizing the aforementioned advanced FPGA with the 28 Gb/s transceivers. Although great care was taken in the design and fabrication of the board, there is still some degradation in the signal between the launch point at the device package pins and the board connectors. For a user to effectively evaluate the transceiver, they must be able to view the original signal as it appears at the package pin. Attempting to probe the signal at the package pin is not possible because the vias at the package pin are back drilled and are not readily accessible through traditional probing techniques. Even if one could access the pins at the package pin vias, the probe itself would create even more problems by disturbing the signal integrity of the channel through the observer effect.

The effects of the interconnection between the test equipment and the DUT can no longer be ignored as risetimes drop to 15pS (~2mm electrical length on a PCB) for a 28 Gb/s data rate and the corresponding transmission bandwidth jumps to 33 GHz. In complex systems, there is impairment on the connecting fixture channel caused by package ballout, board vias and traces, connectors, and cables. Since the channel transfer function acts like a low pass filter, it is critical to be able to isolate one segment at a time and optimize the path for the targeted frequency range. The ability to de-embed the interconnecting fixture channel requires up-front design of calibration standards to correctly place reference planes at the DUT pins as well as EM simulations to validate and adjust the calibration standards for improved accuracy⁽²⁾. De-embedding of the fixture from a measurement is not new, but the analysis and trade-offs that must be made in identifying the correct methodology for a 28 Gb/s SERDES measurement at the DUT pin brings up questions like AFR 2x Through vs. TRL calibrations⁽³⁾, partial vs. full de-embedding, and filtering vs. bandwidth to support Fourier Transforms and Nyquist sampling requirements. The challenge accepted in this experimental signal integrity project is in demonstrating the design, simulation, measurement, processing, and validation of the fixture de-embed model for a given application.

Overview of a 28Gbps SERDES Channel

A printed circuit board was designed and built with the following goals:

1. Provide a set of channels for carrying 28Gbps signals from the Xilinx FPGA to an external device such as a piece of test equipment.
2. Provide a set of test structures that assist with de-embedding the PCB channel.

The signal path for the 28Gbps signals is from the Xilinx Virtex-7 FPGA to SMA connector that is the working point for connection to devices such as test equipment (e.g. oscilloscopes) or data transmission devices (e.g. optical transceivers). The components of the signal path are:

1. BGA to PCB interface structure including the solder ball pad and BGA launch structure on the PCB.
2. Differential loosely coupled embedded stripline traces
3. PCB to connector interface structure including vias and connector PCB pads.
4. Samtec BullsEye™ connector and test cable.

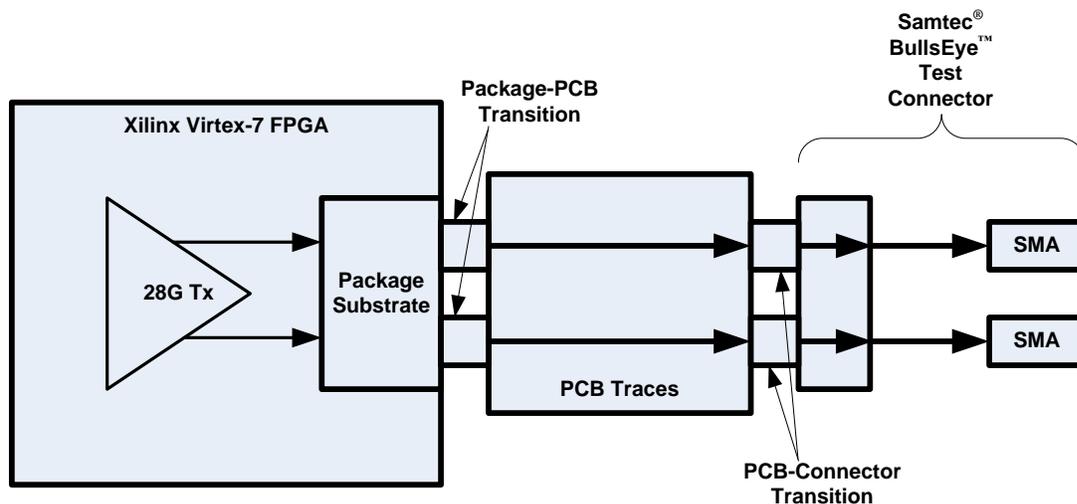


Figure 1: 28G Signal path

The printed circuit board consists of the FPGA launch structure, a differential stripline and the Samtec BullsEye™ connector interface. Figure 2 shows the design parameters for the stripline and the resulting detailed layout of the 28Gbps channels. Figure 3 shows the full board with the additional test fixture calibration structures.

Net	Etch Length (in)	Routing Layer	Trace Width (mil)	Trace Spacing (mil)
TX0	2.683	5	3.75	8.25
TX1	2.293	5	3.75	8.25
TX2	2.298	5	3.75	8.25
TX3	2.501	5	3.75	8.25
TX4	2.698	5	3.75	8.25
TX5	2.373	5	3.75	8.25
TX6	2.607	5	3.75	8.25
TX7	2.804	5	3.75	8.25

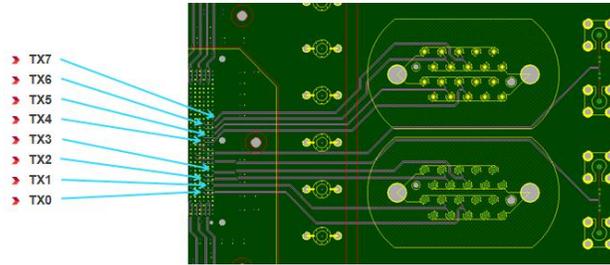


Figure 2: VC7222 28Gbps internal stripline routing design parameters and the resulting Detail 'A' PCB layout with the location shown in Figure 3.

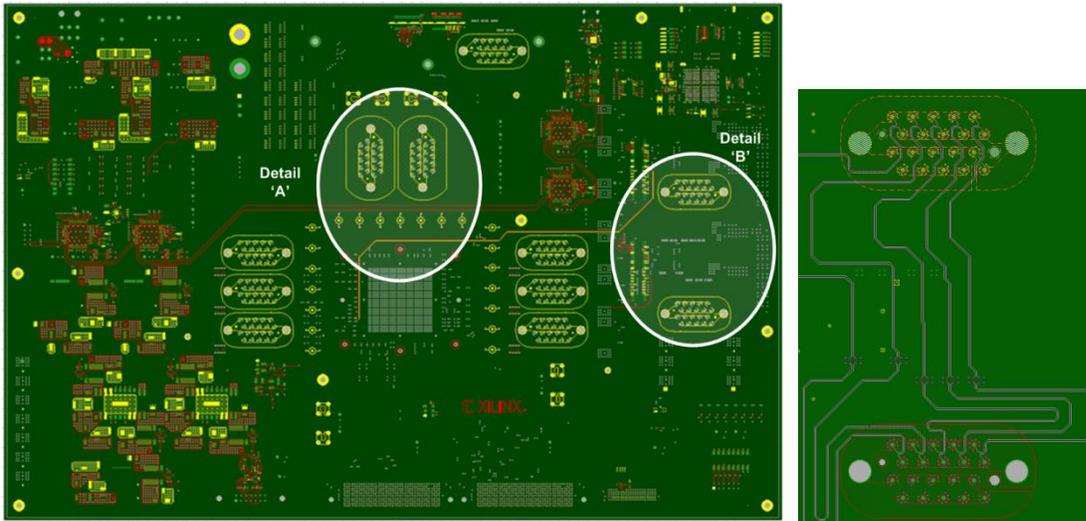


Figure 3: Top view of the VC7222 PCB with the 28Gbps Channels in Detail 'A' and the test fixture calibration structures in Detail 'B', which are expanded on the right to show the inner layer routing.

Test Fixture Calibration Structures

To facilitate a fast and accurate method of channel fixture characterization for de-embedding purposes a set of calibration test fixture structures were designed and incorporated into the board layout (Detail B of Figure 3). Figure 4 shows the basic design of the test fixture. As shown, the test fixture is composed of two copies of the path from the BGA ballout to the connector. The two copies are a mirror image of each other and are connected between the two copies of the BGA launch. It should be noted that the separation between the two BGA launch structures must be sufficient to eliminate interaction between the two structures. This structure utilizes an exact matched trace length with one of the 28 Gbps channels. A second structure with 2 inches of additional stripline routing is also included in the test structures for the purpose of extracting the PCB as fabricated material properties.

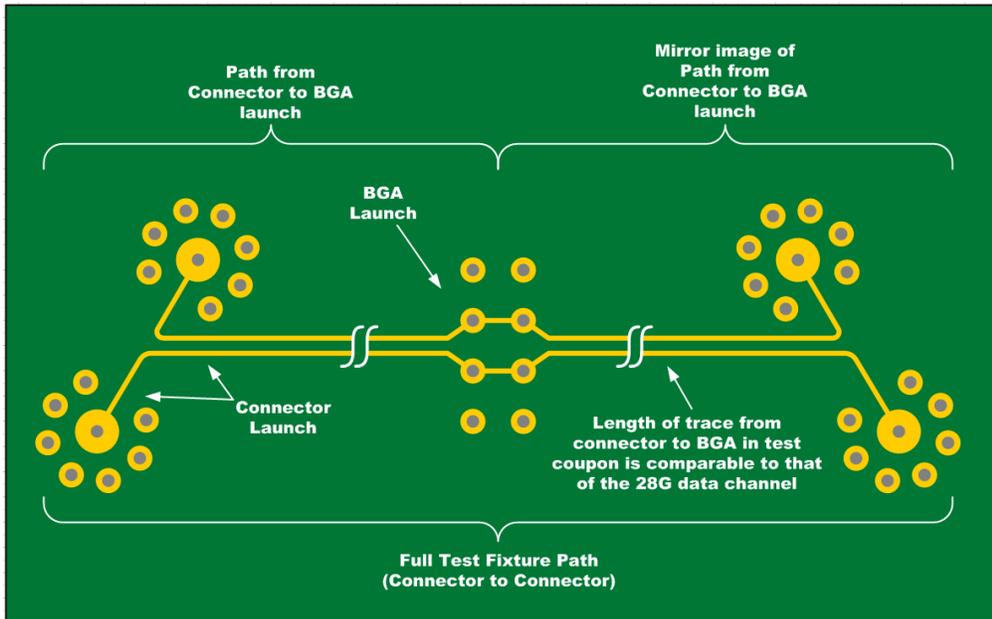


Figure 4: Calibration test fixture design

Test Methodology

To verify the validity of fixture de-embedding for this 28Gbps application it is necessary to step through a series of measurement comparisons. Initial Tests 1 and 2 shown in Figure 5 utilize an independent 28 Gbps pattern generator to show how this source signal can pass through the 28Gbps channel paths shown in Figure 2 and through the use of fixture model de-embedding get back to the reference source signal. The same test is repeated in Tests 3 and 4 but this time utilizing the 28Gbps source from the output of a VC7222 Xilinx V7 PCB to run through the 28Gbps channel on a second PCB. Steps 1-4 validate the de-embedding process for the given application. The next step is to measure the signal with the V7 DUT installed on the board and compare 3 methods of obtaining the fixture de-embed model. Test 5 utilizes direct probing of the channel path for the de-embed model and is the same model that was used for de-embedding in steps 2 and 4. Test 6 utilizes a de-embed model from a 2x through AFR measurement of the matching test fixture calibration structure for the 28Gbps channel. Test 7 utilizes a hybrid measurement based simulated model for the fixture de-embed. The final Test 8 looks at the performance at the DUT BGA package pins and evaluates the issues with full and partial de-embedding.

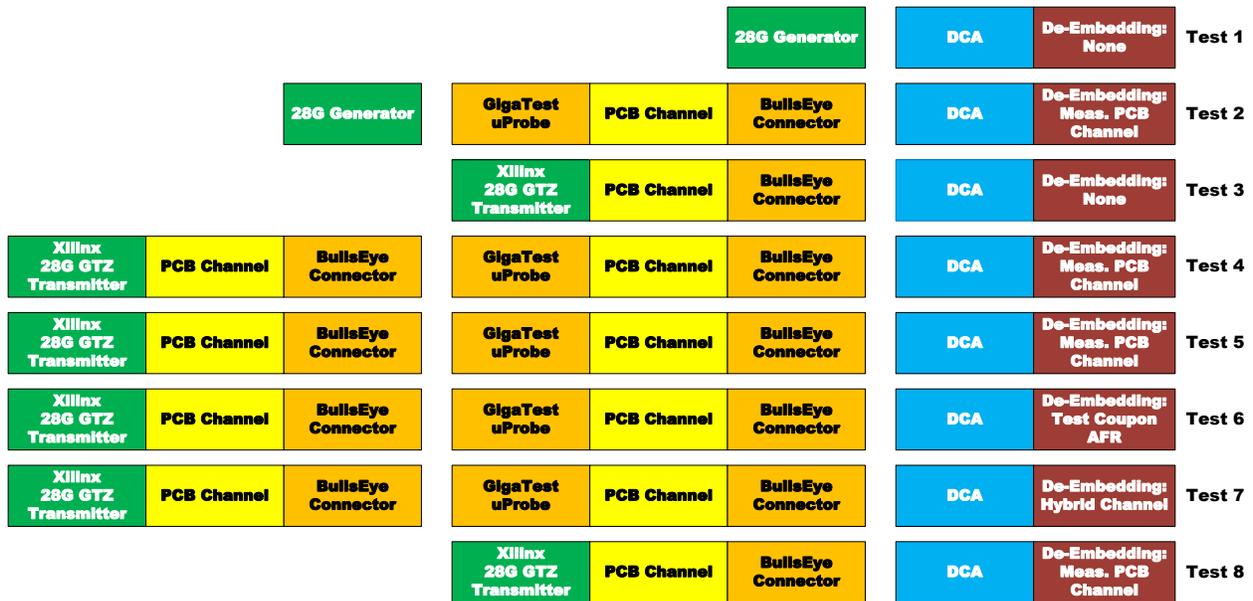


Figure 5: Planned measurements for verification of fixture de-embedding methodology.

Test Fixture Characterization

High Density Hybrid Fixture De-Embedding Methodology

The challenge of fixture de-embedding is not new and there are numerous techniques available for careful calibration and measurement of a fixture. The challenge now facing the high speed signal integrity designer is that it is no longer just one or two test fixtures that need de-embedding but multiple fixture paths as speeds and density increase. High density boards usually do not have the luxury of equal length routing on the same layer. Therefore each high speed connection to a DUT can end up with a different routing path for de-embedding. In such cases, one has to make trade-offs between cost, time and performance to find a realistic solution.

The much published technique of TRL calibration to move a measurement reference point onto a PCB quickly becomes a PCB space hog. It is also time consuming to implement for differential pairs with coupling and multiple fixture paths for characterization. Using newer methods of symmetrical 2x through splitting of the S-Parameters such as Automatic Fixture Removal (AFR) makes more efficient use of board space and provides a reduction in measurement time [2]. In the case of longer path lengths, however, even this 2x through method requires a significant amount of board space for the fixture test structures. Direct measurement of the channel fixture with coaxial probes (Figure 6) is another option which works quite well but typically requires a significant investment in measurement hardware for probing and an additional investment in optimized probe interposer interfaces for improved impedance matching [3].



Figure 6: High performance Ground-Signal-Ground probes for direct measurement of the channel fixture path for de-embedding from the active measurement of the DUT to accurately predict the performance at the package. (Probes courtesy of Gigatest Labs)

A more practical solution is to leverage a hybrid of measured and simulated data to quickly characterize a variety of fixture paths and provide the S-Parameters for de-embedding. In the case of the Virtex7 DUT PCB board, the channel fixture consists of the PCB path and the Samtec BullsEye™ cable with connectors. Running an EM simulation of this full path including the board, connector, and cable would be very time consuming and resource expensive due to the complexity of the connector interfaces and length of the coaxial cable. The better choice for characterizing the connector plus cable is to create a loopback path between adjacent pins as shown in Figure 1. Then use the AFR 2x through method to split the measurement in half obtaining measured data for each cable connection to the desired PCB layer. This short loopback path requires very little space on a PCB and enables quick re-characterization of a cable and connector. Also, multiple connector cable assemblies can be characterized using a single PCB footprint.

Cable Fixture Measurement

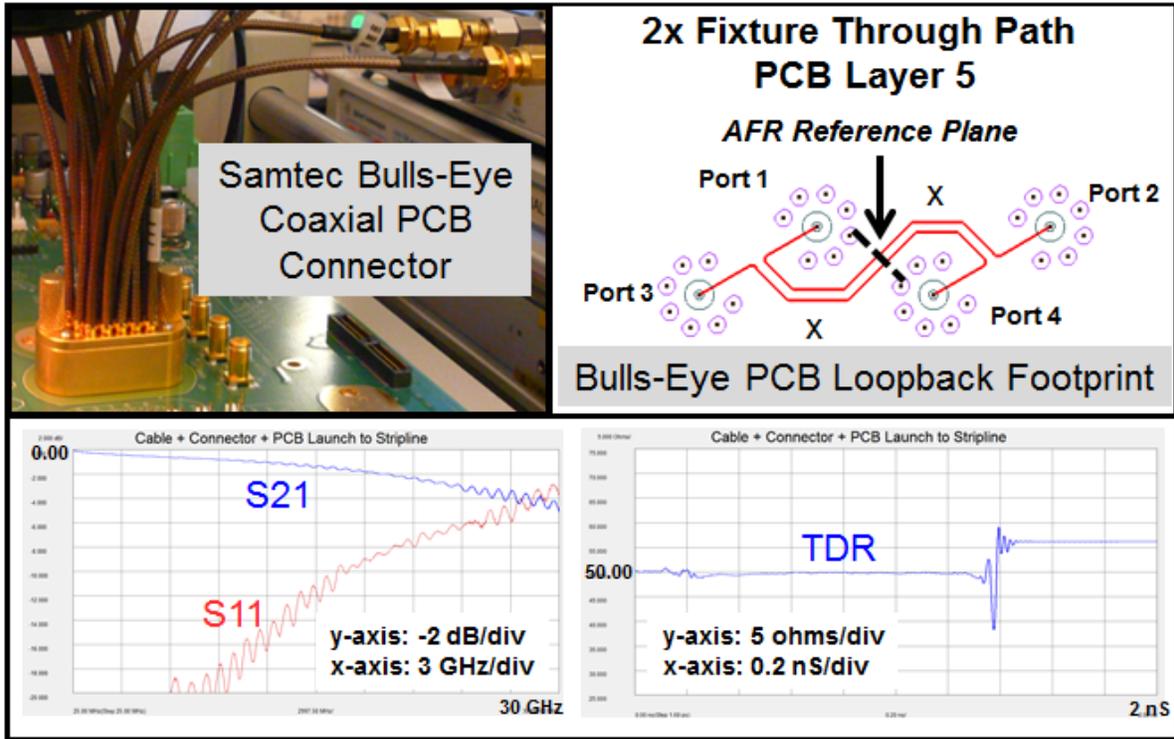


Figure 7: The 1x path length fixture data for the coaxial cable connection to the PCB can be measured using a 2x symmetrical through AFR calibration to split the 2x through path in half and get the S-Parameters for each cable connection to the PCB inner layer. This also provides a quick verification of cable performance in the event a cable is suspected of being damaged through mating and de-mating cycles.

The remaining PCB path does not have 3-dimensional complexity of the cable and connector and it is unlikely to change over time. So for this case, simulation is a much faster and far less costly method of characterizing a variety of fixtures. The accuracy of the simulation method does depend on the ability to extract out the correct loss vs. frequency material properties. So, a characterization path for each signal layer on the board is still required. At a minimum two calibration structures are needed each with the same fixturing connections, but one with an added length of PCB routing so that the material losses can be separated from those of the connecting transitions and connectors, see Figure 8.

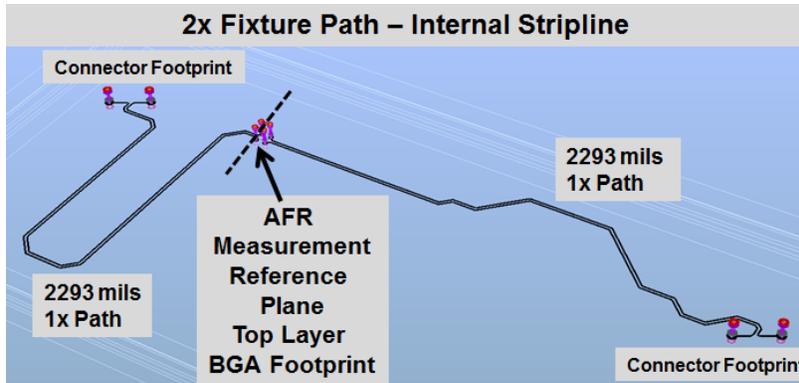


Figure 8: The full 1x fixture path including the cable and the PCB inner layer differential pair stripline routing can be measured using the 2x Fixture Through path with the reference plane located at the top layer BGA via pads. Implementing an additional 2x Fixture path with 1 inch added to each side for a 1x fixture length of 3293 mils enables measurement of material properties and simulated fixture data for the remaining DUT fixture paths.

Dielectric constant is calculated from the difference in electrical length of 325 pS for the added 2 inches of trace length [4]:

$$\begin{aligned} \epsilon_r &= \left(\frac{c}{v}\right)^2, \text{ where } c \text{ is the speed of light and } v \text{ is the velocity of the signal} \\ &= \left[\frac{(0.0118)}{\left(\frac{2}{325}\right)}\right]^2, \text{ where length is in inches and time is in picoseconds} \\ &= 3.7 \end{aligned}$$

The remaining material properties are extracted by tuning a Multi-Layer Transmission Line Model with various sections of impedance discontinuities. The modeled TDT and TDR is matched to the measured data for the short 2x through path and then tuned so that the material properties accurately predict the longer 2x path with the additional 2 inches, see Figure 9. Once the material properties are known and a measurement based model is created, they can be leveraged to simulate the varied routing of any of the SERDES 28Gbps channel paths going to the DUT. The simulated data of the PCB path is easily cascaded with the appropriate cable assembly measured data or a nominal model of the cable fixture path to create the full-path fixture losses for de-embedding.

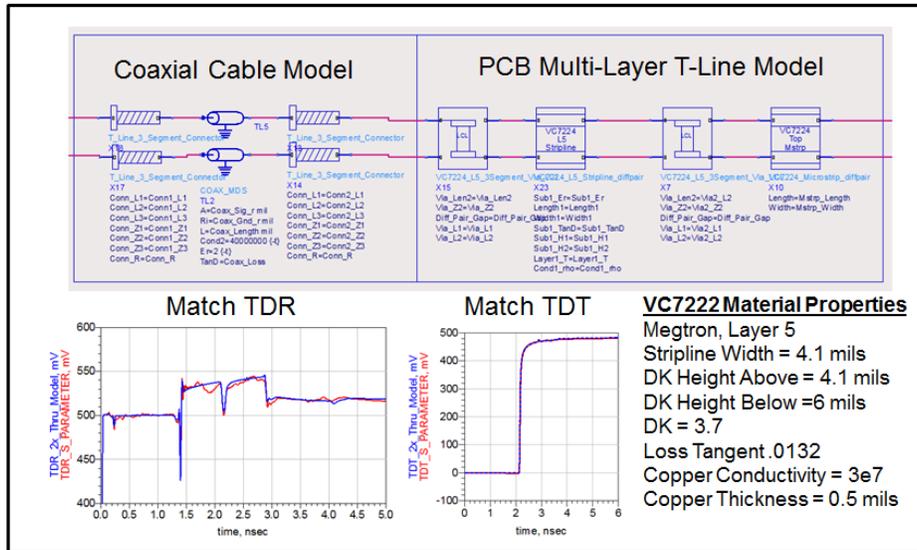


Figure 9: Creating a measurement based model by matching transmission line impedances with that of 2x fixture test structures enables the extraction of material properties and the ability to quickly simulate all the fixture paths for a given routing layer.

The measurement based model runs in a matter of minutes to generate the distribution of fixture losses for de-embedding. In Figure 10 is an example of how a large number of paths with varying length can be simulated for loss vs. frequency and then this fixture loss de-embedded from the measurements. This eliminates the need for matching routing lengths for all lanes to that of the worst case longest routing which consumes added board space and can significantly increase the layout designers routing complexity. This technique of using the shortest route for each high speed connection also ensures the best overall performance by minimizing the amount of correction needed for each channel. Obviously there is a noise floor limit to how well any calibration or de-embedding technique can work and the lower the losses the better the signal to noise ratio will be for all types of de-embedding techniques(6).

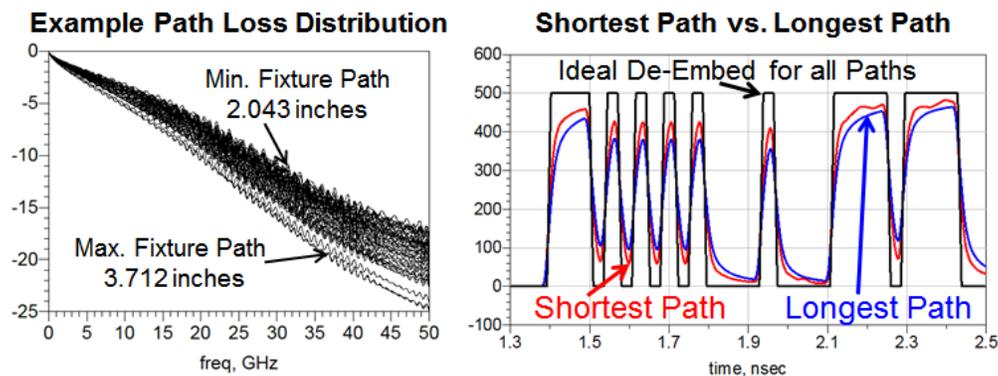


Figure 10: The measurement based hybrid model of the fixture path quickly simulates all of the possible paths on a given PCB layer as shown in the plot on the left. The plot on the right shows the variation in bit shape between the longest path and the shortest path and the ideal source input bit pattern that is desired after fixture de-embedding

This hybrid model methodology combining measured cable data with measurement based transmission line models of the signal path provides an effective way to quickly generate fixture de-embedding files to obtain the signal at the DUT package bumps. Full EM simulations can also predict fixture losses, but with simulations running on the order of hours and days vs minutes there is a lot of value in starting with a good 1st order model for fixture de-embedding that can be quickly adapted to the lot to lot variations that are inherent in low cost PCB manufacturing.

Oscilloscope Measurement Techniques

Precision probing on high-speed devices requires high-bandwidth probes and a probe station with a camera. However, for optimum measurement fidelity and ease-of-use, accurate device characterization is usually performed by connecting test equipment to the device-under-test (DUT) via a fixture and high quality coaxial cables.

If the high speed channel fixture band limits the signal from the DUT, the resultant signal measured by the test equipment will be distorted. However, if the fixture is accurately characterized through measurement or modeling (or ideally both), it is possible to remove, or de-embed, the effects of the fixture and/or cables from the measurement. It is important to note that de-embedding should not be expected to absolve the designer from using good fixture design techniques and materials. De-embedding has its limitations and every effort should be used to minimize signal degradation due to a fixture.

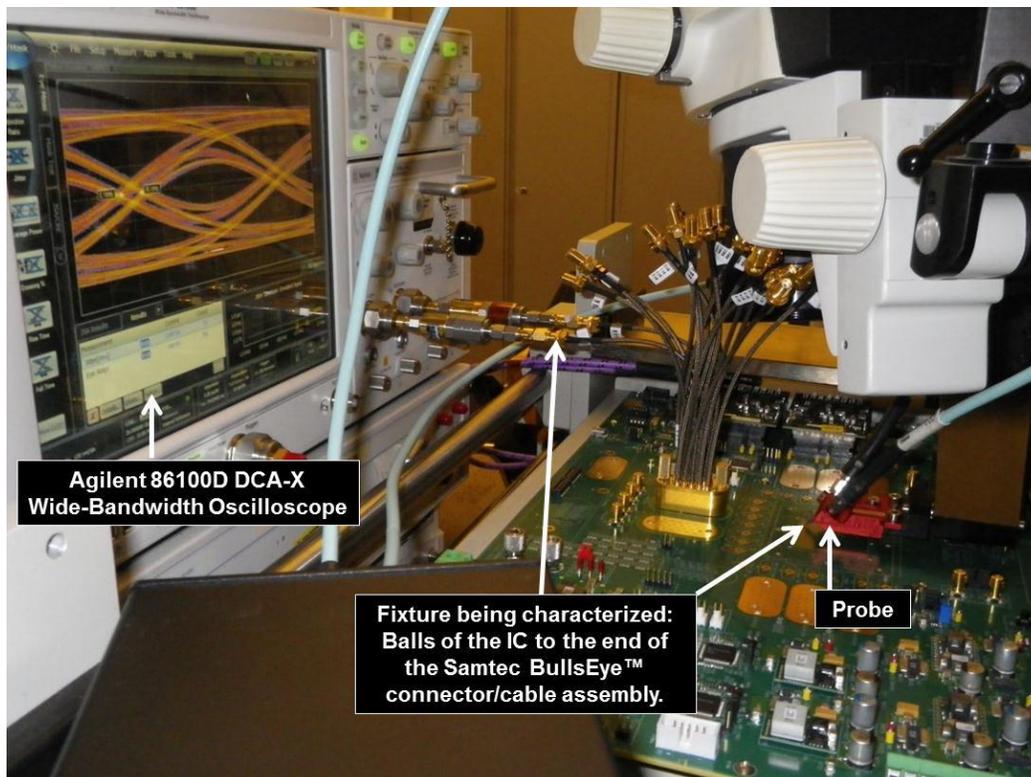


Figure 11: A probe station was used to launch a reference signal onto the high speed channel fixture using a probe, and the signal at the output of the fixture was then analyzed using a wide-bandwidth oscilloscope.

Limit Fixture Loss

De-embedding software takes the S-parameter file and creates an inverse transfer function which is then used to deconvolve the fixture response from the incoming signal.

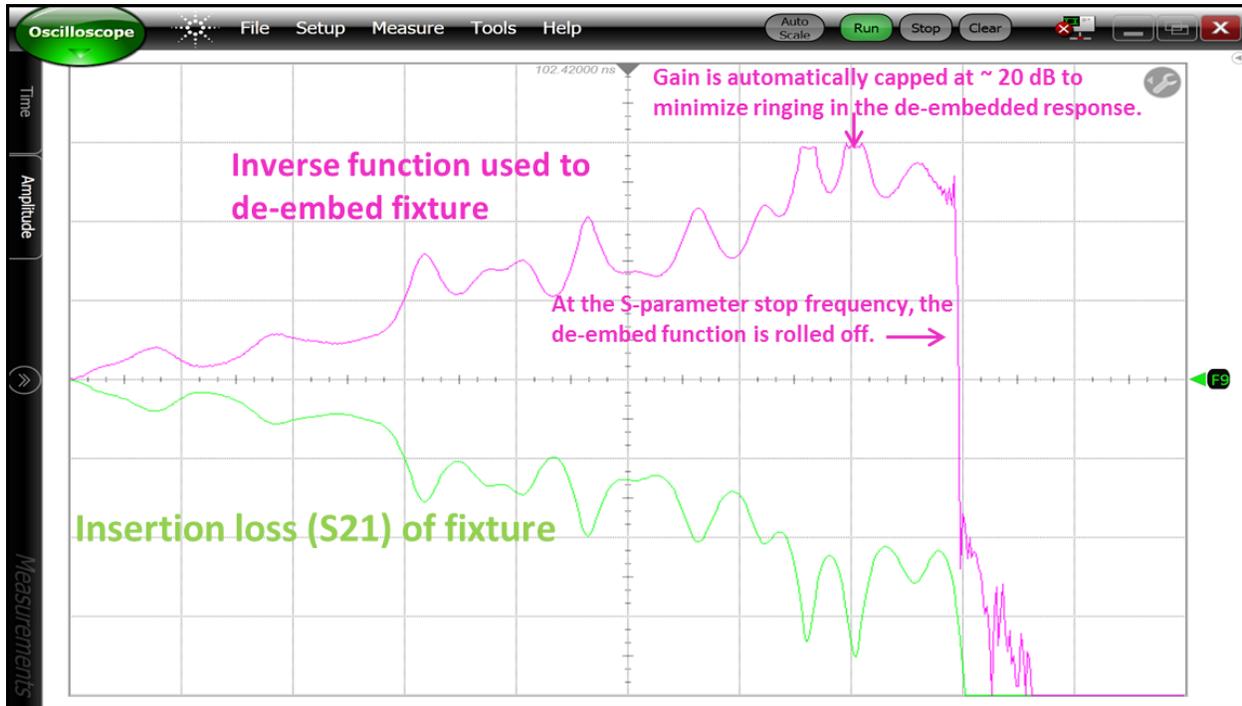


Figure 14: Frequency vs amplitude plot of a fixture's insertion loss profile (bottom trace S21) and the corresponding inverse function (top trace) used by de-embedding software to compensate for fixture effects.

Although the deconvolution process can apply 20 dB of gain or more in order to compensate for loss through a channel, it is unlikely a designer will be satisfied with the quality of the de-embedded signal. While spectral energy from the DUT will be amplified by an amount equal to the fixture loss at a given frequency, system noise will be amplified as well. Anytime 15 to 20 dB of gain is applied to an incoming signal, the de-embedded signal will typically include a high amount of noise. This is true of all wideband measurements that are made with all oscilloscopes. If the user has a narrowband instrument such as a vector network analyzer available, then applying 15 to 20 dB of gain does not result in a high amount of noise because of the low system noise of VNAs.

S-parameter Stop Frequencies

Ringing will occur whenever a data signal is filtered with a Sinx/x filter response. This type of response is often used to roll-off the inverse function at the frequency where the S-parameters stop. Therefore, it is beneficial to roll-off the response at a point where the inverse function's gain is not maximized, DUT energy content is at a minimum (a null), and/or the function's cutoff frequency is beyond the bandwidth of the oscilloscope.

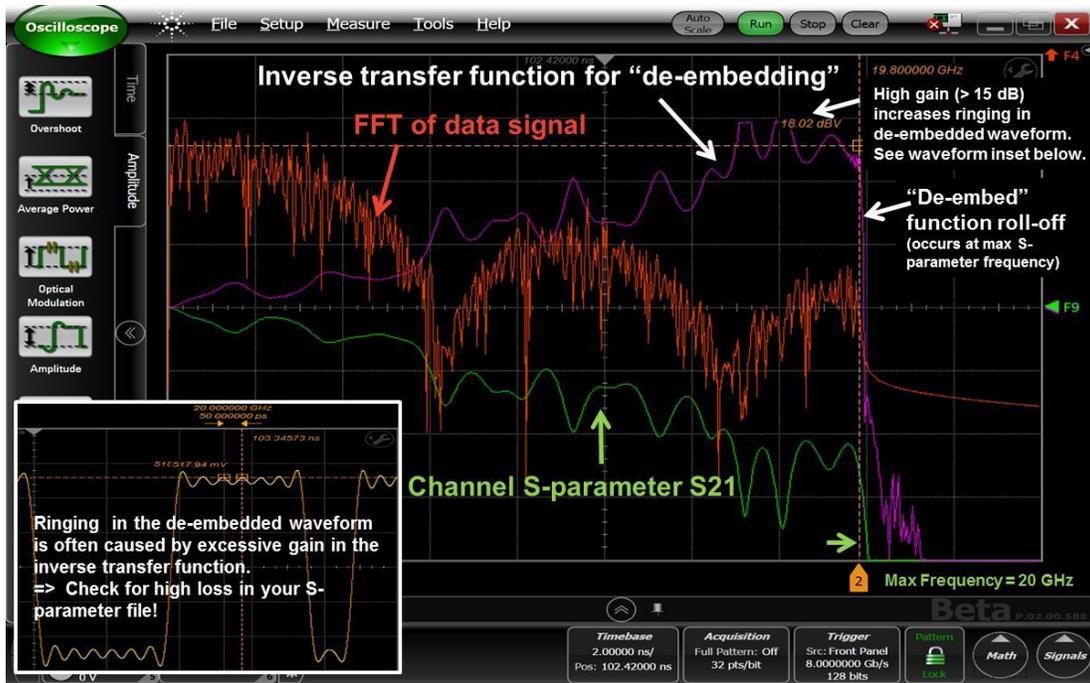


Figure 15: Frequency plot showing S21(green), inverse S21 function(purple), overlaid with the FFT of the data signal (orange). Attempting to de-embed too much loss often results in ringing in the de-embedded waveform (lower left).

To mitigate ringing in the de-embedded response, the best solution is through proper fixture design (minimize loss and reflections). Once designed, some de-embedding tools such as InfiniiSim-DCA allow users to control the roll-off frequency of the inverse transfer function – it does not need to always be at the maximum S-parameter frequency.

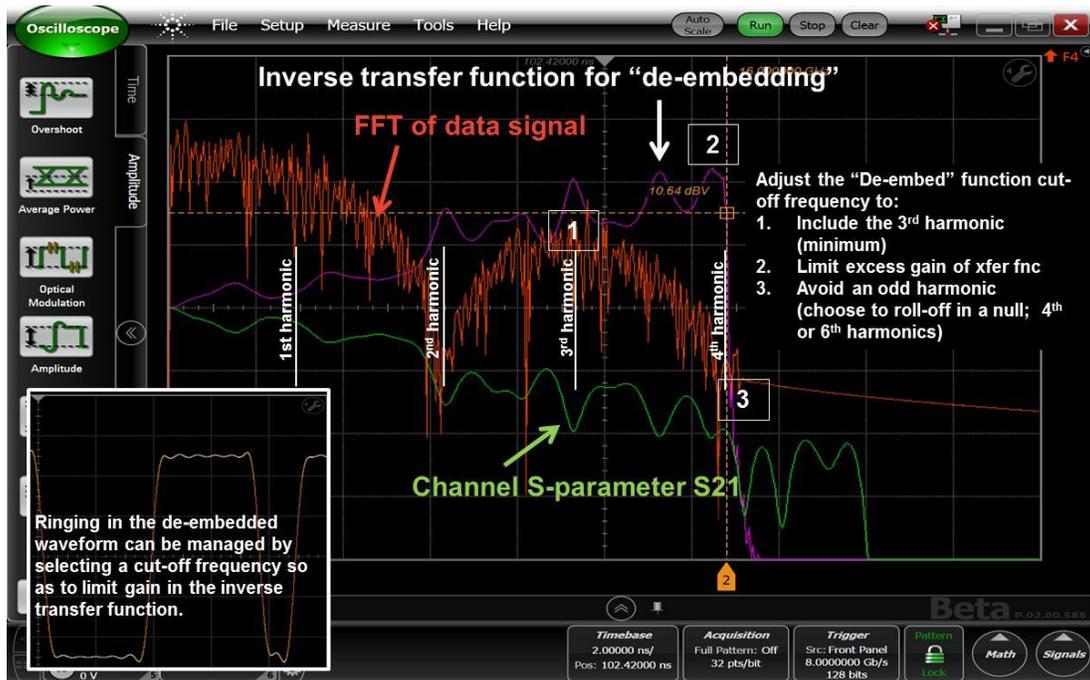


Figure 16: Frequency plot showing the cut-off frequency for a de-embed function (top trace) which has been optimized to minimize ringing in de-embedded waveform.

In the case of a real-time oscilloscope that has a receiver response similar to a Sinx/x filter (used to minimize aliasing), the S-parameters can stop at a frequency equal to or less than receiver bandwidth. But in the case of a sampling scope where the receiver response rolls off much more slowly, the receiver has useable frequency response well beyond the 3dB frequency. Therefore, it is beneficial to use S-parameters that have a stop frequency that is at least 1.5x the 3dB bandwidth of the receiver.

Through measurement it was determined that the spectral content of the experimental DUT, as measured with the fixture, was limited to about 35 GHz. Therefore having an S-parameter file characterized to 50 GHz ensured minimal ringing in the de-embedded response from the Sinx/x filter roll-off.

Noise and Slew Rate Effects on Jitter Results

Noise on a signal, in combination with the signal's slew rate, will be interpreted by a receiver as random jitter. This is sometimes referred to as amplitude modulation (AM) to phase modulation (PM) conversion.

$$\langle \text{Random Jitter due to noise} = \text{Random Noise} / \text{Slew Rate} \rangle \quad \text{Equation 1}$$

The greater the random noise, and/or the slower the slew rate of the signal, the greater the random jitter (RJ). Random noise (RN) sources include noise from the signal itself, as well as intrinsic noise from the oscilloscope. To minimize the impact on RJ results, designers should consider configuring their oscilloscope's bandwidth to capture all the spectral content from the DUT, but no more. While this should be a consideration when using all scopes, it is less of an issue for sampling scopes since their receivers have very low noise compared to a real-time oscilloscope with equivalent bandwidth.

Example:	<u>Random Noise</u>	<u>Slew Rate (V/s)</u>	<u>Induced Random Jitter</u>
	750 μV	2E10	37.5 fs
	5 mV	2E10	250 fs

As shown in the example above, a signal having 5 mV of random noise and slew rate of 2E10 V/s would contribute 250 fs of random jitter to a jitter measurement. Being random in nature, this noise induced jitter has a Gaussian distribution, and as such, will Root Sum Square (RSS) combine with true timing jitter:

$$\text{Measured Random Jitter} = \sqrt{(\text{Timing Jitter})^2 + (\text{Noise Induced Jitter})^2}$$

Example:

- a. Noise Induced RJ = 37.5 fs (noise due to scope + DUT)
 True Timing Jitter = 200 fs
 $\text{Measured Random Jitter} = \sqrt{(200 \text{ fs})^2 + (37.5 \text{ fs})^2} = 203 \text{ fs}$
- b. Noise Induced RJ = 250 fs (noise due to scope + DUT)
 True Timing Jitter = 200 fs
 $\text{Measured Random Jitter} = \sqrt{(200 \text{ fs})^2 + (250 \text{ fs})^2} = 320 \text{ fs}$

As seen, 5 mV of noise riding on a signal can significantly degrade a jitter measurement, increasing measured jitter by over 50% from 200 fs to 320 fs. Additionally, when a signal is de-embedded, the slew rate is typically changed. As a result, de-embedding software such as Agilent Technologies InfiniiSim-DCA is designed to account for AM-to-PM conversion effects when performing jitter measurements on a de-embedded signal.

28 Gb/s SERDES Measurements

As bit rates increase the bit period decreases making jitter margins much tighter. Jitter measurements reported by test equipment include random jitter generated by the device itself, random jitter generated by the equipment's internal timebase, and the jitter due to AM-to-PM conversion, as mentioned earlier. So, for optimal measurement analysis, it is important to select a scope that has both low intrinsic jitter and low noise.

For this reason, we chose to conduct this experiment using the Agilent Technologies 86100D DCA-X sampling oscilloscope with 86108B precision waveform analysis module. The Agilent Technologies 86108B 35/50 GHz bandwidth module has an integrated 32 Gb/s clock recovery circuit and an internal timebase with random jitter < 50 fs typical.

Prior to de-embedding the fixture from our measurements we needed to validate the S-parameter model of the fixture. To gain confidence in the model we chose to validate the model through simulated and real 28Gb/s sources.

A. Predict what we expect to see at the output of the channel

Prior to making any waveform measurements, we implement an easy method to perform a quick sanity check of the model. This method involves simulating a 28 Gb/s signal source using Agilent Technologies FlexDCA software. In Figure 17, D5A Green is the 28G PRBS signal having infinite bandwidth that is convolved with the S-parameter model of the channel fixture. We perform eye measurements on the resultant waveform and eye diagram (F3 pink, Figure 17).



Figure 17: Predicted waveform at the output of the fixture (F3 Pink) when using an ideal 28G input signal (D5A Green).

Notice the lower amplitude and edge speeds resulting from the band-limiting effects of the channel fixture. Some ripple was introduced on the longer strings of 1's and 0's. Wrapping the waveform into an eye diagram allows quick prediction of the eye opening, and the rise/fall times using various patterns.

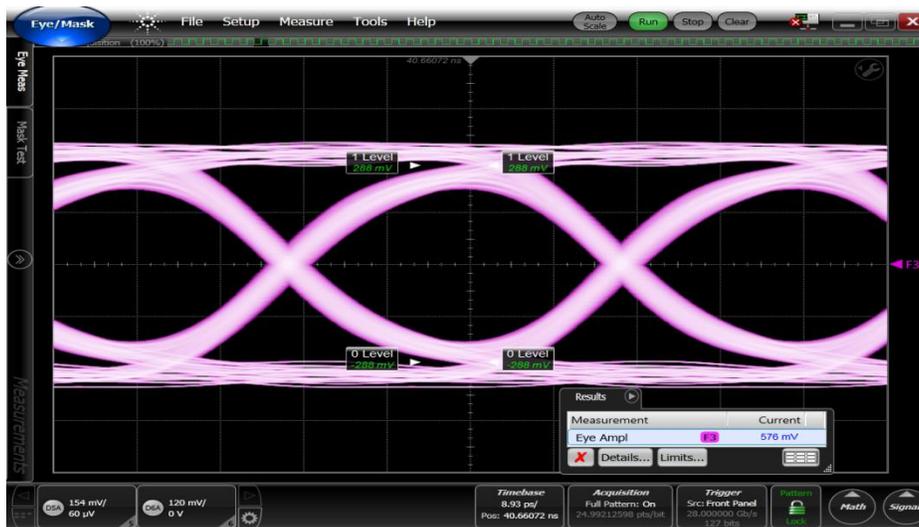


Figure 18: Predicted eye diagram at the output of the fixture (F3 pink).

Despite the fact that the channel is fairly well behaved, at 28 Gbps there are still significant frequency dependent losses that introduce noticeable inter-symbol interference (ISI) and reduces the eye opening. Now that we have predicted the signal at the output of the fixture, we can connect an actual signal to the channel and attempt to validate the S-parameter model of the channel fixture used in the simulation.

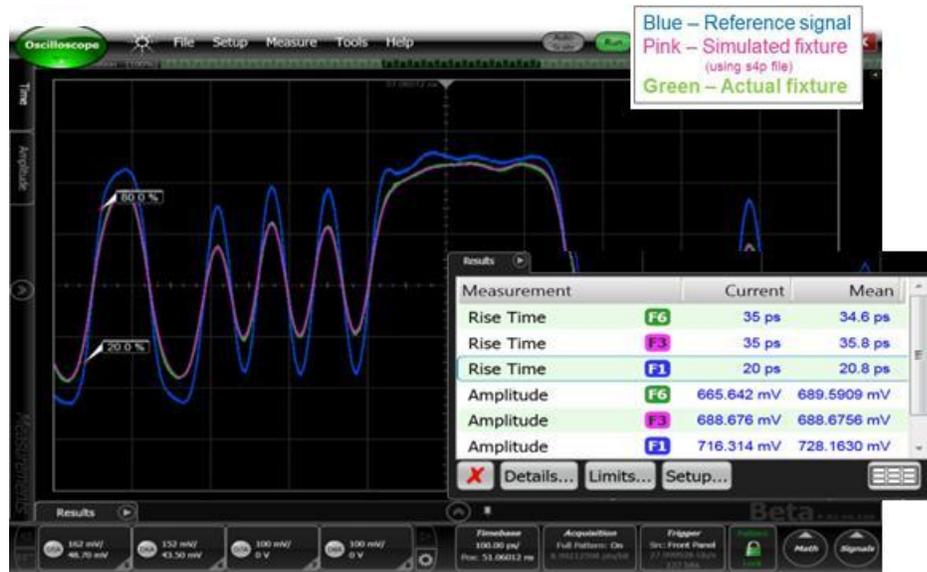


Figure 20: Comparison of waveforms from simulated fixture (F3 pink) and actual fixture (F6 green) showing excellent correlation.

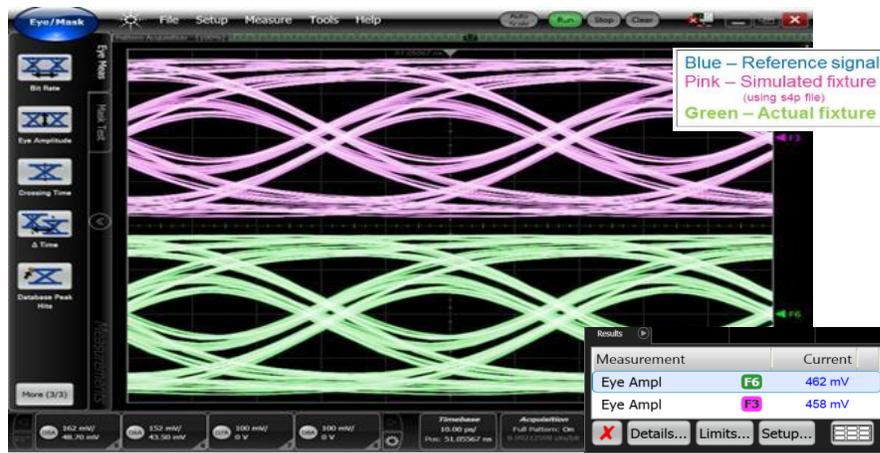


Figure 21: Eye diagram measurements of simulated fixture (F3 pink) and actual fixture (F6 green) showing good eye and amplitude correlation.

Figure 21 compares the simulated and measured eye diagrams. The wave shape shows excellent correlation in the various bit trajectories, which further validates our S-parameter model.

- e. **De-embedded Signal:** de-embed the fixture model from 1(c) and compare to 1(a).



Figure 22: De-embedded signal (F7 pink) compared to reference trace (F1 blue) showing good correlation and provides further model validation.

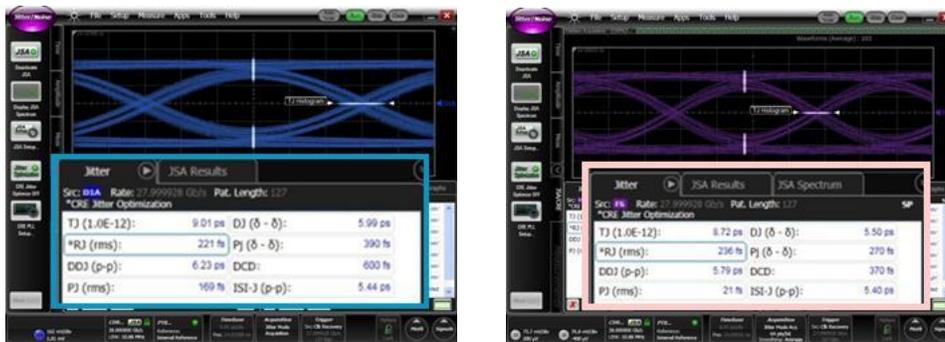


Figure 23: Jitter measurement comparison of de-embedded signal and reference signal; good ISI correlation (both measured and de-embedded signals are 5.4ps) which further validates the model.

Conclusion - Experiment #1: Amplitude, rise/fall times, waveshape, and jitter measurements correlate very well (within 2 %) which validates the S-parameter model to be used for de-embedding purposes.

2. Validate using Xilinx SERDES

We repeat the experiment in #1 above but this time using an actual SERDES as the source.

- a. **Reference Signal:** Directly measure a 28G SERDES using the oscilloscope to establish a baseline for the SERDES output.

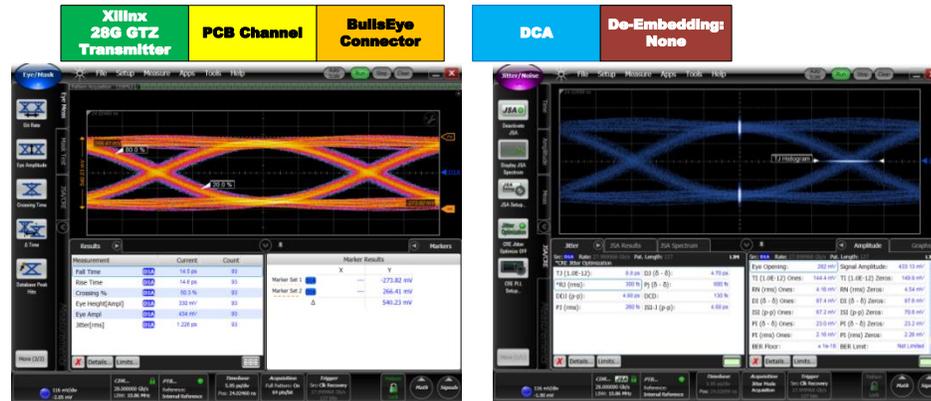


Figure 24: Eye diagram and jitter measurements of the reference signal establish a baseline for subsequent analysis (Rise/Fall times 14.5ps, Eye amplitude 434 mV, ISI 4.8 ps, TJ (@1E-12 8.8 ps).

- b. **Embedded Signal:** Predict what the reference signal should look like after passing through the channel fixture. Pass the source through the model of the channel fixture, and measure the response. (See F2 (pink) trace in Figure 25.)
- c. **Degraded Signal:** Using a probe to launch the reference signal onto the fixture, transmit the signal through the actual channel fixture and measure the response. See F6 (Green) trace in Figures 25 and 26.
- d. **Compare 2(b) and 2(c).** The degraded signals should look similar.

Note that the expected amplitude (F2 Pink trace) shown in Figure 25 correlates very well with the measured data (F6 Green trace) in the 1010 sequence, but the correlation is not quite as good during the long string of consecutive 1's.

Since we did not observe as much mismatch when using the pattern generator (Step 1c above), this slight but increased amplitude deviation is most likely due to increased impedance mismatch between the actual source and the fixture or scope compared to the “ideal” pattern generator. One could test the match between fixture and scope by inserting an attenuator between the actual source and the fixture or scope. (to temporarily improve the return loss and attenuate reflections more than the incident signal).

A full de-embed of the path would account for reflections and would likely improve the match on these consecutive bits, but since they take place in an area which is less important (higher amplitude), designers often find this level of performance acceptable.



Figure 25: The simulated signal (F2 Pink) and actual signal (F6 Green) show good correlation, especially on 1010 bit and isolate bit sequences (most important).

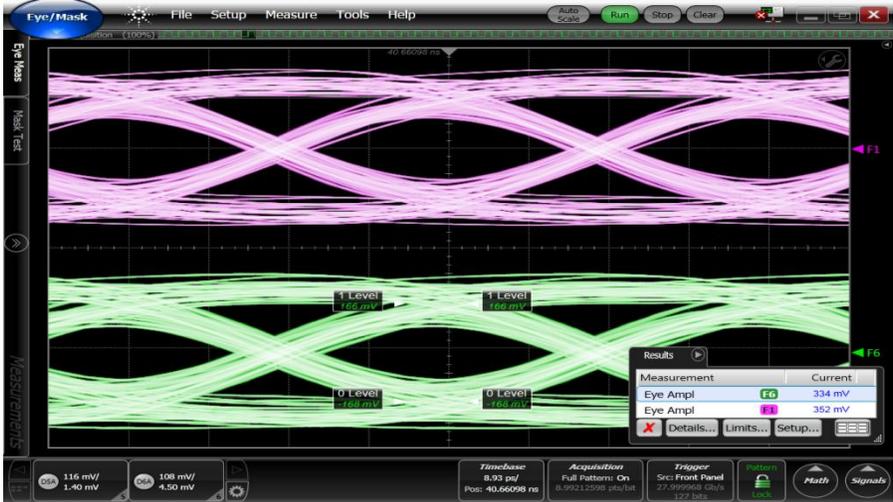


Figure 26: Good correlation between simulated and measured signals.

The similarity in the outlying trajectories is an excellent indication that the S-parameter model is a good representation of the actual fixture.

- e. **De-embedded Signal:** De-embed the fixture model from 2(b) and compare to 2(a).



Figure 27: De-embedded signal (F7 pink) compared to reference trace (F1 blue) shows good correlation and provides further model validation.

The de-embedded signal (F7 pink trace in Figure 27) rise time improves from 25 ps to 17 ps which is very close to the reference signal performance of 15.8 ps (F1 blue in Figure 27). As mentioned above, the amplitude correlation is not quite as good as that found in 1(d) when we used the “ideal” signal source, and this is attributed to the fact we used a partial de-embed (does not account for reflections) instead of a full de-embed.

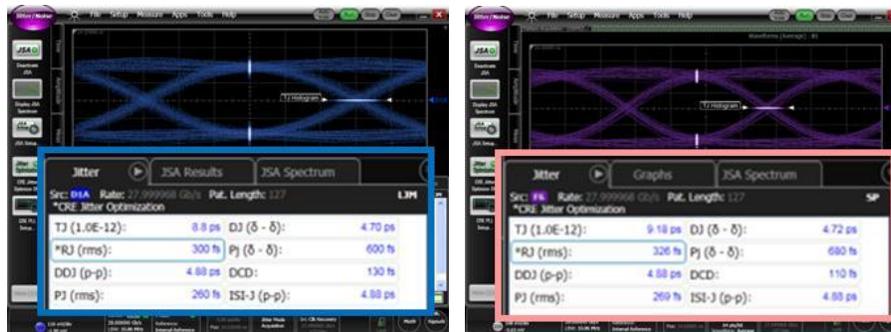


Figure 28: Jitter measurement comparison of de-embedded signal and reference signal; good ISI correlation (measured and de-embedded ISI is 4.88ps) which further validates the model.

Conclusion - Experiment #2: Amplitude, rise/fall times, wave shape, and jitter measurements correlate very well (within 6 %) which validates the S-parameter model to be used for de-embedding purposes.

3. **Validate Automatic Fixture Method (AFR) method for measuring S-parameters**
 We compare de-embedded waveforms using two S-parameter models:

- a. **AFR generated model** from the test fixture structures described at the beginning of the paper .
- b. **Direct measurement model** using the probe station.

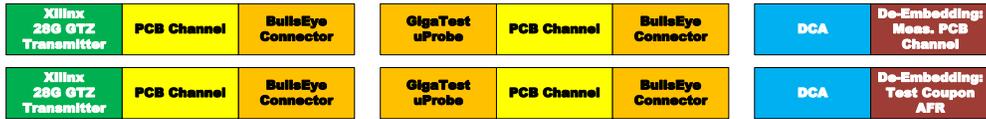


Figure 29: Waveform comparison showing good correlation between de-embedded signal using direct probe measurement model (F7 pink) and AFR model from the calibration 2x test fixture trace (F8 orange).

The de-embedded signal generated from the S-parameter model derived using the AFR measurement method still shows very good correlation to the reference signal (F1 blue in Figure 29) (note the amplitude correlation in the 1010 sequence). While there is slightly better correlation to the reference signal when using the S-parameter model generated from a direct probe measurement of the fixture channel, the AFR generated S-parameter model saves designers considerable time and money (no probing required) and still yields very good results.

4. Hybrid Channel (from ADS)

To further validate the manual S-parameter measurements, we used an EDA design tool (ADS) to model the circuit and generate a hybrid measurement based S-parameter model of the fixture channel as described in the previous Test Fixture Characterization section. Once the hybrid model is created, it is validated through measurement. The advantage of this method is that it can scale to any line length.

The measured signal at the output of the fixture (F6 green trace in Figure 30 below) is de-embedded using three S-parameter files and compared to the reference trace (F1 blue trace). As seen in Figure 30, all three of the de-embedded signals (F2, F5, and F8) correlate very well with one another, and with the reference signal.

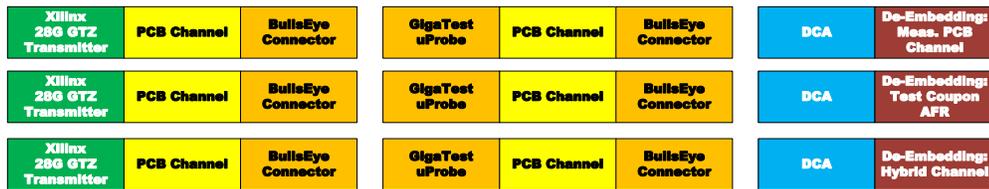


Figure 30: Comparison of de-embedded data using an S-parameter file model generated by direct measurement using a probe (F2 pink), AFR test structure measurement (F8 orange), and a simulated hybrid fixture model using ADS (F5 light purple).

We now have validated two direct measurement S-parameter models and a simulated hybrid model and they are:

- a. **Direct Measurement using a probe station** - more difficult to generate but yields the best correlation with our reference signal
- b. **Direct Measurement of a connectorized test fixture structure (AFR)** – easy to generate, good correlation

- c. **Measurement Based Hybrid Model** – more difficult to generate but scalable to any trace length.

5. Device measurements – de-embed using the validated S-parameter model.

Now that we have validated our S-parameter model through measurement and simulation, we can use it to de-embed the fixture channel from future measurements of the SERDES device installed on the fixture. This allows us to see the true performance of the DUT at the balls of the device without the signal degradation due to the fixture.

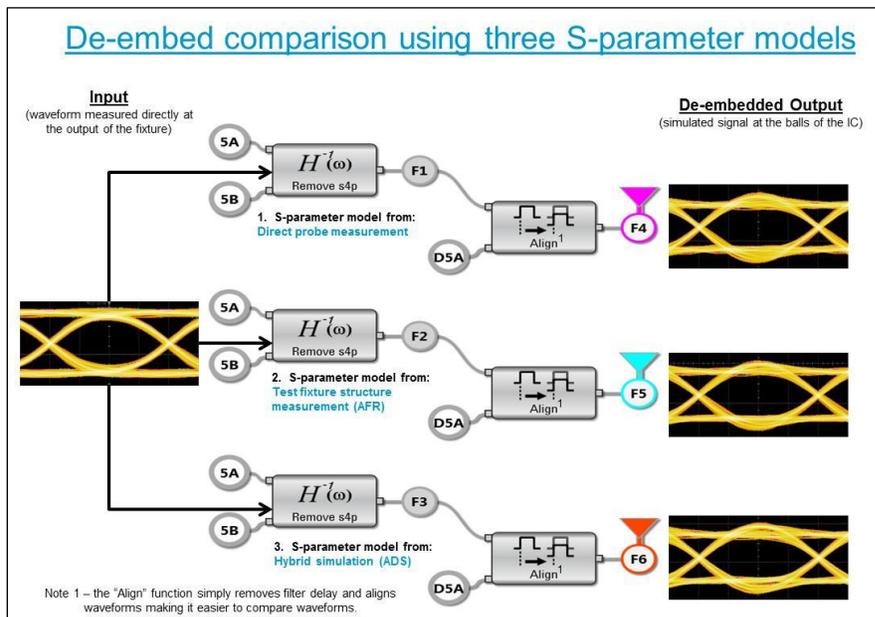
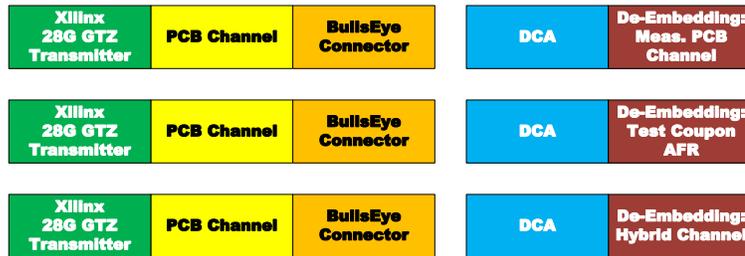


Figure 31 – Graphical representation of the signal processing setup used to compare the de-embedded signals (the same input signal is processed by three different S-parameter models)

The three lower eye diagrams (F4, F5, F6) displayed in Figure 32 all depict what the signal would look like at the balls of the device. Each signal was generated using a different S-parameter model, but as seen by the similarities in the eye diagrams and the results in Table 1, all three S-parameter models yield waveforms having very good correlation with one another. The de-embedded waveforms show that the signals at the balls included some emphasis to compensate for fixture losses. Additionally rise time and eye amplitude are also higher at the balls of the device, as expected.

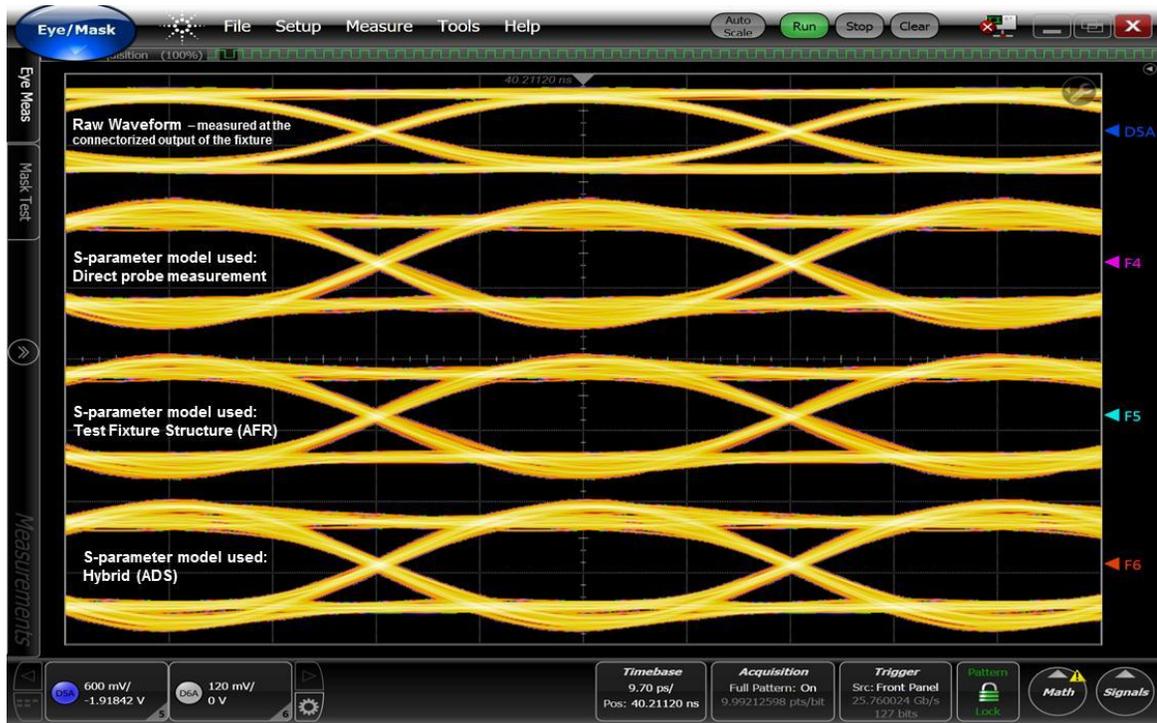


Figure 32: Direct DUT measurement at the output of the fixture (top) vs. de-embedded signals showing what the 25.78 Gb/s signal would look like at the balls of the device (three lower waveforms).

		S-Parameter Model Used by De-Embed Function		
FlexDCA Signal Identifier	D5A	F4	F5	F6
Description	Raw Differential Waveform	Direct Probe Measurement	Test Structure (AFR)	Hybrid (ADS)
Rise Time 20-80% (ps)	16.04	12.8	13.32	13.44
Eye Amplitude (mV)	587.5	822.5	813.5	833.0
Deterministic Jitter ($\delta - \delta$) (ps)	3.12	2.54	2.66	2.68

Table 1: Key parameters as measured directly out of the fixture (D5A) versus de-embedded signals simulated at the balls of the device (F4, F5, F6).

After removing the fixture effects through the use of de-embedding techniques, the 25.78 Gb/s signal at the balls of the device has the following (minimum) improvements in signal quality:

- Rise Time: 2.6 ps faster
- Eye Amplitude: 226 mV higher
- Deterministic Jitter (DJ): 440 fs lower.

Conclusion

The ability to measure the true 28 Gbps signal parameters at the device package pins can be quite challenging. PCB design, fixture path characterization, and instrument measurement capabilities all contribute to the success of predicting the true signal at the package pins. By systematically breaking down the data channel, the smaller components within can be optimized and characterized by both measurement and simulation to achieve a controlled impedance environment that propagates the highest of data rates.

Often the barrier to using advanced error correction techniques such as de-embedding is the cost in time and materials to develop the necessary calibration structures and the measurement of the channel fixture. The work in this paper has shown that 2x through AFR calibration structures can be used to achieve a very acceptable level of de-embedding quality. The keys to achieving a useful level of de-embedding include careful design, construction, and measurement of the calibration test fixture. A calibration test fixture can be designed that does not require an inordinate amount of board space and does not require the investment in micro-probing stations. Additionally, if the high speed fixture path is properly designed to avoid large impedance mismatches, partial S21 de-embedding provides very good results, eliminating the need to characterize the source using Hot TDR and accurately line up measurement reference planes to within picosecond accuracies for the cascaded elements in the model of the fixture path. High density applications that have 10's of channels with significant variations in path length (electrical delay) benefit from a hybrid measurement based model of the channel fixture so that the effect of path length variations can be simulated in a matter of seconds and reduce the board space required for fixture calibration structures.

In conclusion, utilizing the right combination of measurement and simulation techniques explored in this paper, it has been shown that the previously existing barriers for using de-embedding have been eliminated. Ultimately, this enables a breakthrough toolset which high speed design engineers can confidently use for evaluating the quality of their next generation of product designs.

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