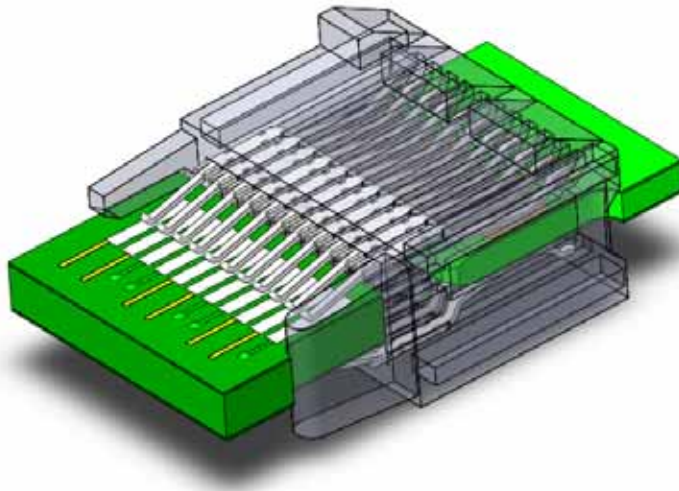




# Application Note

## **PCIE-EM Series Final Inch® Designs in PCI Express® Applications Generation 3 - 8.0 GT/s**



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**Series:** PCIe-EM

**Standard:** PCI Express®, Generation 3, 8 GT/s

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## **Abstract**

The PCI Express® is primarily intended as a high performance serial interface targeted for use in desktop, mobile, workstation, server, communications platforms, and embedded devices. As with any modern high speed PCB design, the performance of an actual PCI Express® interconnect is highly dependent on the implementation. Recent advances in technology have allowed PCI Express® designs to reliably reach 8.0 GT/s using common PCB materials and advanced Tx and Rx equalization techniques. This paper describes a statistical simulation compliance method applied to proven Samtec Final Inch™ designs. This application note is intended to help engineers deploy systems of two PCB cards mated through Samtec's family of high speed electrical connectors.

To demonstrate the feasibility of using Samtec's PCIE-Edge Mount (EM) card socket with standard FR4 epoxy PCBs, statistical simulations will be used to characterize the full Tx die-to-Rx die PCIE 8.0 GT/s channel, utilizing Samtec Final Inch® s-parameter modeling of the connector and complete interconnect channel, including all aggressor crosstalk impacts.

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## **Introduction**

Samtec has developed a full line of connector products that are designed to support serial speeds up to 8 GT/s, the maximum transfer rate of each PCI Express® data lane. Working with Teraspeed Consulting, they have developed a complete breakout and routing solution for each member of the Samtec line of high speed connectors, called Final Inch®. To demonstrate the feasibility of using Samtec PCIe-EM connectors in PCI Express® applications with standard FR4 epoxy PCBs, full s-parameter modeling of the channel, along with statistical simulation techniques, will be used to sweep various trace lengths across the design space to show a final compliance region.

## **The PCI Express® Specification**

PCI Express® 8.0 GT/s links are based on recent advances in signal processing technology using advanced Tx and Rx equalization. A PCI Express® link is comprised of a dual-simplex communications channel between two components physically consisting of two low-voltage, differential signal pairs. The PCI Express® Base Specification defines one half of a link (one transmitter and receiver) as an electrical sub-block. The design model used for this paper is of three electrical sub-blocks operating in tandem, one the victim surrounded by 2 aggressors, with all bit streams heading in the same direction.

Detailed specifications for an electrical sub-block can be found starting in Section 4.3 of the PCI Express® Base Specification and will be referred to throughout the rest of this paper. Detailed channel specifications start in Sub-section 4.3.6. Channel compliance testing requirements of subsection 4.3.6.4 for 8.0 GT/s were adhered to for these simulations. See PCI Express® Base Specification Revision 3.0 for more details.

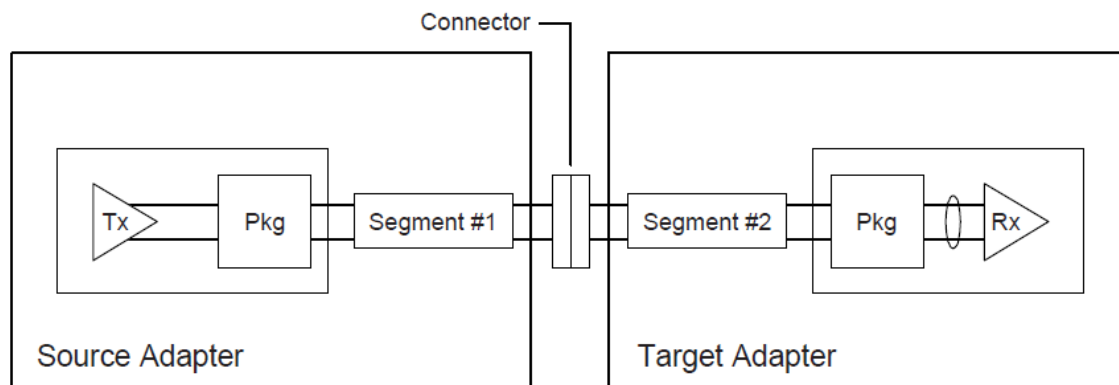
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### ***The Simulation Model***

Figure 1 shows the mated Samtec PCIe-EM card socket used in a typical multi-segment channel with a source adapter residing on a motherboard and a target adapter residing on an add-in card. The test circuit is modeled as:

- Agilent's Advanced Design System Tx and Rx modules that correlate to the Tx and Rx package models released by the PCI Special Interest Group, and defined in Section 4.3.6 - Channel Specification - of the PCI Express® Base Specification, Rev 3.0.
- A variable length interconnect trace segment on the source adapter, with and without a 200 nF capacitor
- A variable length interconnect trace segment on the target adapter.
- A mated Samtec PCIe-EM connector touchstone s-parameter model.



**Figure 1 - PCI Express® 8.0 GT/s Test Configuration**

Segment topology of the source and target adapters were swept in multiple ways to determine the limits of compliant channel operation, and whether any sensitivity exists.

1. All combinations of 0.1" to 1" in steps of 0.1" for both the source and target adapter.
2. Source length = target length swept from 1" to 20" to determine the entire reliable operation limit of the channel.
3. Source length swept from 1" to 30" with the target length set at 4", which is the typical maximum length for PCIe add-in cards.

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For sweep configuration #3 additional simulations were performed with the addition of 200 nF DC blocking capacitors, to model additional signal quality degradation.

All traces were modeled as microstrip on FR4 with the following parameters:

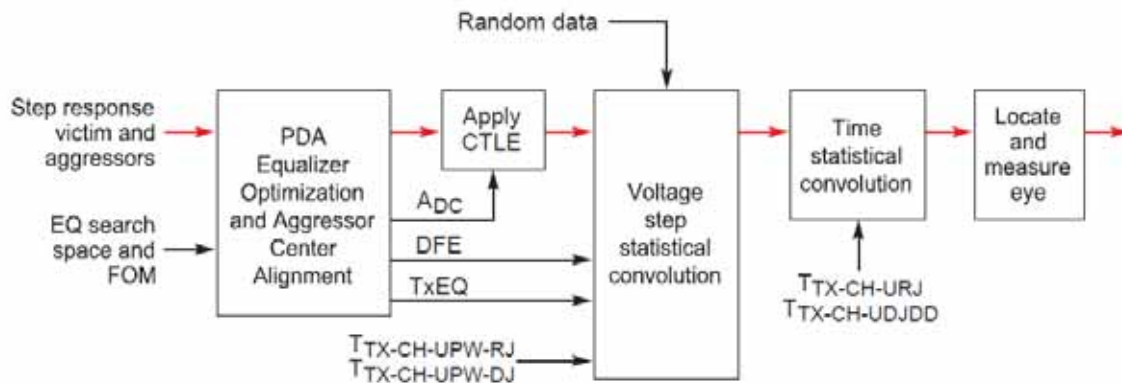
- FR4 is modeled using a Svensson/Djordjevic causal model that has a broadband response that is faithful to measured results from DC to greater than 20 GHz, using the following parameters:
  - $\epsilon_r = 4.2 @ 1 \text{ GHz}$
  - Loss Tangent = 0.02 @ 1 GHz
- Copper is modeled as follows to reflect the reduced conductivity of copper foil used in PCB fabrication:
  - Conductivity =  $4.5E+7 \text{ S-m}$
  - Surface roughness = 0.6 micron
- Traces are differential microstrip with the following geometry:
  - 100 ohm differential impedance
  - 4.2 mil trace width
  - 2 mil trace copper thickness
  - 5.75 mil center-to-center spacing
  - 4.4 mil FR4 dielectric thickness
  - No differential coupling to neighboring differential channels

Using other trace geometries or materials will lead to different results than shown here. However, if reasonable care is made to stay well within the design space and guidelines provided in this document, it is possible to build robust PCIE 8.0 GT/s channels with limited additional simulation verification.

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## The Simulation Environment

The PCI Express® Base specification requires that 8.0 GT/s channel compliance be performed utilizing a die-to-die interconnect model, including the Tx and Rx packages. "The model shall include both victim and a sufficient number of aggressor paths to accurately capture the channel crosstalk effects. Using the Tx voltage and jitter limits defined in the transmitter specification ... it is possible to transform these parameters to what would appear at the die pad of a Tx" [sic]. As shown in Figure 2, the output of the simulation is actually the eye as it appears at the input of the Rx sample latch.



**Figure 2 - PCI Express® 8.0 GT/s Flow Diagram for Channel Tolerance**

The PCI Special Interest Group (SIG) provides an open source statistical eye simulator (seasim v0.46) that may be used to implement the following necessary simulation and modeling requirements:

- Channel characteristics defined as s-parameters.
- Behavioral Tx and Rx package models.
- Transmitter jitter and voltage.
- Transmitter and receiver termination impedance of 2 x 50 ohm.
- Time domain representation of the end-to-end connectivity.
- Behavioral Tx equalization.
- Behavioral Rx continuous time linear equalizer (CTLE).
- Behavioral Rx digital feedback equalizer (DFE).
- Optimization of Tx equalization and Rx DFE/CTLE settings.
- Statistical treatment of jitter.
- Statistically defined output eye width and eye height.

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For this application note, Agilent's Advanced Designed System 2011.10 (ADS2011) software simulation tool is used to accomplish the simulation tasks. Templates were developed within ADS to automate the analysis so that channel components can be easily replaced. The results from SEASIM and ADS are the same provided the same source jitter and equalization settings are used. The ADS templates require the following channel definitions:

- Definition of input S-parameter files to be used in the simulations.
  - Samtec PCIE-EM mated connector
  - PCIE3 Tx and Rx package models
- Definition of Tx segment 1 and Rx segment 2 trace lengths to be simulated.
- Iterative processing of all trace length cases using the ADS2011 batch simulation mode.
- FR4 Microstrip Differential Trace
- 200 nF capacitor

### ***Compliance Eye Mask***

Figure 3 shows the 8.0 GT/s channel compliance eye mask. The ADS2011 channel simulator and Samtec modeling provide all necessary inputs required to generate the statistical eye necessary to test against the eye mask pass/fail requirements. Although the specification allows for a minimum measured eye height of 25 mV P-P, we will de-rate the specification to 50 mV P-P for the purposes of this study, to provide a guard band for "the things that keep engineers awake at night." Or at least the things that keep this author awake. This guard band should be sufficient to provide designers using this document additional confidence.



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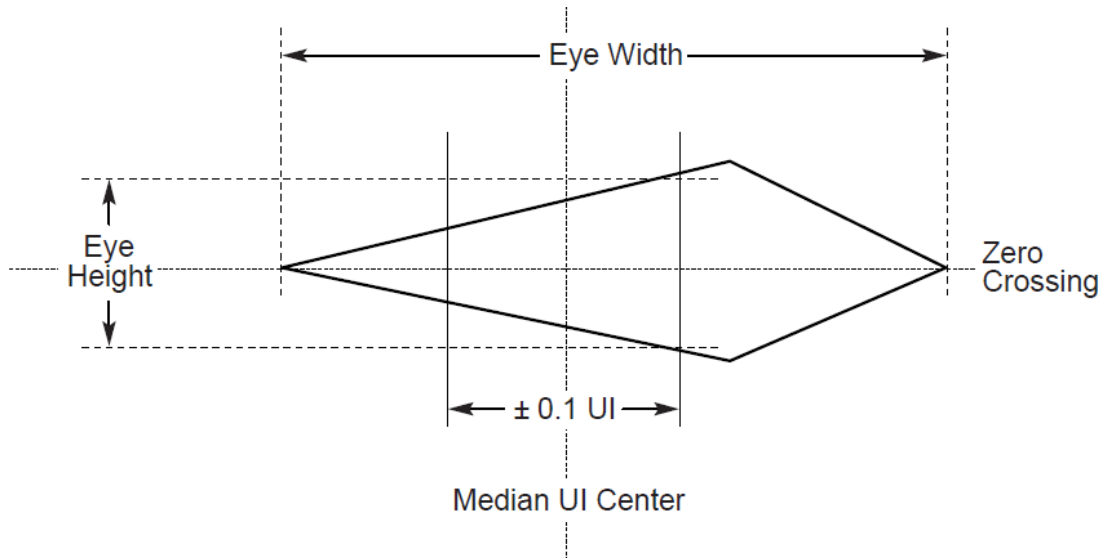


Table 4-27: Channel Tolerancing Eye Mask Values

Symbol	Parameter	Value	Units	Comments
$V_{RX-CH-EH}$	Eye height	25 (min)	mVPP	Eye height at BER=10 <sup>-12</sup> . Note 1.
$T_{RX-CH-EW}$	Eye width at zero crossing	0.3 (min)	UI	Eye width at BER=10 <sup>-12</sup>
$T_{RX-DS-OFFSET}$	Peak EH offset from UI center	±0.1	UI	See Figure 4-87 for details.
$V_{RX-DFE\_COEFF}$	Range for DFE $d_1$ coefficient	±30	mV	See Figure 4-70 for details.

Figure 3 - 8.0 GT/s Channel Tolerance Eye Mask and Values

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## ***Compliance Measurements***

To obtain a feel for the overall range of operation of PCI Express® 8.0 GT/s channels simulation models were created with equal length Tx and Rx trace segments without DC blocking capacitors, swept from 1" to 20", for a total channel length from 2" to 40". Figure 4 displays a graph of the measured inner eye height for each simulated length. This simulation includes all channel, jitter, and crosstalk effects. Our chosen compliance limit of 50 mV P-P is shown on the chart as a red line. With the trace models and material parameters that we are using, a total channel reach of 23" is possible. Longer channels will have higher loss, with lower eye openings; however, we generally do not advise using longer channels without detailed channel modeling.

Figure 5 displays a graph of the measured inner eye width for the same simulation deck as Figure 4. The 0.3 UI eye width compliance limit is shown as a red line on the chart. Clearly there is sufficient jitter margin at any of our simulated channel lengths. This is typical for well-behaved, resonance free interconnect systems, which are generally not jitter limited, and are limited by the received signal amplitude.

The simulated eye for 23" of interconnect (11.5" Tx board trace and 11.5" Rx board trace) is shown in Figure 6. For these statistical simulations the eye boundary is defined for a statistical confidence interval with a bit error rate (BER) of  $10^{-12}$ , as required by the PCI Express® specification. An inner eye opening of 52 mV was measured by the simulator; this is just above our established compliance limit for this study. The measured inner eye width of 0.50 UI is well above our 0.3 UI limit. By providing 25 mV of additional amplitude margin over the specified 25 mV limit, we provide a guard against additional issues that may be unforeseen by the designer. The impact of adding 200 nF DC blocking capacitors to this same model is shown in Figure 7. For these long reach PCI Express® channels, the impact of a well-designed blocking capacitor pad pattern is essentially negligible, due to the dominance of dielectric and conductor losses.

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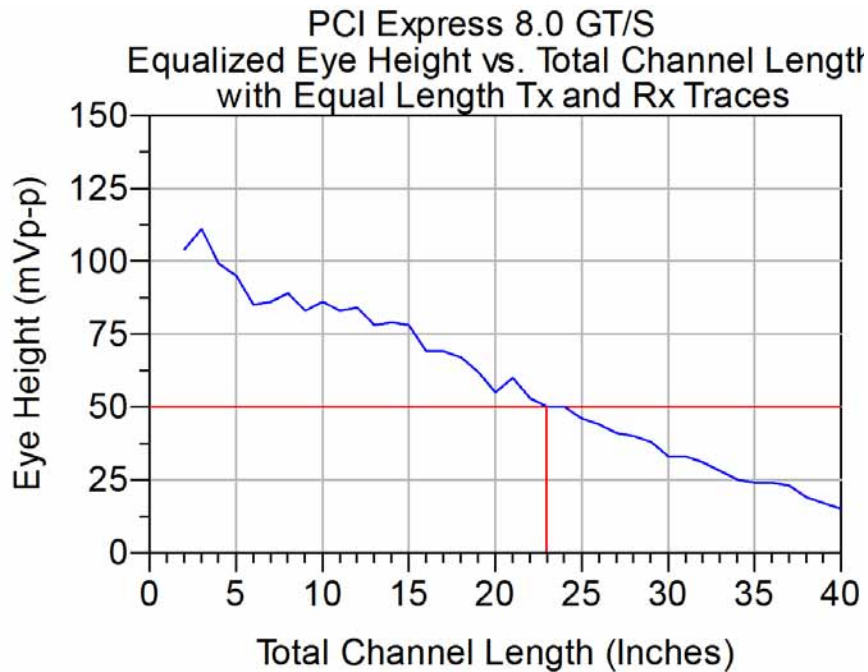


Figure 4 - 8.0 GT/s Eye Height vs. Length

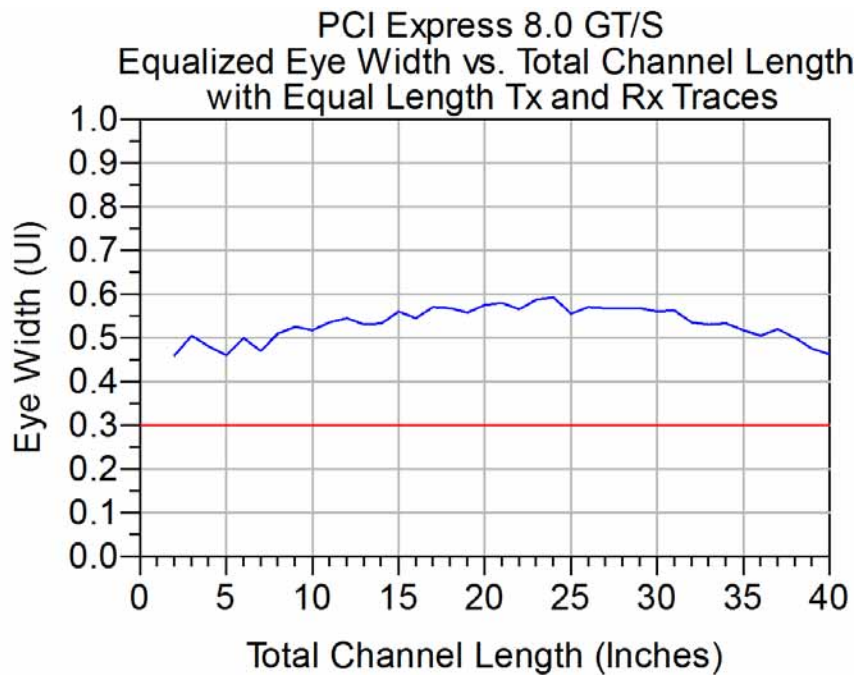
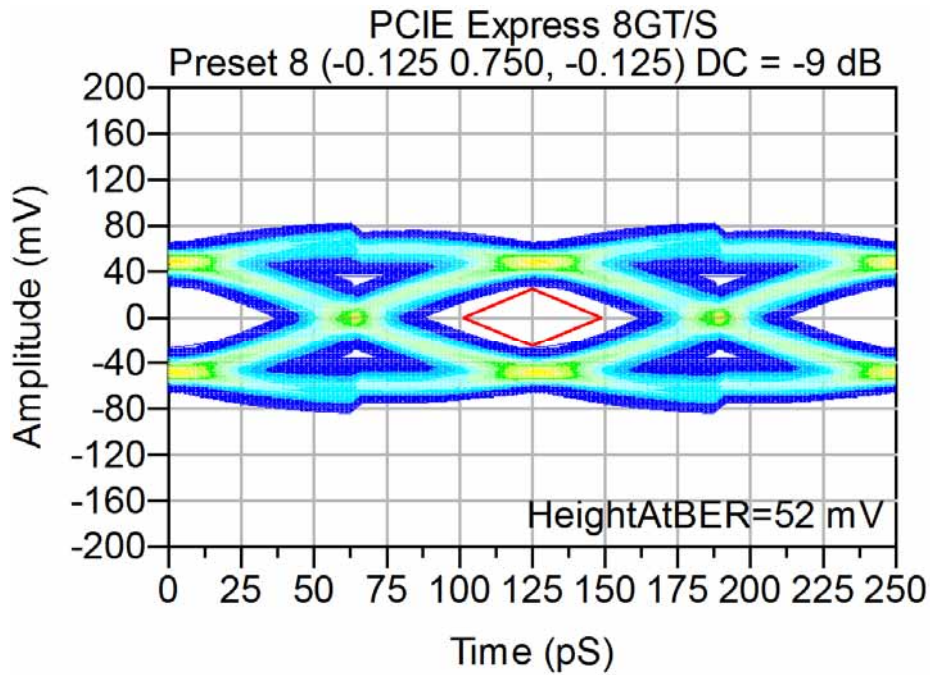
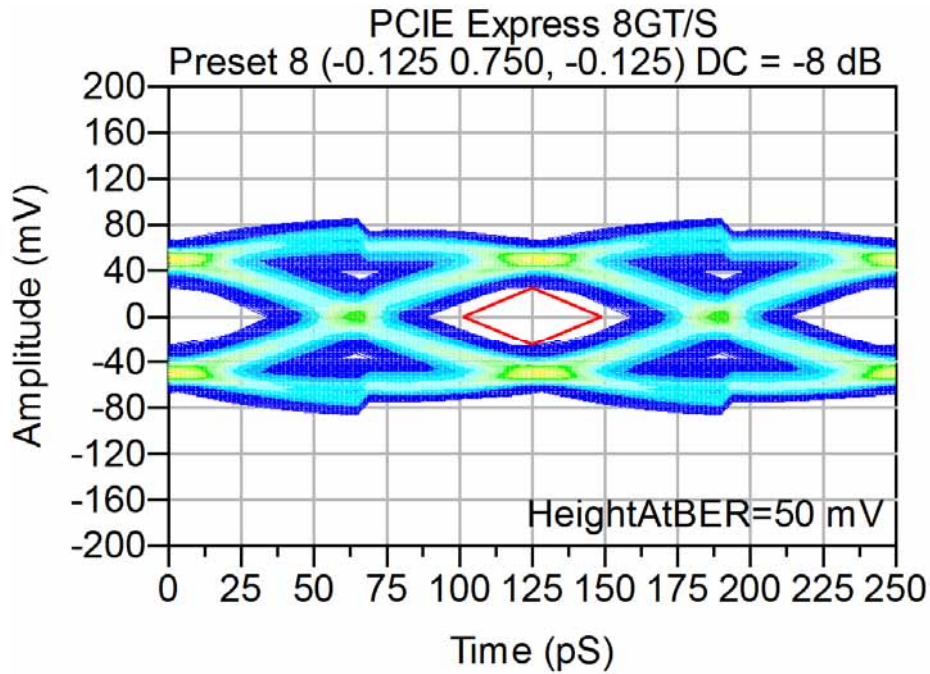


Figure 5 - 8.0 GT/s Eye Width vs. Length

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**Figure 6 - System 8.0 GT/s Eye**  
(11.5" Tx board trace, 11.5" Rx board trace)

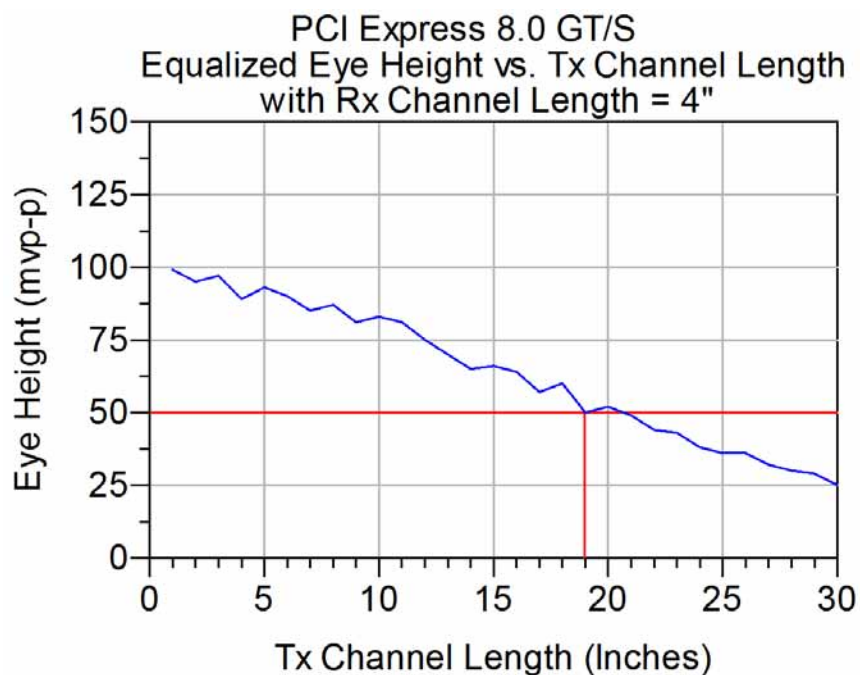


**Figure 7 - System 8.0 GT/s Eye**  
(11.5" Tx board trace, 11.5" Rx board trace, with 200 nF DC blocking Capacitor)

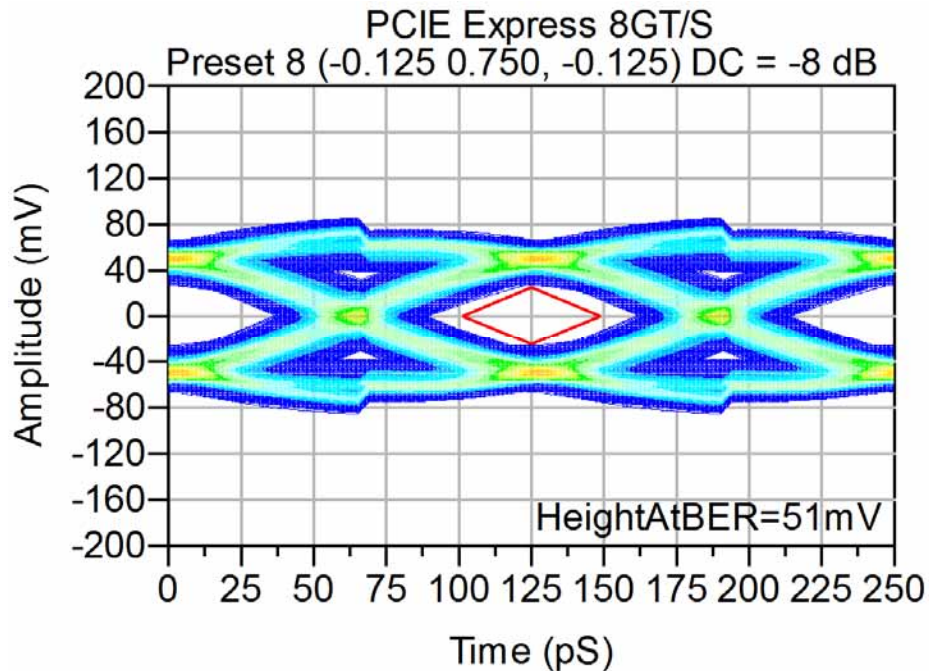
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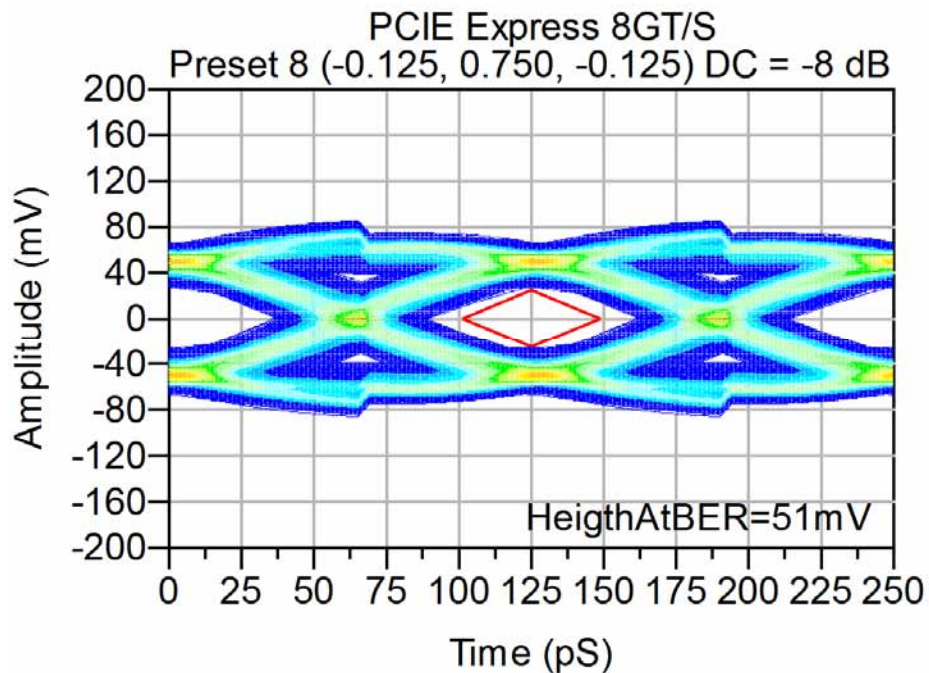
If we set the length of the Rx adapter to 4", the maximum length for a standard PCI Express® 8.0 GT/s add-in card, we can now sweep the Tx adapter (motherboard) trace length from 1" to 30" and view the results. Figure 8 shows a plot of the measured eye height vs. Tx trace length, resulting in Tx length limits of 19". Figures 9 and 10 show the representative eyes for the 23" channels, with and without DC blocking capacitors. As seen previously, addition of the capacitor has a negligible impact on these long reach channels.



**Figure 8 - 8.0 GT/s Eye Height vs. Tx Length  
with Rx Length = 4"**

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**Figure 9 - 8.0 GT/s Eye**  
(19.0" Tx board trace, 4" Rx board trace)



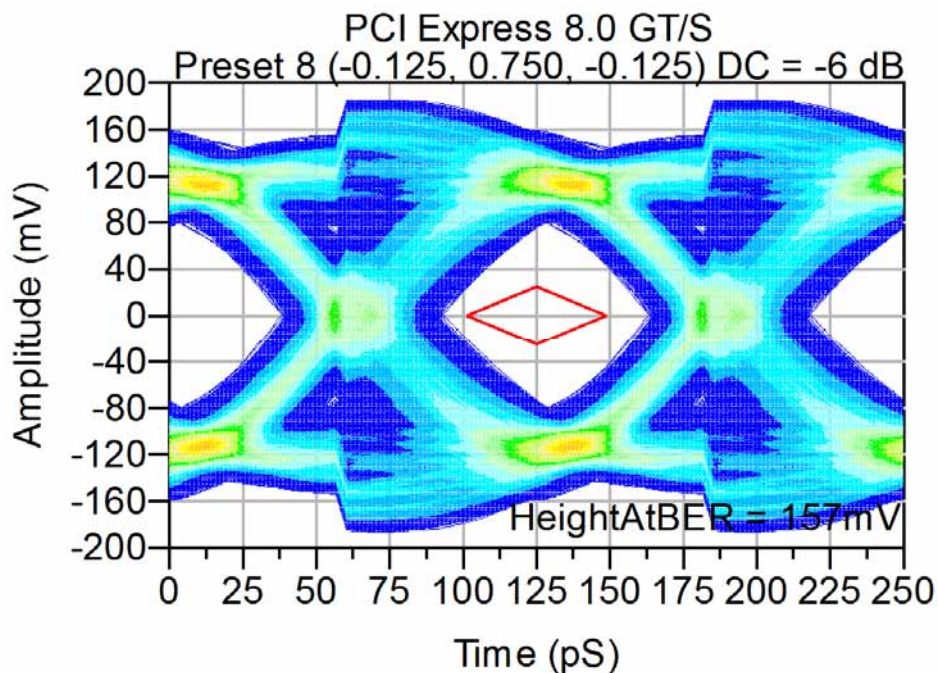
**Figure 10 - 8.0 GT/s Eye**  
(19.0" Tx board trace, 4" Rx board trace, with 200 nF DC blocking Capacitor)



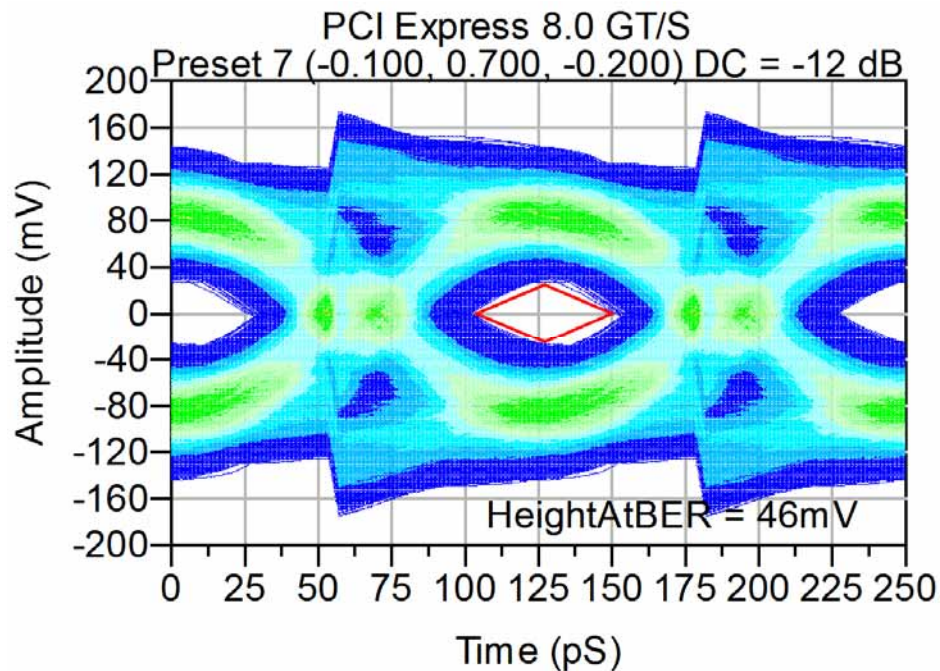
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Simulation sweeps with all combinations of extremely short trace segments from 0.1" to 1" were used to characterize the potential for amplitude and jitter degradation of the Tx package, Rx package and connector combination, providing a view of potential short channel low loss resonance issues. Figure 11 shows the best case short channel eye opening with a 1.0" Tx and 0.1" Rx trace length. While Figure 12 shows the worst case short channel eye opening when the Tx trace length is 0.7" and the Rx trace length is 0.6". In both cases, the equalized eye is well within compliance margins, with no serious resonance peaking issues that are beyond the capabilities of PCI Express® 8.0 GT/s equalizers.



**Figure 11 - 8.0 GT/s Eye**  
(1.0" Tx board trace, 0.1" Rx board trace)

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**Figure 12 - 8.0 GT/s Eye**  
(0.7" Tx board trace, 0.6" Rx board trace)

If we use an 85 ohm system impedance and set the length of the Rx adapter to 4", the maximum length for a standard PCI Express® 8.0 GT/s add-in card, we can now sweep the Tx adapter (motherboard) trace length from 1" to 30" and view the results. Figure 13 shows a plot of the measured eye height vs. Tx trace length, resulting in a Tx length limit of 22.5" for our study. Figure 14 shows the representative eye for this 26.5" channel with a DC blocking capacitor. Margin for an 85 ohm PCI Express® interconnect is slightly larger than that for the 100 ohm system, due to the lower loss of the 85 ohm traces using the same dielectric thickness of the 100 ohm system.



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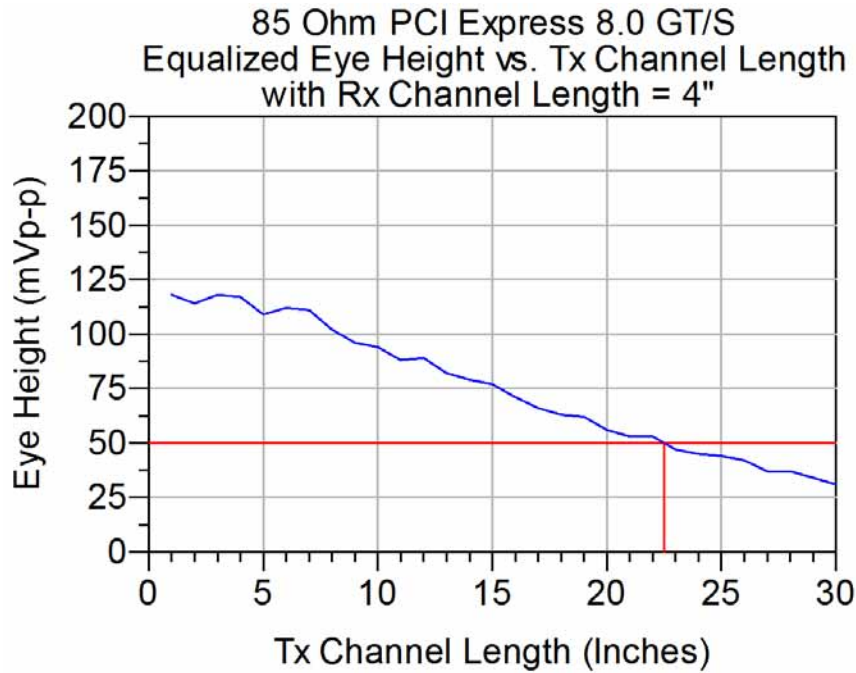


Figure 13 - 85 Ohm System 8.0 GT/s Eye Height vs. Tx Length with Rx Length = 4"

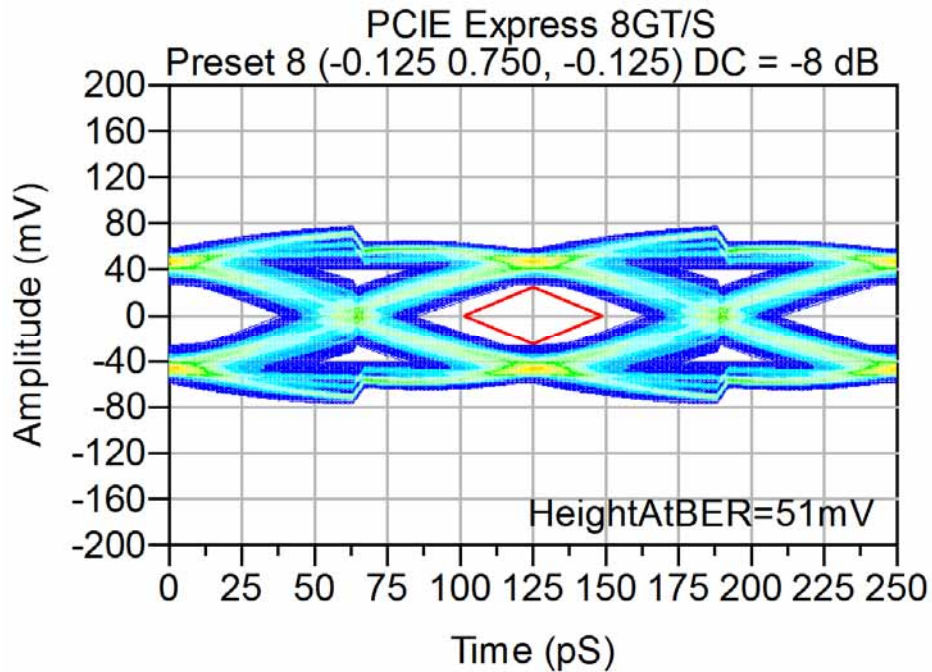


Figure 14 - 85 Ohm System 8.0 GT/s Eye (22.5" Tx board trace, 4" Rx board trace, with 200 nF DC blocking Capacitor)

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## ***Conclusions***

A single Samtec PCIe-EM connector in a board-to-board configuration can be used in 100 ohm PCI Express® 8.0 GT/s systems with total trace lengths not to exceed 23 total inches when used with Samtec's Final Inch® routing, breakout, and trace width solutions as modeled and simulated in this document. 85 ohm systems have slightly higher margins and subsequently a longer reach of 26.5 inches of total interconnect length.

Because loss is the dominant contributor to system degradation, designers should be aware that using smaller trace widths, laminates with higher loss tangent, sub optimal routing solutions with higher pair-to-pair coupling, and additional vias will decrease overall performance and the maximum allowable trace length. It is advisable, when designing systems that approach the maximum trace length limits, to perform detailed modeling, simulation, and measurement of the target design including the effects of material properties, traces, vias, and additional components.