WHITE PAPER

ARM

RealView® Hardware Platforms Product Selector

Javier Orensanz October 2007

This document is intended to help you select the RealView Hardware Platforms appropriate for your needs.

The first section shows the different implementations of ARM processors on our boards, and their relative advantages and disadvantages. The document then covers typical combinations of boards that work together out of the box, and other combinations of boards which require you to update the FPGA designs before running any software.

Finally, the document explores the memory and peripherals available in different boards.

Before making a decision it is advisable to look at the RealView Obsolescence Note on the ARM website, as some of the RealView Hardware Platforms mentioned in this document may be retired soon. The Obsolescence Note can be downloaded from www.arm.com/miscPDFs/8757.pdf.

IMPLEMENTATIONS OF ARM PROCESSORS IN REALVIEW HARDWARE PLATFORMS

RealView Hardware Platforms are often the only way developers can get hold of ARM silicon with an AMBA bus for prototyping hardware. ARM processors can be found on our boards in 'test chips', 'development chips', 'soft macrocell models' and 'FPGA validation systems'.

Note that these devices are not normally sold on their own, but only as part of development boards.

Test chips

ARM and ARM partners manufacture silicon in small quantities to validate new processor designs or silicon processes. Test chips contain an ARM processor plus a minimum amount of logic required to validate it, such as clock management (PLL and clock dividers) and boundary scan test logic.

In order to reduce the pin count of the device, test chips sometimes do not provide access to all the interface signals of the processor. For example, processors with multiple AMBA interfaces (e.g. ARM926EJ-S, ARM1136JF-S) have their interfaces multiplexed into a single external AHB bus. Also, the coprocessor, ETM and TCM interfaces are not normally bonded out to the test chip pins.

Test chips impose few constraints on the system architecture and memory map, and provide access to an ARM processor running at a speed close to that of an ASIC. When using boards based on test chips, the memory system is normally implemented in FPGAs. This approach gives you flexibility in the implementation of the design, but introduces a performance bottleneck in the memory system, which affects the speed of the overall system.

Test chips are found in Core Tiles.

Development chips

A development chip is a complete system on chip that contains all the performance-critical components of a typical system: ARM processor, coprocessors, ETM, LCD controller and memory controller. What makes a development chip special, compared with a standard ASIC or ASSP, is that it has standard AMBA interfaces (AHB or AXI), which allow you to extend the system with your own AMBA compatible peripherals. These peripherals are normally implemented in FPGAs.

Typically, most of the bus transactions happening in the system are between the processor and memory or between the LCD controller and memory. Since these three devices are integrated inside an ASIC, they and their interfaces can be clocked at high frequencies, which usually results in a faster overall system than that based on a test chip.

Development chips can be found on Platform Baseboards and Application Baseboards.

Because of the lack of development chips for some ARM applications processors such as ARM11 MPCore and Cortex-A8, their Platform Baseboards implement a 'test chip + northbridge' architecture, in which the processor is implemented on a test chip and the performance critical components of the memory system on a 'northbridge' structured ASIC. The performance achieved by these two devices together is similar to that of a development chip.

Soft Macrocell Models

A Soft Macrocell Model (SMM) is an implementation of an ARM processor in an FPGA, normally the FPGA on one of our Logic Tile boards.

For ARM9 and ARM11 processors the SMM is the only solution that gives you access to all the pins of an ARM macrocell and is ideal for 100% cycle accurate hardware prototyping. For Cortex processors the SMM has limited availability of the processor pins so that its pinout is compatible with a Core Tile and the same baseboard can be used for both boards.

SMMs provide early availability of new processors, since they are released straight after the processor RTL is frozen, which happens months or years before test chips or development chips are manufactured. Finally, SMMs provide access to specific revisions of ARM processors not available on test chips or development chips.

The disadvantage of SMMs is that they only achieve frequencies of about 15 to 20MHz. This is much faster than a hardware emulation box but much slower than test chips and development chips.

FPGA Validation Systems

FPGA validation systems are the first implementations of ARM CPUs on one or more RealView Logic Tiles.

FPGA validation systems are intended for internal validation, benchmarking and early access to lead silicon, OS and tools partners only. They are slow and only partially documented, therefore not suitable for general availability.

Intended use of Core Tiles, Platform Baseboards, SMMs and FPGA Validation Systems

Deciding which platform to choose is not complex if you apply the following rules:

- When speed is required, the best solution is a Platform Baseboard based on a development chip or 'test chip + Northbridge'. These boards are ideal for software development and for prototyping of new AMBA peripherals
- An SMM is the best option for early access to processors, prototyping a complete system on chip, and for cycle accurate benchmarking

- A Core Tile based on a test chip is a compromise between the other two solutions. It achieves speeds much greater than an SMM and provides access to most pins of the processor
- FPGA validation systems are the only option for early access to new processors

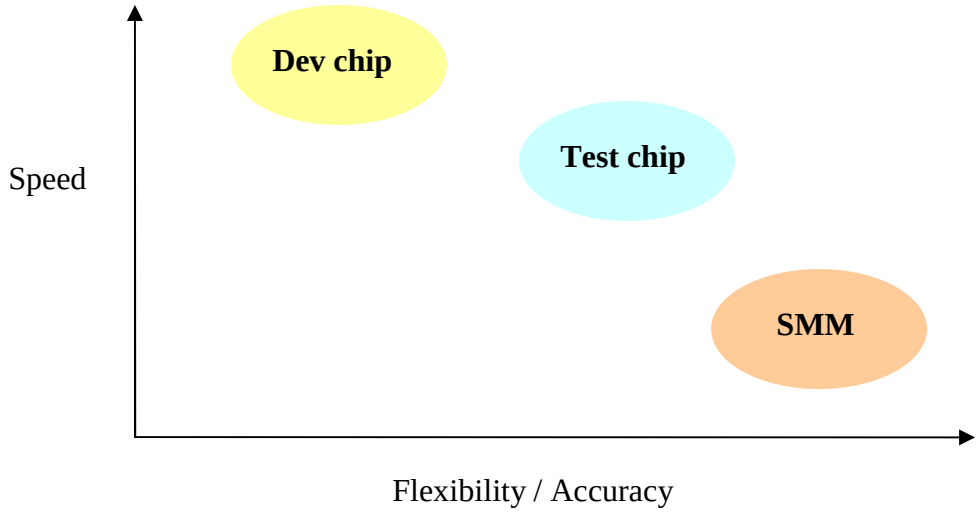


Figure 1: Comparison of test chip, development chip and SMM

Which board should I choose if I base my decision on the processor?

Table 1 shows the availability of processors on different development boards.

In some cases it is a requirement that the board chosen contains the processor that will be used in the final ASIC. In that case the number of options is greatly reduced.

In other cases this requirement is not so important. The main reason for this is the software compatibility between processors. For example, the ARM7TDMI, ARM720T and ARM740T are based on the same integer core. Also, the ARM architecture is backwards compatible, so software written for the ARM7TDMI can run on an ARM926EJ-S or an ARM1136JF-S. Finally, the interfaces of two processors of the same family are in some cases identical (e.g. ARM920T and ARM922T) or very similar (e.g. ARM946E-S and ARM966E-S).

Sometimes the processor required is not available on RealView hardware platforms or it is more advantageous to use a development board with a different processor (for example this happens when the speed or the cost of the system is critical).

	Core Tile	Platform Baseboard	Application Baseboard	SMM	FPGA Validation System
ARM7TDMI	✓				
ARM720T					
ARM740T					
ARM920T					
ARM922T					
ARM926EJ-S	✓	✓	✓	✓	
ARM940T					
ARM946E-S				✓	
ARM966E-S				✓	
ARM968E-S				✓	
ARM1020E					
ARM1022E					
ARM1026EJ-S				✓	
ARM1136J(F)-S	✓			✓	
ARM1156T2(F)-S	✓			✓	
ARM1176JZ(F)-S	✓	Dec 07		✓	
ARM11 MPCore	✓	Nov 07			
Cortex-A8		Planned		Q1 08	✓
Cortex-R4F	Planned			✓	
Cortex-M3					✓
Cortex-A9		Planned			Q4 07

Table 1: Availability of processors on different platforms

TYPICAL SYSTEMS BASED ON REALVIEW HARDWARE PLATFORMS

RealView hardware platforms provide a complete out-of-the-box solution. As well as ARM processors they also include memory, peripherals and FPGAs to prototype your own peripherals.

Below is a list of supported platforms or bundles of boards. ARM provides example FPGA RTL and bit files as well as example software for these supported configurations so that you can start to run code or prototype your system straight away.

Application Baseboard for ARM926EJ-S (AB926EJ-S)

This is a software development board based on the ARM926EJ-S development chip. This board contains memory and enough peripherals to run an operating system.

Extra peripherals can be added with the AB-IB1 and AB-IB2 interface boards.

Figure 2: AB-IB2 on top of AB926EJ-S

Platform Baseboard for ARM926EJ-S (PB926EJ-S)

This is a hardware and software development board based on the ARM926EJ-S development chip. This board contains all the peripherals available on the Application Baseboard for ARM926EJ-S plus additional peripherals.

The main difference between these two boards is that the Platform Baseboard can be extended with custom AHB peripherals implemented in the FPGA on Logic Tiles. In this case, an Analyzer Tile can be used to measure signals between the baseboard and the Logic Tile.

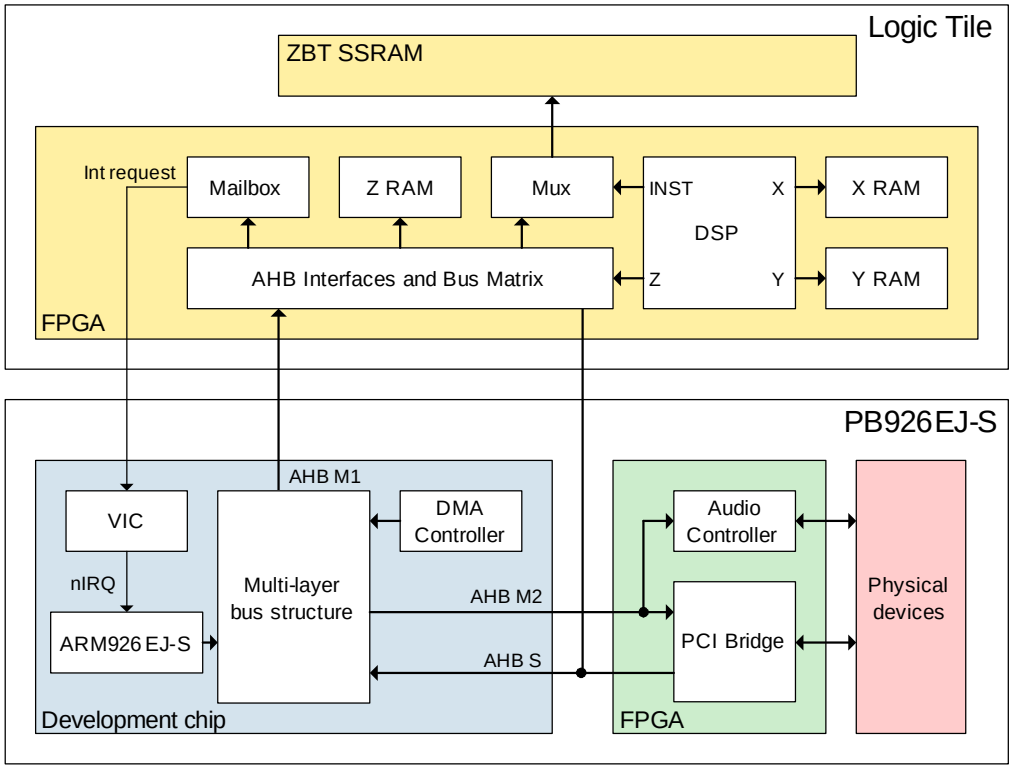


Figure 3: Example application - PB926EJ-S + DSP on Logic Tile

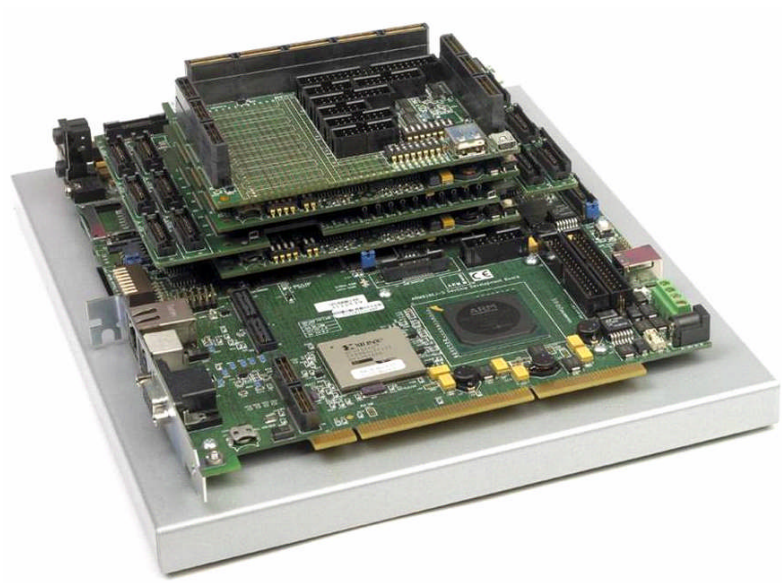


Figure 4: PB926EJ-S with two Logic Tiles, Analyzer Tile and Interface Tile

Extra ARM7TDMI, ARM926EJ-S and ARM1136JF-S processors can be added to the PB926EJ-S using Core Tiles. Each additional processor requires one Core Tile and one Virtex-II Logic Tile. The Logic Tile is required to interface the signals from the test chip on the Core Tile to the AHB system buses.

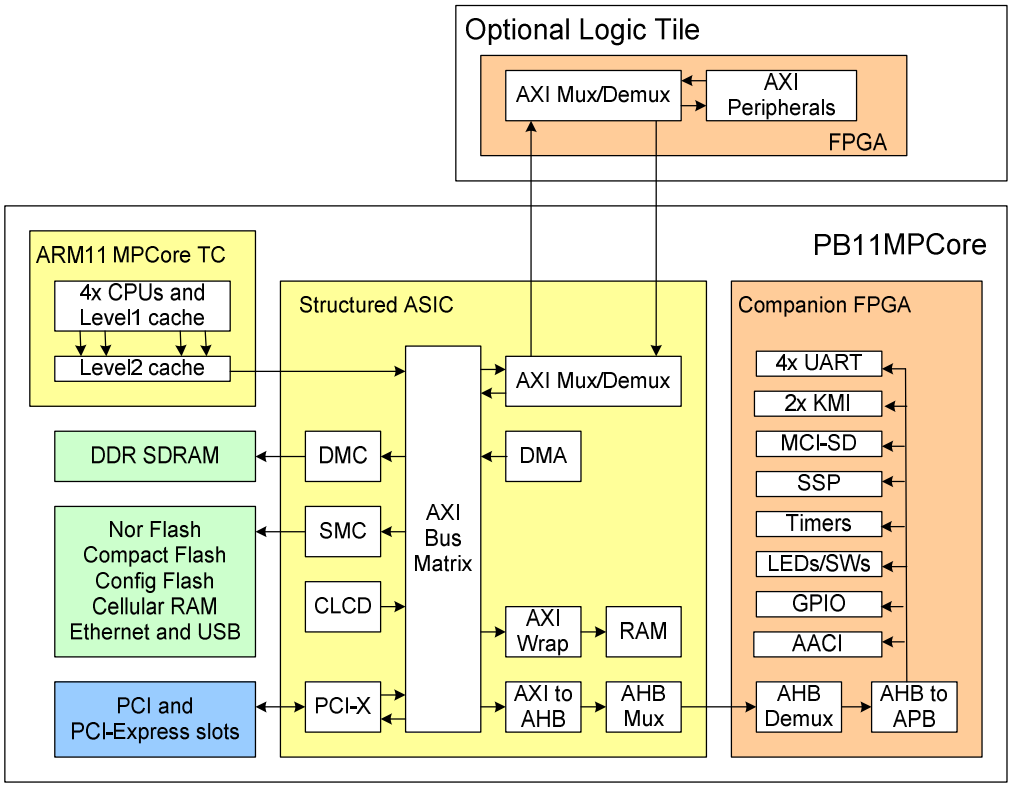
Finally, an Interface Tile on top of a Logic Tile can be used to provide additional peripherals for automotive or industrial applications as well as test connectors and a prototyping grid.

A PCI kit and a 2.2" Color LCD kit interface directly with the PB926EJ-S.

Platform Baseboard for ARM11 MPCore (PB11MPCore)

PB11MPCore is a software and hardware development platform based on the ARM11 MPCore multiprocessor. The Platform Baseboard is designed for Symmetric Multi-Processing (SMP) software development at near real time. In addition to the rich set of peripherals found in the Platform Baseboard for ARM926EJ-S, PB11MPCore has a Compact Flash and PCI-Express slots.

Logic Tiles for Virtex-II, Virtex-4 and Virtex-5 FPGAs can be stacked on top of the PB11MPCore to provide FPGA space to integrate custom AXI or legacy AHB peripherals to the ARM11 MPCore system.

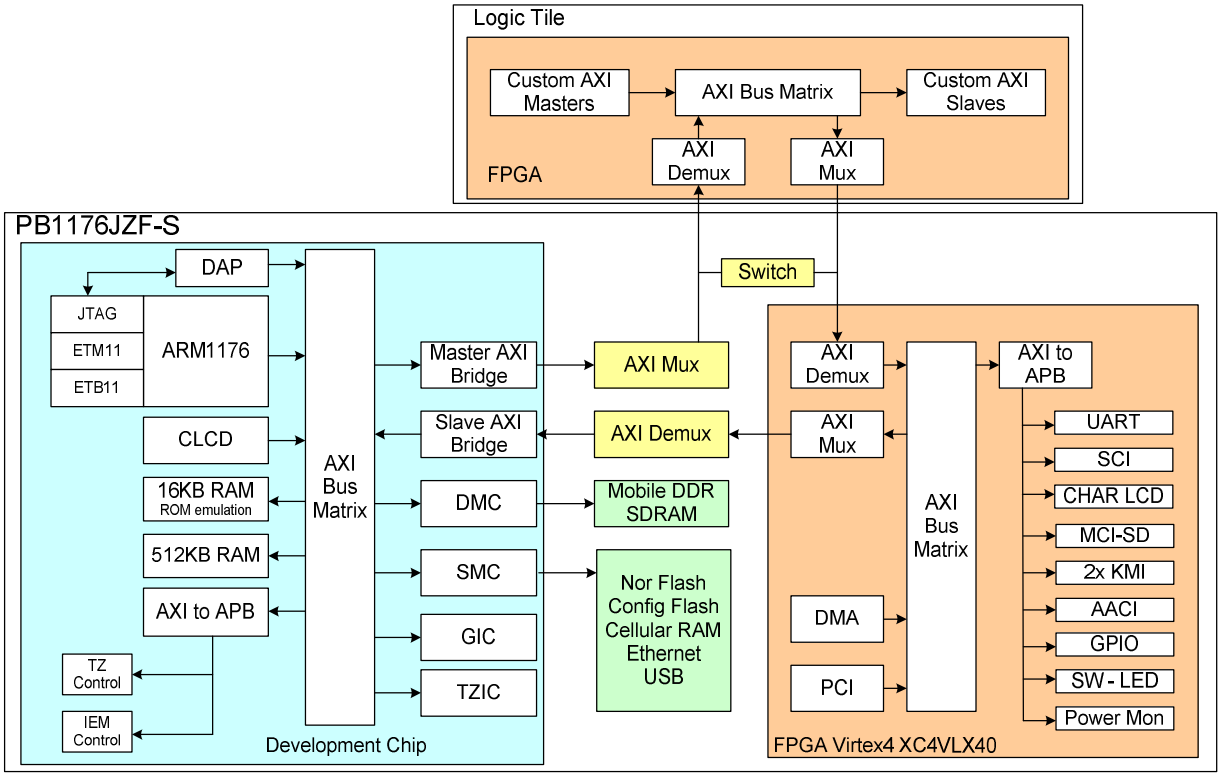


Platform Baseboard for ARM1176JZF-S (PB1176JZF-S)

The Platform Baseboard is a software and hardware development platform based on the ARM1176JZF-S processor. PB1176JZF-S is the reference platform for security critical software applications development using TrustZone technology from ARM.

The development chip features the Intelligent Energy Management technology from ARM so as to enable optimized balanced CPU workload energy consumption applications development.

Logic Tiles for Virtex-II, Virtex-4 and Virtex-5 FPGAs can be stacked on top of the PB1176JZF-S to provide FPGA space to integrate custom AXI or legacy AHB peripherals to the ARM1176JZF-S system.



Core Tile (CT), Cortex SMMs or SMM968E-S on the Emulation Baseboard (EB)

Test chips for the latest ARM processors are fitted on Core Tiles. A Core Tile cannot be used standalone but requires a baseboard implementing a memory system for the processor. Core Tiles are normally used on top of the Emulation Baseboard, which provides memory, peripherals and an FPGA with the bus infrastructure and peripheral controllers. The EB has a large FPGA (Xilinx Virtex2 XC2V6000) which can also be used to prototype your own peripherals. If the size of this FPGA is not enough, Logic Tiles can be added on the second tile site of the EB.

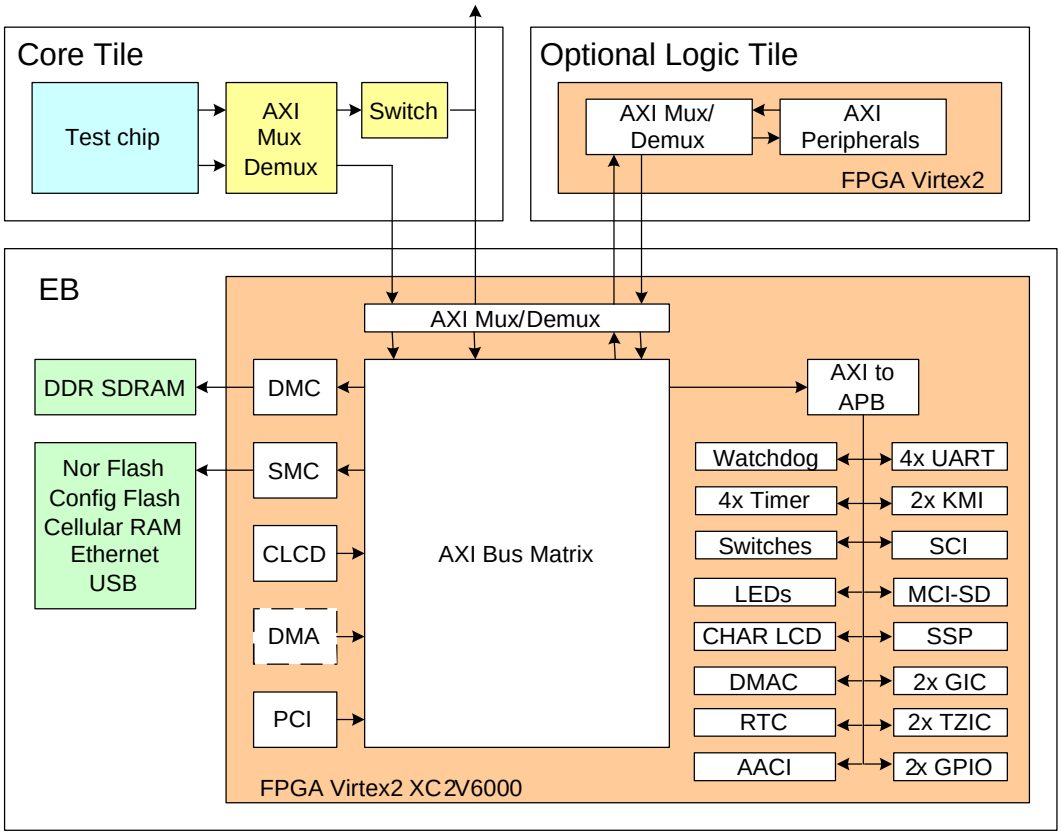


Figure 5: AXI-based system consisting of Core Tile, EB and Logic Tile

EB FPGA images and RTL that implements and AHB system are provided for CT7TDMI, CT926EJ-S and CT1136JF-S. An example AXI system is provided for AXI-based Core Tiles such as CT11MPCore, CT1156T2F-S and CT1176JZF-S.

New Soft Macrocell Models for ARM968E-S and Cortex processors such as R4 and A8 are pin compatible with Core Tiles and example FPGA images supporting them are also provided for the Emulation Baseboard. The SMM on EB is a good system for early software and hardware prototyping, which can be upgraded with Core Tiles or Platform Baseboards as they become available.

The CT926EJ-S is capable of performing early bus termination on its AHB interface. This prevents it from working correctly when connected with a standard AHB-AXI bridge to some AXI peripherals, such as the PL340 dynamic memory controller. The current workaround is to split all burst accesses from the CPU into single accesses, which greatly reduces the maximum performance of the system. If you require high performance, you should use a PB926EJ-S instead.

Similarly, the bus infrastructure inside the CT1136JF-S makes it generate BUSY accesses in the middle of bursts. This is not handled well by the memory system, which provides slow access to high latency devices such as SDRAM. A faster solution for ARM1136JF-S software development is a PB926EJ-S + LT + CT1136JF-S.

CT1176JZF-S supports the development of TrustZone software, but the default FPGA images provided for EB do not include secure and non-secure peripherals. This can be

done by modifying the EB FPGA RTL or in custom designs on Logic Tiles, but involves some hardware prototyping.

We do not provide EB FPGA RTL that supports combinations of multiple Core Tiles. However, this can be easily generated by the customer from the RTL provided with the board.

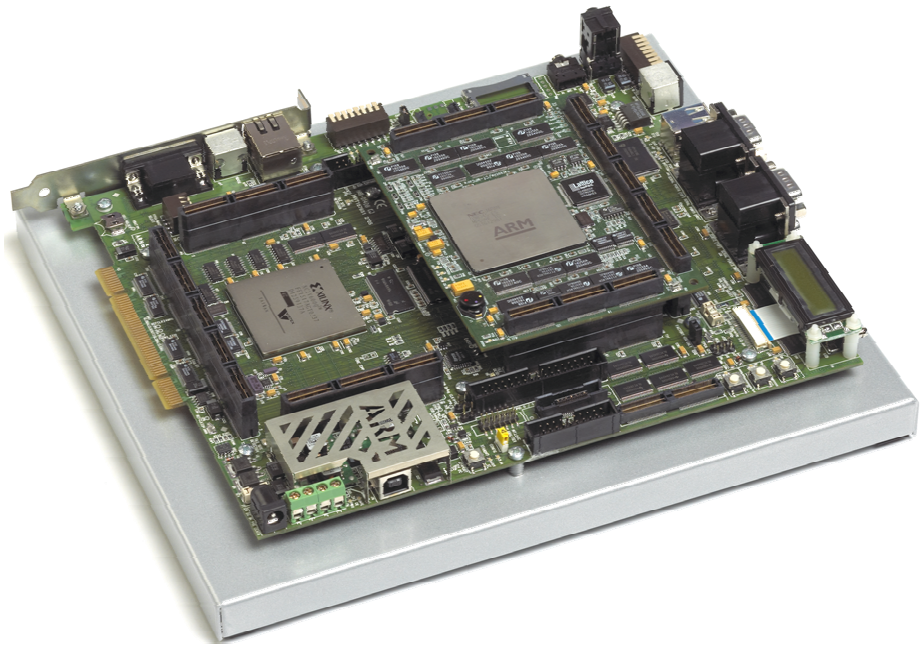


Figure 6: Core Tile for ARM11 MPCore on top of EB

An Interface Tile can be used to add extra chipsets and connectors for automotive, industrial or any custom applications. An Analyzer Tile can be used to measure signals between tiles.

Systems based on Soft Macrocell Models (SMMs) for ARM9 and ARM11 processors

Soft Macrocell Models for ARM9 and ARM11 processors use most of the signals on the bottom connectors of the Logic Tile in which they are implemented. In practical terms this means that the SMM cannot be stacked directly on top of an EB, a PB926EJ-S or an IM-LT3 interface module, but another Logic Tile is required to implement the memory system.

Since SMMs are intended for hardware prototyping and system on chip emulation, you can implement your whole ASIC in a stack of Logic Tiles or in a hardware emulation box with an interface to an SMM.

The SMM deliverables include RTL and FPGA bit files for an example memory system implemented on a Logic Tile on top of an IM-LT1 Interface Module. This memory system is very basic and does not include any peripheral controllers.

For the SMM1176JZF-S there is another SMM called "Secure Memory Logic Tile" (SMLT), which allows the processor to be stacked on top of an IM-LT3 Interface Module and a Compact Platform baseboard. This system can be used to evaluate the processor and do early software development with secure and non-secure peripherals.

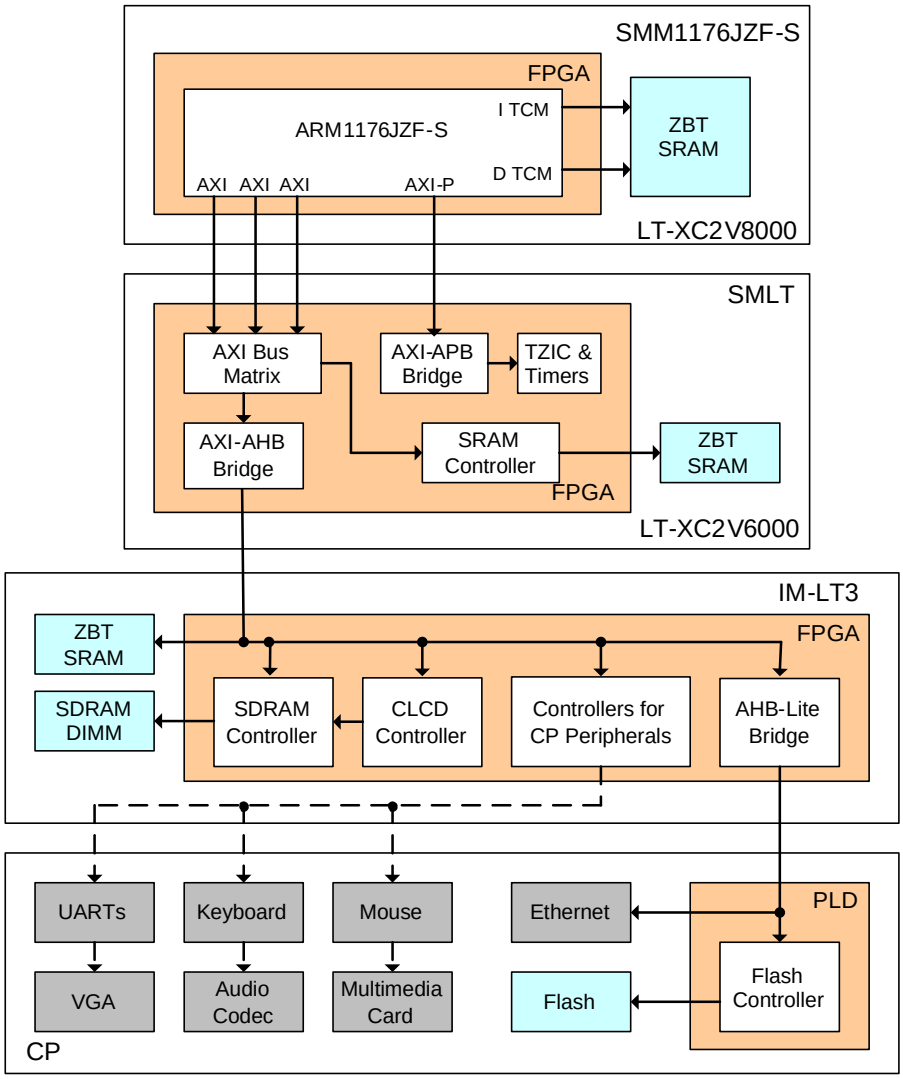


Figure 7: ARM1156T2F-S/ARM1176JZF-S software development system

Hardware Platforms in Development

The following board is currently in development.

Platform Baseboard for Cortex-A8 (PB-A8): PB-A8 will be a software and hardware development board for Cortex-A8, with similar architecture as the PB11MPCore.

For information about this board, please contact your nearest ARM sales office.

CONFIGURATIONS THAT ARE NOT SUPPORTED

RealView hardware platforms are modular in design so that you can create systems customized to your needs. This can be done by using several boards together in an unsupported configuration or by adding a board to a custom emulation system.

Core Module, Logic Module and the Compact Platform are part of the legacy Integrator family of boards, which is reaching end of life. They are no longer promoted products.

Stacking rules

When stacking several RealView boards together, some rules apply. Table 2 shows which board, if any, is required to stack two boards together:

		Board on top						
		AHB CT	**AXI CT**	**LT**	**CM**	**LM**	**IT**	**AB-IBx**
Board on bottom	**Core Tile (CT)**	LT	LT	✓	×	×	LT	×
	Logic Tile (LT)	✓	✓	✓	×	×	✓	×
	Core Module (CM)	IM-LT3	×	IM-LT1	✓a	✓	IM-LT3	×
	Logic Module (LM)	IM-LT3	×	IM-LT1	×	✓	IM-LT3	×
	Interface Tile (IT)	×	×	×	×	×	×	×
	Compact Platform (CP)	IM-LT3	×	IM-LT3	✓	✓	×	×
	Platform Baseboard (PB)	LT	LT	✓	×	×	LT	×
	Emulation Baseboard (EB)	✓	✓	✓	×	×	✓	×
	App. Baseboard (AB)	×	×	×	×	×	×	✓

Table 2: Stacking rules

✓ = connection does not require any interface board
× = connection is not possible
✓a = connection is possible with the exception of the CM922T-XA10

Note:
This table applies only to boards currently on sale. More complex stacking rules apply to obsolete board such as the CM7TDMI and AP.

Note:
AHB Core Tiles are CT7TDMI, CT946E-S, CT926EJ-S and CT1136JF-S
AXI Core Tiles are all the new Core Tiles based on AXI interfaces, such as CT11MPCore, CT1156T2F-S and CT1176JZF-S.

Multi-processor systems using Core Tiles and Logic Tiles

Currently FPGA RTL and bit files are only provided for a multi-processor system consisting of pairs of Core Tiles and Logic Tiles stacked on top of an IM-LT1 Interface Module or a PB926EJ-S.

FPGA RTL and bit files are not provided for the following configurations of boards, but it is possible to stack them:

- Two Core Tiles on the Emulation Baseboard's two tile sites. Core Tiles can also be staked on top of each other if a Logic Tile is stacked every two Core Tiles
- Several Core Modules together. This only requires a change to the Core Module FPGA RTL. The exception is the CM922T-XA10
- Core Tiles on top of Core Modules using an IM-LT3 Interface Module
- An SMM on top of a Core Tile or a PB926EJ-S using a Logic Tile
- An SMM on top of a Core Module or a Compact Platform baseboard using a Logic Tile and an IM-LT3 Interface Module

Note that, since SMMs use most of the signals of the stacking connectors, it is not possible to stack other processors on top of them.

If you are unsure about the feasibility of the system that you want to implement, please contact ARM support or your distributor for advice.

FEATURE COMPARISON

Memory and Peripherals on RealView Baseboards

The following table shows the memory and peripherals available on CP, EB, PB926EJ-S, PB11MPCore, PB1176JZF-S and AB926EJ-S. If a peripheral is provided by a daughterboard, the name of the board is written in the cell.

	CP	EB	AB926EJ-S	PB926EJ-S	PB1176JZF-S	PB11MPCore
SDRAM	✓b	256MB DDR	128MB	128MB	128MB	512MB
SRAM	✓b	4MB Cellular	2MB	2MB	2MB	2MB
NOR Flash	16MB	64MB	64MB	64MB	128MB	128MB
DoC Flash	×	64MB / ×e	64MB / ×e	64MB / ×e	×	×
PISMO expansion	×	✓	AB-IB2	✓	✓	✓
ETM	✓b	✓b	✓	✓	✓	×
ETB	✓b	✓b	×	×	✓	××
MOVE	×	×	✓	✓	×	××
VFP	✓b	✓b	✓	✓	✓	✓
VIC	×	×	×	×	×	×
GIC	×	✓	×	×	✓	✓
TZIC	×	✓c	×	×	✓	×
IEM	×	×	×	×	✓	×
DMAC	×	✓a	✓	✓	✓	✓
MMC	1	1	1	2	✓	✓
SmartCard	×	1	1	2	✓	✓
Compact Flash	×	×	×	×	×	✓
LCD	✓	✓	✓	✓	✓	✓
Keyboard	✓	✓	✓	✓	✓	✓
Mouse	✓	✓	✓	✓	✓	✓
Audio	✓	✓	✓	✓	✓	✓
Keypad	×	×	AB-IB2	×	×	×
Camera	×	×	AB-IB2	×	×	×
Bluetooth	×	×	AB-IB2	×	×	×
GSM	×	×	AB-IB2	×	×	×
UART	2	4	1	4	4	4
Ethernet	✓	✓	✓	✓	✓	✓
PCI	×	✓	×	✓	✓	✓
PCI-Express	×	×	×	×	×	✓
USB	×	Host, slave, OTG ✓	OTG only ✓d	Host, slave, OTG ✓d	Host, slave, OTG ✓	Host, slave, OTG ✓
AHB expansion	✓	✓	×	✓	×	×
AXI expansion	×	✓	×	×	✓	✓

Table 3: Memory and peripherals on RealView baseboards

✓a = EB can implement a DMA controller on its FPGA, and a netlist for a PrimeCell DMA controller is provided. However, the DMA controller is not included by default, as it affects the maximum clock frequency of the design

✓b = CP does not contain RAM, since it is normally provided by the Core Module or IM-LT3 Interface Module. ETM, ETB and VFP can be found in some Core Modules and Core Tiles

✓c = TZIC will only be provided on baseboard designs that support TrustZone

✓d = PB926EJ-S and AB926EJ-S implement USB with a Transdimension USB chipset. Unfortunately this chipset has no OS drivers publicly available, which limits its usability. EB, PB1176JZF-S and PB11MPCore implement USB with an ISP1761 USB chipset from NXP, which has Linux and WinCE drivers available from the NXP website.

×e = DoC Flash is replaced with 64MB of NOR Flash on the Pb-free versions of these boards

PISMO	Connector for static memory expansion
DoC Flash	DiskOnChip Flash
ETM	Embedded Trace Macrocell required for trace
MOVE	Video Coprocessor
VFP	Vector Floating Point Coprocessor
VIC/GIC/TZIC	Interrupt Controllers
DMAC	DMA Controller
MMC	Multimedia Card