Design Considerations for a Cost Optimized 28G NRZ / 56G PAM-4 Backplane

Rula Bakleh, Teraspeed Consulting – A Division of Samtec
Scott McMorrow, Teraspeed Consulting – A Division of Samtec
Ed Sayre, Teraspeed Consulting – A Division of Samtec
Backplane and Card Objectives

• Acceptable Performance with Margin
• Lowest Possible Cost
• Predictable Robust Design
• Utilize previous high-performance Tachyon 100G design and rules.
ExaMAX® Hyper-Gigabit Connector

This exciting new backplane system is one of the many full-signal-channel solutions available from Samtec, enabling you to take a signal from the silicon to the panel and all points in between with optimal signal integrity.

samtec.com/ExaMAX

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Steps to a Successful 28 Gbps Backplane Design

Choose PCB materials appropriate to 28 Gbps loss requirements

Create S-parameter Impedance, Insertion Loss and Crosstalk characterizations of the system channels for the various choices of PCB materials, trading off material costs and fabrication costs

Create trial stackups from the optimum results based on:

– Maximum backplane thickness based on chassis and system requirements
– Number of routing layers and slots
– Satisfying PCB differential trace impedance requirements 100 or 85 ohms. Perform trial layout and routing studies.
– Meet the performance requirements of COM or similar system operating margin requirements for the channel.
– Power requirements for the total logic card dissipation based on copper weight ampacity, power distribution voltage and safety compliance needs

Finalize the design choices based on the results of these tasks
ExaMAX® Backplane Stackup

Stackup Features:

- Overall backplane thickness ~4 mm
- 14 slots, 3 cm pitch
- 22 layers
- Tachyon material
- Smooth ½ oz. copper 100 Ω signal layers
- Backdrilled signal traces
- Buried 1 oz. power layers
- Sized to fit a 19” rack
ExaMAX® 2 mm Backplane Insertion and Return Losses: Slot 1 to Slot 14
The Basis of Teraspeed Consulting’s Backplane Design Methodology

Backplane component, footprint and end-to-end S-parameter analysis and channel characterization

- Demonstrated accuracy, case analysis speed, design optimization
- Teraspeed Tools: Highly parallelized cluster running ANSYS HFSS and SIWave

Methodology to manipulate the various component circuit and S-parameters into multi-port end-to-end system channels and back-end analysis of best and worst case with statistical backup

De-embedding structures designed into test cards and test articles

Long-term experience with the analyses of PCB structural granularity and glass weave effects, semiconductor packages, connectors and parasitic effects

Significant involvement with semiconductor development, clients and other technology partners
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ExaMAX® Backplane Test Card

Test Card Trace Length ~ 8"

Trace Loss @ 14 GHz ~ 4.4 dB
Trace Loss @ 28 GHz ~ 7.3 dB

AirMAX Alignment Pins

2 or 3x14 Exarax MA Receptacle
ExaMAX® 2 mm Test Card Connector Breakout
ExaMAX® 2 mm Test Card Connector
Breakout Insertion & Return Loss

Insertion Loss: all paths

Return Loss: all paths

Freq [GHz] vs Magnitude (decibels)

LM05
-1.02 dB
26.0 GHz

S21
Attenuation Limit

LM05
-10.6 dB
26.9 GHz

S11
S22
Return Loss Limit
ExaMAX® Backplane Connector Breakouts

S01 (left)

S14 (right)
ExaMAX® 2 mm Backplane Connector
Breakout Insertion Loss & Return Loss
Internal Routing Layers: 2 mm and 3 mm ExaMAX® Trace Geometries

S01<>S14 Length ~ 22in
ExaMAX® 2 mm Internal Backplane Trace Insertion & Return Loss

Insertion Loss: all paths

-0.545 dB/in

Return Loss: all paths

-0.91 dB/in

BC06 -20.1 dB 28.0 GHz

EF06 -21.0 dB 27.4 GHz
ExaMAX® Backplane with Test Card
ExaMAX® 2 mm Backplane + Connector Insertion and Return Losses: S01 to S14

Insertion Loss: all paths

- Connector Loss @ 14GHz ~ 0.5*(19.0 - 12.0) = 3.5 dB
- Connector Loss @ 28GHz ~ 0.5*(33.3 - 20.1) = 6.6 dB

Return Loss: all paths

- 1.84 dB at 19.1 GHz

Connecter Loss @ 28GHz ~ 0.5*(33.3 - 20.1) = 6.6 dB
End-to-End NEXT and FEXT
Crosstalk Results: S01 to S14

NEXT: all paths

FEXT: all paths

CD05
-49.3 dB
27.1 GHz

CD05
-49.8 dB
27.1 GHz

DESIGNCON 2016
WHERE THE CHIP MEETS THE BOARD
JANUARY 19-21, 2016
#DC16
28 Gbps $2^{31}-1$ PRBS Backplane Eye-diagram and Error Performance

A pair of Xilinx VCU109B 28Gbps Hyperscale FPGA test cards were used to confirm the data transfer properties of the Samtec ExaMAX® backplane.

The Xilinx VCU109B 28Gbps test cards are equipped with an ExaMAX® receptacle which interfaces directly to the HS backplane as shown in the next slide. A total of 8 differential pairs are connected between selected slots and pinouts.

Two Xilinx cards plugged into the ExaMAX® backplane, powered on, loaded with Xilinx Vivado operating system software and upon command, error free data transfers were initiated and maintained between the two cards.

The error-free eye-diagram extracted from the chip receivers is shown in the next slide.
ExaMAX® Backplane with 28 Gbps Xilinx Virtex Ultrascale Logic Cards
Xilinx VCU109B to Xilinx VCU109B - Eye Diagram
Slot 1 to Slot 14, 0.79 meters @ 28 Gbps
The Case for Cost-Reduced Design
### Relative PCB Material cost

<table>
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<tr>
<th>Material Name</th>
<th>Cost-Index-36 layer line card</th>
<th>Cost-Index-22 layer backplane</th>
<th>Loss-Df-10GHz</th>
<th>Skew Optimized</th>
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<tr>
<td>370-HR</td>
<td>1.00</td>
<td>1.00</td>
<td>0.02200</td>
<td>No</td>
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<td>IS415</td>
<td>1.14</td>
<td>1.12</td>
<td>0.01200</td>
<td>No</td>
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<td>FR408HR</td>
<td>1.65</td>
<td>1.62</td>
<td>0.00980</td>
<td>No</td>
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<tr>
<td>I-Speed</td>
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<td>1.27</td>
<td>0.00700</td>
<td>No</td>
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<tr>
<td>Nelco-13 EP</td>
<td>2.37</td>
<td>2.30</td>
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<td>Megtron-4</td>
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<td>1.69</td>
<td>0.00800</td>
<td>No</td>
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<tr>
<td>I-Speed IS</td>
<td>2.20</td>
<td>2.23</td>
<td>0.00550</td>
<td>Yes</td>
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<tr>
<td>Gigasync</td>
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<td>0.00800</td>
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<td>Nelco-13 EPSI</td>
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<td>3.54</td>
<td>0.00800</td>
<td>No</td>
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<tr>
<td>I-Tera</td>
<td>2.82</td>
<td>2.82</td>
<td>0.00320</td>
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<td>TerraGreen</td>
<td>3.03</td>
<td>3.02</td>
<td>0.00300</td>
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<td>Megtron-6</td>
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<td>Tachyon/100G</td>
<td>4.09</td>
<td>4.39</td>
<td>0.00200</td>
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</table>
ExaMax HSBP PCB Material VS Connector contribution (37” Reach)

Negligible increase in loss up to 25G due to Connectors and Vias

Up to -12 dB of additional loss at 40-50G

Take advantage of cost reductions for scalable 10-28G designs with material selection.

Better connector designs in this region will relax the requirements on materials.

PCB Material
Total PCB plus Connectors plus Vias

Material Limited Region
Connector Limited Region

JANUARY 19-21, 2016
Interconnect Reach with -25db loss
LR (Long reach) Backplane

Potential Design Space for Low Cost PCB Materials Depending on Cu Roughness

Megtron 6
ISpeed
FR408

High Cost PCB
Low Cost PCB
2X Cost

10G  25G

30” Reach
25” Reach
20” Reach
15” Reach
10” Reach
High Density Dual-Stripline Routing

- One half the routing layers.
- One 28G differential pair per 1.5 mm per layer. (One 28G pair per 2 mm for 2 mm connector.)
- 33% higher board utilization
- 50% layer count reduction.
- Significant PCB cost savings.
Dual-Stripline Routing

- Use when possible.
- Can reduce layers by 25% by removing ground layer.
- Provide sufficient crosstalk isolation by spatial topology.
Cost Reduced Backplane

16 layers vs 22
Ispeed vs Tachyon
Dual-stripline vs Isolated stripline

55% lower fabrication cost
Cascaded Link Block Diagram

A_Card Connector Breakout \( \rightarrow \) A_Card Connector \( \rightarrow \) A_Card BP Connector Breakout \( \rightarrow \) BP_Traces With Diff Materials \( \rightarrow \) B_Card BP Connector Breakout \( \rightarrow \) B_Card Connector Breakout \( \rightarrow \) B_Card Connector \( \rightarrow \) B_Card 3 in Trace
Cascaded Link Insertion Loss with Different Materials of ~19.78” & 17.37” Traces on the Backplane

Tachyon Design
-15.8 dB @ 12.5 GHz
-17.3 dB @ 14 GHz

Cost-Reduced Design
-23 dB @ 12.5 GHz
-25 dB @ 14 GHz

Red = Tachyon
Blue = I-Tera
Green = I-Speed-IS
Black = I-Speed
Orange = I-Speed 17.37” BP/I-Speed-IS 3.00” Break Boards
Cascaded Link Insertion Loss with Different Materials & ~0.7 inch Trace

Red = Tachyon
Blue = I-Tera
Green = I-Speed-IS
Black = I-Speed
# MSH210 Simulation Results Summary with I-SPEED

<table>
<thead>
<tr>
<th></th>
<th>TX-Post-Tap Values</th>
<th>21</th>
<th>26</th>
<th>31</th>
<th>36</th>
<th>42</th>
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<tbody>
<tr>
<td>After the Transmitter</td>
<td>Eye Height (mV)</td>
<td>520.8</td>
<td>393.87</td>
<td>438.23</td>
<td>439.68</td>
<td>339.88</td>
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<td>Eye Width (ps)</td>
<td>38.00</td>
<td>36.64</td>
<td>37.20</td>
<td>37.68</td>
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<td>After the Channel</td>
<td>Eye Height (mV)</td>
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<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
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<tr>
<td></td>
<td>Eye Width (ps)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
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<tr>
<td>Inside the Receiver with RX-Boost = 1</td>
<td>Eye Height (mV)</td>
<td>NA</td>
<td>NA</td>
<td>22.34</td>
<td>16.17</td>
<td>30.51</td>
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<tr>
<td></td>
<td>Eye Width (ps)</td>
<td>NA</td>
<td>NA</td>
<td>19.76</td>
<td>16.32</td>
<td>23.2</td>
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<td>Inside the Receiver with RX-Boost = 3</td>
<td>Eye Height (mV)</td>
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<td>NA</td>
<td>26.15</td>
<td>21.72</td>
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<td>Eye Width (ps)</td>
<td>NA</td>
<td>NA</td>
<td>22.24</td>
<td>19.44</td>
<td>24.24</td>
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<td>Inside the Receiver with RX-Boost = 5</td>
<td>Eye Height (mV)</td>
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<td>NA</td>
<td>29.94</td>
<td>27.37</td>
<td>34.39</td>
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<td>Eye Width (ps)</td>
<td>NA</td>
<td>NA</td>
<td>24.56</td>
<td>22.16</td>
<td>27.37</td>
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<td>Inside the Receiver with RX-Boost = 7</td>
<td>Eye Height (mV)</td>
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<td>NA</td>
<td>37.88</td>
<td>12.06</td>
<td>39.1</td>
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<td>Eye Width (ps)</td>
<td>NA</td>
<td>NA</td>
<td>28.4</td>
<td>19.68</td>
<td>27.84</td>
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<td>Inside the Receiver with RX-Boost = 8</td>
<td>Eye Height (mV)</td>
<td>18.13</td>
<td>25.53</td>
<td>23.97</td>
<td>NA</td>
<td>NA</td>
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<td></td>
<td>Eye Width (ps)</td>
<td>21.36</td>
<td>19.52</td>
<td>20.16</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>
Eyes for ISpeed Backplane Plus 3” ISpeed-IS Trace on Cards with Silicon

Short Path

Long Path

TX Post = 1

TX Post = 42
Thank you!

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QUESTIONS?