

A large, faded, light gray silhouette of a tiger's head and upper body is positioned on the left side of the page, serving as a background for the title text.

Channel Performance Metric: A Definition of Interconnect Signal Integrity Performance **White Paper**

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Abstract

In this paper, we discuss the evolution of component specifications, leading to a new “single number” figure of merit or rating system of channel performance. The Samtec Channel Performance Metric allows system signal integrity engineers to compare the relative performance of connectors and cable assemblies while factoring in noise contributions from (and interactions with) other parts of the channel. It also permits the consideration of digital signal conditioning.

The new system is based on recent developments in statistical noise analysis, including the IEEE® COM specification, which allow rapid computation of component performance in a system channel.

In this paper, we discuss the development of the Samtec Channel Performance Matrix chart and explain how it can be used to estimate a component’s performance in channels (the Channel Performance Metric) with varied loss and signal conditioning schemes. We touch on how the method can be used to perform high-level design tradeoff analysis.

Integration leads to Innovation

Samtec is structured like no other company in the interconnect industry: We work in a fully integrated capacity that enables true collaboration. The result is innovative solutions and effective strategies supporting optimization of the entire signal channel.

For more information contact SIG@samtec.com

Introduction

Samtec refers to a single figure of merit for component signal integrity performance called the Channel Performance Metric (CPM). This development was enabled by engineering advances in statistical analysis of system noise and the reduction in system simulation times which followed.

The Channel Performance Metric allows a “one number” side-by-side comparison of components, includes all common sources of system noise, and considers the application of prudent signal processing (see Figure 1).

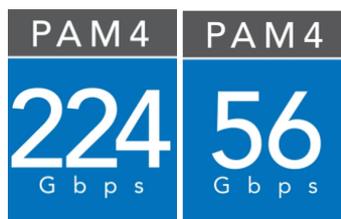


Figure 1: Selection of Samtec Channel Performance Metrics

Along with the new performance rating metric, Samtec can provide customers with a more feature-rich data set (the Channel Performance Matrix) to help system designers quickly evaluate potential system design tradeoffs and channel data rate performance limits.

Earlier Methods of Rating Component Performance

Rating connector and cable assembly signal integrity performance has always been a challenge. Since the interconnect is only one component of several in a signal channel, and because different systems have different pass/fail criteria, end performance is best predicted through circuit simulations of the entire channel. But such simulations can be extremely time intensive, so it is desirable to have a means of rapidly screening and comparing the performance of various interconnect schemes before a full channel simulation is carried out.

In the past, such comparisons were often made using frequency domain parameters such as insertion loss (IL), return loss (RL), near and far end crosstalk (NEXT, FEXT, or generically XT), and power sum crosstalk (PSXT). Related time domain parameters were also sometimes used, such as impedance (Z_0), group delay and crosstalk.

For some time, Samtec used an insertion loss limit as its “one number” figure of merit for side-by-side performance comparisons. The limit numbers chosen were -3 dB for connectors and -7 dB for cable assemblies. These values were based on traditional analog channel metrics, and while somewhat crude, offered a reasonable approximate number for side-by-side comparisons (see Figure 2).

SERIES	PITCH	STACK HEIGHT	3dB INSERTION LOSS POINT
GFZ	1,27 mm	1,65 mm	17.00 GHz
		3,00 mm	16.00 GHz
HDAM/HDAF - HD Mezz	1,27 mm	20,00 mm	9.50 GHz***
		25,00 mm	8.50 GHz
		30,00 mm	10.00 GHz
		35,00 mm	9.00 GHz
LPAM/LPAF	1,27 mm	4,00 mm	17.00 GHz+
		5,00 mm	20.00 GHz+
SEAM/SEAF - SEARAY™	1,27 mm	7,00 mm	12.50 GHz+
		10,00 mm	18.00 GHz+
		12,00 mm	16.00 GHz+
		16,00 mm	13.50 GHz+
		17,50 mm	12.50 GHz+
SEAMI/SEAF	1,27 mm	16,00 mm	14.00 GHz+
SEAMP/SEAF	1,27 mm	7,00 mm	12.00 GHz+
SEAM-RA/SEAF-RA	1,27 mm	-RA	5.00 GHz
SEAM/SEAF-RA	1,27 mm	-RA	4.50 GHz
SEAM8/SEAF8	0,80 mm	7,00 mm	12.00 GHz+
YFS/YFT - Sam Array®	1,27 mm	5,00 mm	3.50 GHz*
ZA1	1,00 mm	1,00 mm	15.50 GHz
ZA8	0,80 mm	1,00 mm	10.50 GHz

Figure 2: Example of Earlier Rating System (Samtec, Inc.)

Although such parameters may be accurately characterized, it is often difficult to intuitively map their relationship to system performance. However, if other portions of the system are known and controlled by, say, an industry standard specification, it may be possible to accurately specify acceptable interconnect performance by applying limit lines to frequency domain parameters (see Figure 3.).

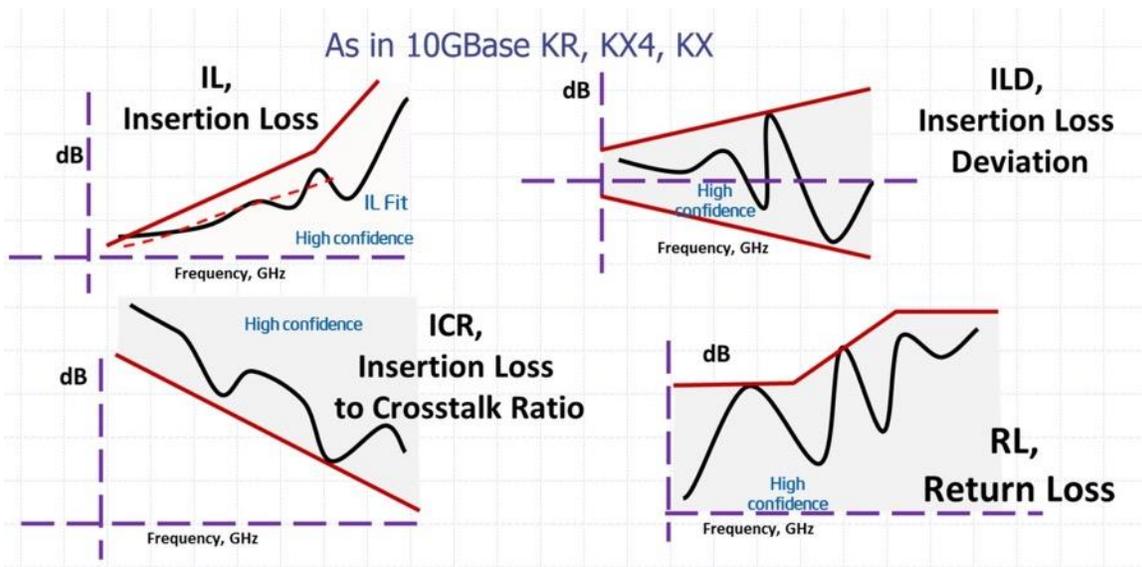


Figure 3: Example of limit lines approach to component performance specification.

However, most digital signal transmission systems operate in the time domain, and there is no clear way to map frequency domain performance to the time domain without using simulations. As a result, there are also attempts to specify component performance in the time domain.

Performance parameters can alternatively be measured in the time domain or converted from the frequency domain via Fast Fourier Transform (FFT). This information can be useful for comparing various components, but it offers limited insight into final system channel performance.

Another approach is to specify the component's eye pattern performance, or a bit error rate (BER) measurement or calculation. An important advantage of this approach is that it can combine the effects of all sources of channel performance degradation. In addition to the effects of RL, IL, and XT, higher level phenomena such as jitter and alien noise can be evaluated.

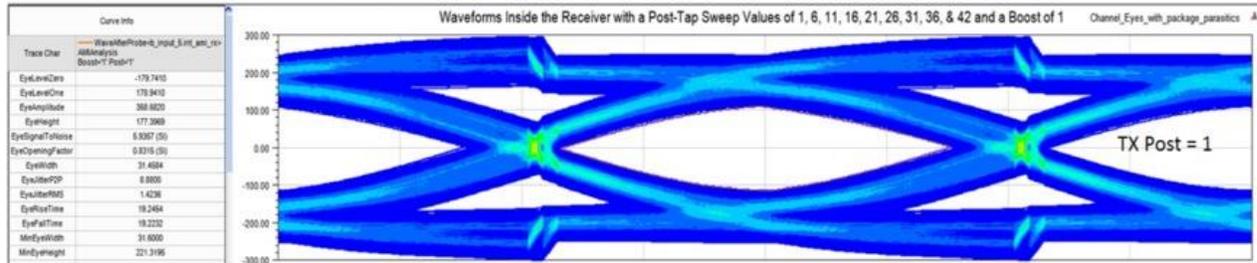


Figure 4: Example of Simulated Eye Pattern of Component or Subsystem

Unfortunately, it is not possible to predict channel performance based solely on a component's eye pattern or BER performance. For instance, the component might interact negatively with other components in the system, so the "real world" channel eye pattern may look worse than the isolated component eye pattern would indicate. Therefore, even these complex time domain approaches are still not an ideal solution.

Advantages of a System-Based Approach

A system or channel-based approach is desirable for several reasons. First, it can help avoid costly over-specification of components. A channel-based approach also allows system designers to make engineering tradeoffs between various components. For example, moving to a higher performance PCB substrate material might allow the use of a less costly or higher density connector.

Several trends have converged to drive the industry toward a system-based approach to component specification:

- As data rates and signal frequency content increase, it is more difficult to isolate the impact of individual components and noise sources.

- Increased availability and lower cost of high-performance PCB substrates and cable interconnects provide the system designer more options for channel component performance tradeoff decisions.
- Lower cost and more ubiquitous signal processing allows designers to add even more design options to the tradeoff mix.
- Continued increases in computer performance and system simulation tools have made rigorous analysis available to many more engineers.

Early channel-based specifications were based on frequency domain parameters with limit lines (see Figure 3). This approach allowed system designers to trade off component performance by performing frequency domain simulations, usually based on S-parameter models and simulations. These simulations can be performed much faster than a full system circuit simulation.

However, with the advent of low-cost and near-ubiquitous digital signal processing, the limits of these frequency-based approaches became evident. It is not possible to perfectly map the effects of such processing into the frequency domain.

An alternate approach is to use advanced statistical analysis techniques to reduce the mathematical complexity of the simulations. By establishing certain acceptable noise envelopes, full channel simulation time can be reduced by many orders of magnitude.

One such channel-based component specification is the IEEE Channel Operating Margin (COM). The COM specification is based on statistical noise analysis using S-parameter models of the individual channel components [1,2]. The COM approach allows rapid analysis of multiple channel configurations while still accounting for all sources of loss, distortion, and noise. It also allows for consideration of various signal processing techniques.

Defining a Channel

To allow Samtec signal integrity engineers to quickly answer customer questions concerning COM-type specifications, Samtec developed an internal software analysis tool based on the IEEE COM specifications. Over time, the tool was expanded well beyond those specifications, and became a more general channel performance analysis method that uses the Samtec Channel Performance Matrix to determine a product's channel performance metric.

Samtec defines a channel as shown in Figure 5.

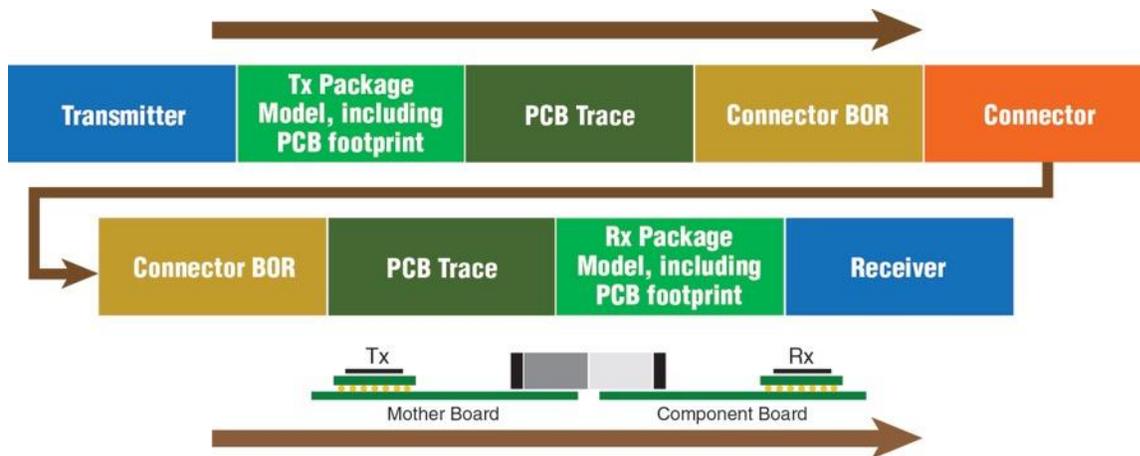


Figure 5: A Channel Defined

Models are available for each of the nine segments, and they can be varied independently. Samtec’s signal integrity engineers estimate channel performance while varying multiple channel parameters, making it an excellent tool for exploring design tradeoff decisions across a broad range of channel configurations.

Using this information, Samtec evaluates performance for connectors and cable assemblies as the substrate or cable and transceiver signal processing levels are varied. The resulting charts will be described later. First, we will discuss the models that represent each component of the channel.

Transmitter and Receiver Models

A typical Channel Performance Matrix chart displays data for five different levels of signal conditioning/processing in the transmitters and receivers. This ranges from no signal processing to a fairly significant amount.

<p><u>TX/RX 1</u></p> <ul style="list-style-type: none"> • Transmit equalization: none • Receive CTLE filter: none • Receive DFE: none 	<p><u>TX/RX 2</u></p> <ul style="list-style-type: none"> • Transmit equalization: 3-taps (1pre. 1 post) • Receive CTLE filter: none • Receive DFE: none 	<p><u>TX/RX 3</u></p> <ul style="list-style-type: none"> • Transmit equalization: 3-taps (1pre. 1 post) • Receive CTLE filter: 9 dB • Receive DFE: none
<p><u>TX/RX 4</u></p> <ul style="list-style-type: none"> • Transmit equalization: 3-taps (1pre. 1 post) • Receive CTLE filter: 9 dB • Receive DFE: 1-tap 	<p><u>TX/RX 5</u></p> <ul style="list-style-type: none"> • Transmit equalization: 3-taps (1pre. 1 post) • Receive CTLE filter: 9 dB • Receive DFE: 5-tap 	

Figure 6: The 5 levels of signal processing.

Why do we specify data for five levels of signal processing? While it is impossible to account for all possible signal condition modes, five options provide a reasonable representation of what is available.

There are times when a system designer might choose to use no or low levels of processing—such as when there is a need for high speed. Signal processing can slow data transfer times and add to latency. Another frequent concern is power consumption, and its side effect, heat. The need to remove the heat generated by transistors can be a significant engineering challenge. There may also be intellectual property concerns related to some signal processing schemes, so designers may wish to avoid them.

Package Models

Package parasitics and the design of the breakout region (BOR) from the package to the substrate can have a significant impact on channel performance. Because this can vary significantly from one case to another, we chose to use a generic case.

We use a simple package model like those used in IEEE COM standards (see Figure 7). The model consists of two shunt capacitors between a constant impedance transmission line. One capacitor represents die capacitance (C_d), and the other represents package capacitance (C_p). For Channel Performance Matrix calculations, we standardize on values of 0.13 pF for C_d and 0.09 pF for C_p . The length of the transmission line is set at 12 mm, with a 78.2 Ohm impedance.

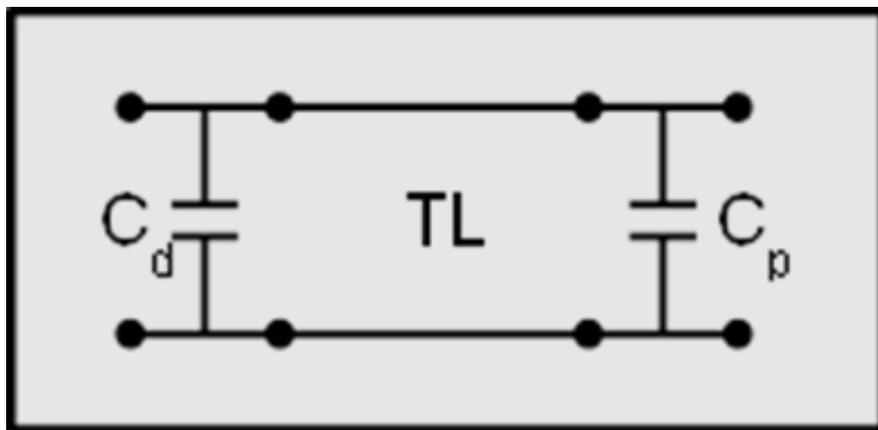


Figure 7: Schematic representation of package model.

Trace Models

The substrate (PCB) traces are microstrip with 100 Ohm differential impedance and a trace width of 10 mil (250 μ m). The models are created in 2 or 3D full wave field solvers or determined analytically and include surface roughness estimates. For certain types of plots, the trace loss, length, dielectric constant, and dissipation factor may be varied. For cable applications, the models are created using a measurement-based S-parameter extraction process.

Connector and BOR Models

The connector and associated BOR models represent a mated connector pair and its associated, optimized PCB footprint, along with any vias associated with the BOR. The S-parameter models are created in 3D full wave field solvers. In these simulations, the BOR and connector models are treated as a unit. In other words, the BOR cannot be varied separately from its connector.

An optimal (from a signal integrity perspective) signal/ground pin out assignment is chosen. We use an interior pair, as opposed to an edge or corner case, and include all nearby terminals as crosstalk aggressors.

Channel Performance Matrix Chart

A typical Channel Performance Matrix chart is shown in Figure 8. At first glance, this looks very “busy,” but it contains a great deal of useful information.

In Figure 8, the horizontal scale refers to the amount of loss in the channel substrate or cable. The vertical scale refers to the useable data rate of the channel. The colors of the blocks map to various levels of signal processing.

The pass/fail criteria used in these charts is a 3 dB channel operating margin. This equates to approximately a 30% open eye voltage level relative to the received eye level. It includes all effects of crosstalk, impedance mismatch reflections, attenuation, and jitter.

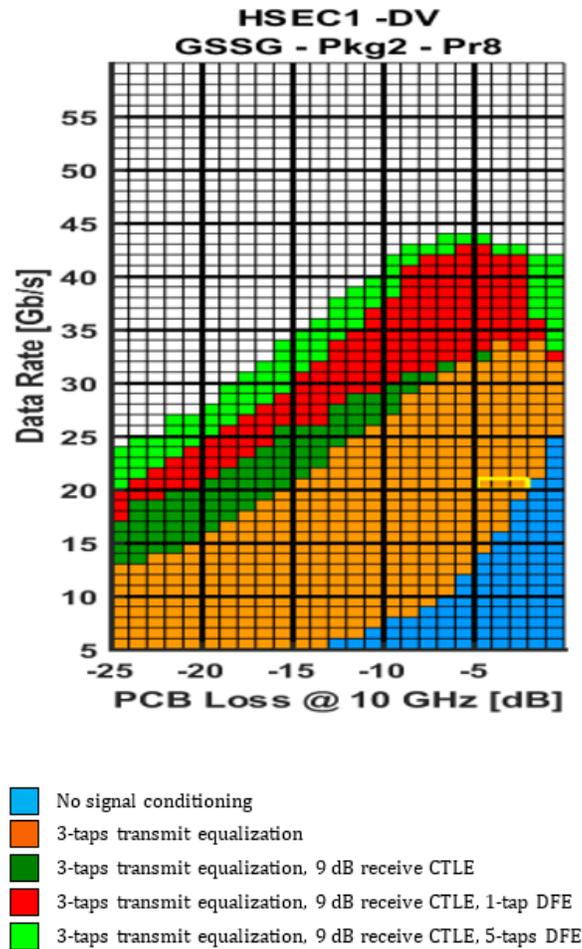


Figure 8: A Samtec Channel Performance Matrix showing performance with varying signal processing/conditioning options

Using the Matrix to Estimate Useable Data Rates

As an example, in Figure 9, a channel with 1 dB of substrate loss could operate successfully with this connector system with no signal conditioning (the blue boxes), up to a 25 Gb/s data rate. If the substrate loss is increased to 10 dB, the system can only function properly to approximately 8 Gb/s. This system fails to operate completely when PCB loss reaches 13 dB.

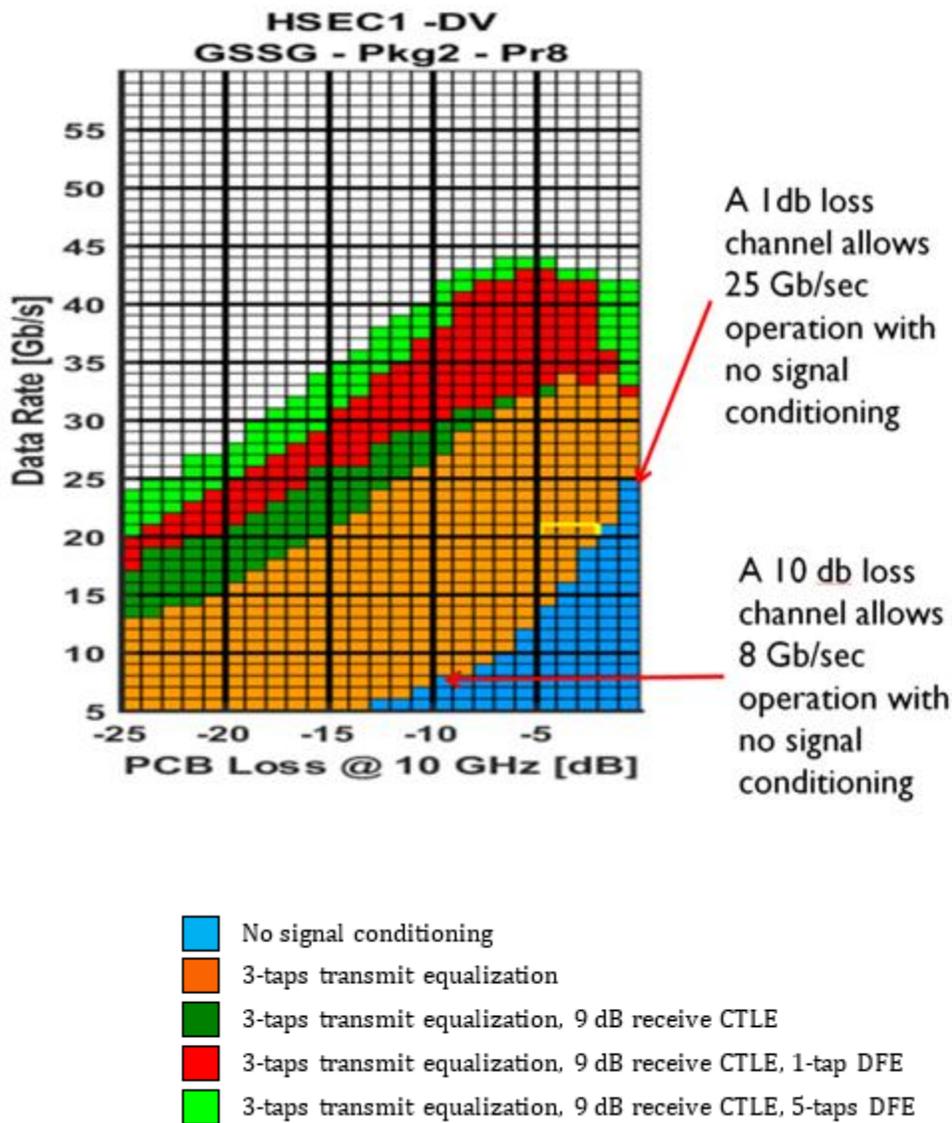


Figure 9: Determining usable bandwidth with a Channel Performance Matrix.

This system’s performance can be boosted significantly by adding some simple signal conditioning (3-tap equivalent transmit side equalization). This is represented by the orange blocks on the graph. The channel can now operate at speeds up to approximately 33 Gb/s with substrate loss of up to 4 dB. It can operate at a data rate of 13 Gb/s with a substrate loss of 25 dB.

It’s interesting to note from this chart that the zero-signal conditioning case behaves as expected, in that lower channel loss maps linearly to increased data rate.

However, as we increase signal processing, loss affects performance in different ways. In some cases, a low loss channel has a lower maximum data rate than some higher

loss channels. This can be observed in the light green and red blocks in Figure 9. Both perform better in channels with 5 dB of loss than they do in channels with 3, 2, or 1 dB of loss. This could be caused by behaviors such as resonances which are not easily corrected by current signal processing techniques, but which can be damped significantly by small amounts of channel attenuation.

Channel Performance Matrix with Substrate Tradeoff Data

Samtec has extended the utility of such charts by developing a version with substrate loss curves added to the bottom. This format allows a quick visualization of tradeoffs in choice of substrate materials.

The chart in Figure 10 allows a designer to quickly analyze changes in a given channel's performance when using four different PCB laminate materials. Material 1 (red trace) is the least expensive, highest loss material, while Material 4 (orange trace) is the best performing material. (Note that the colors of these traces have no relationship to the colors in the data rate boxes in previous figures.)

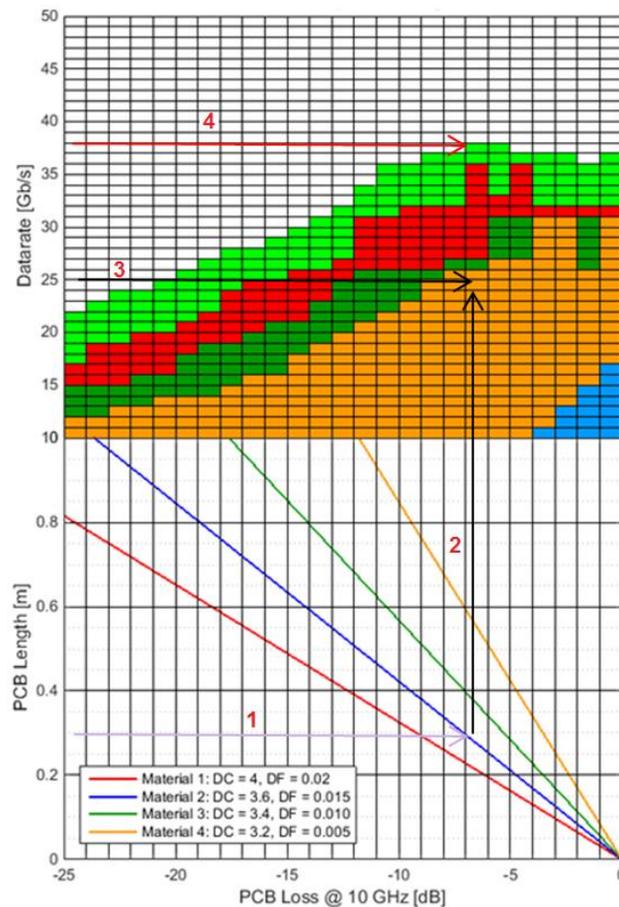


Figure 10: Channel Performance Matrix with variable substrate information.

For example, assume a design uses Material 2 shown in Figure 10 with 0.3 meters of trace. First, find the trace length on the lower left side of the chart. Then, follow the purple line (numbered 1) to the point where it intersects the loss curve for Material 2.

Next, move vertically up the chart from that point (line numbered 2) to estimate channel performance at various data rates and signal processing schemes. This chart shows that 25 Gb/s can be obtained with simple equalization (line numbered 3). A maximum of about 37 Gb/s can be obtained by using maximum signal processing (line numbered 4).

It is also possible to work in another direction with such a chart by first picking the data rate and amount of equalization desired, then choosing the correct PCB material line. Finally, follow that point to the left to arrive at the maximum allowable trace length.

Channel Performance Matrix for Cable Assemblies

The Channel Performance Matrix also provides an intuitive way to analyze cable assembly performance. In this case, we replace the PCB trace model with a cable assembly model. Short PCB trace models are included on each end.

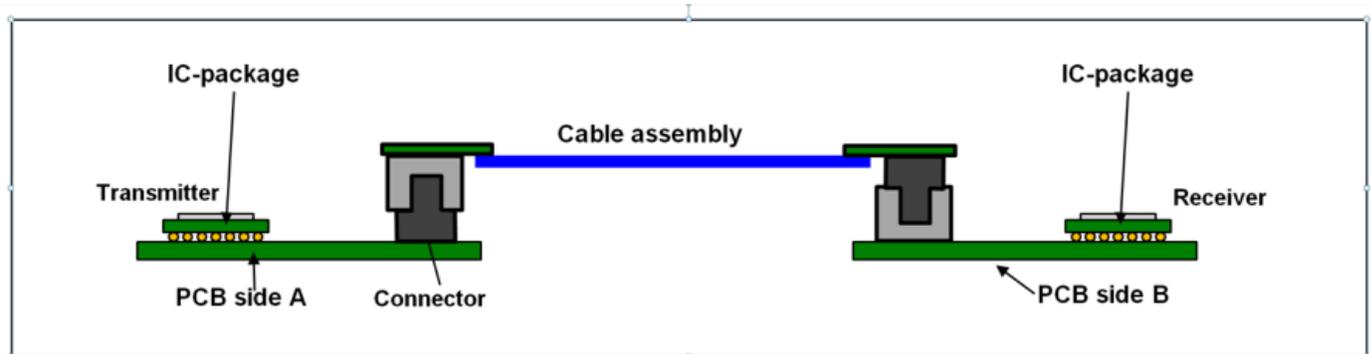


Figure 11: Channel definition for cable assemblies.

The PCBs are defined as:

- Type trace: edge coupled microstrip
- Differential impedance = 100 Ohm
- Trace width = 10 mil (250 μ m)
- Trace length = 2 inch (5 cm) = 1 dB loss
- Board material: DC = 3.5, DF = 0.01

The cable length is variable. For a cable assembly chart, we replace channel loss on the horizontal axis with cable length. An example is provided in Figure 12.

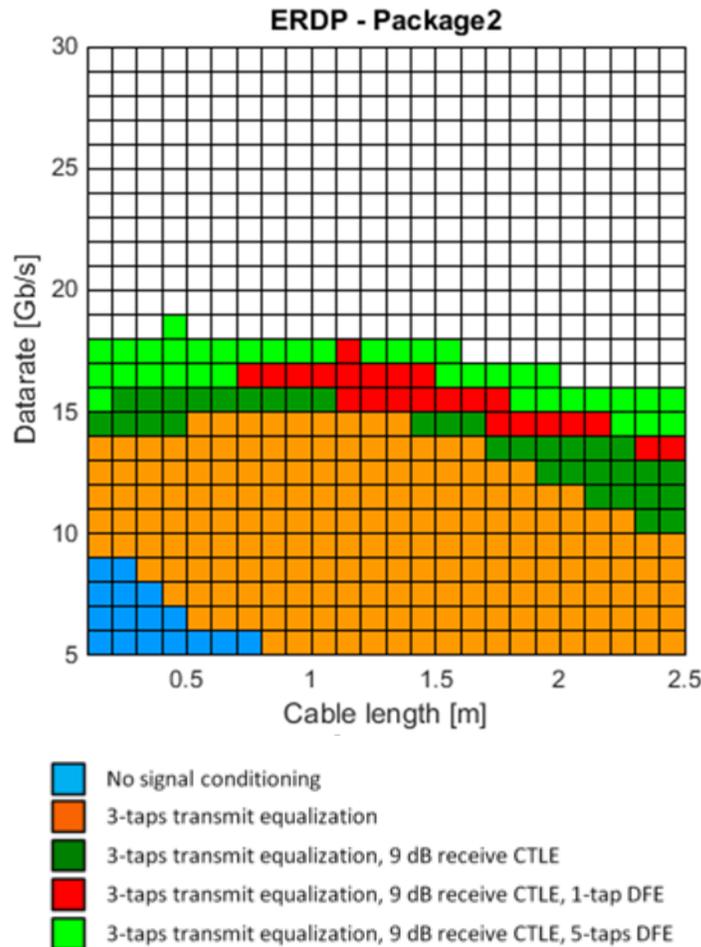


Figure 12: Channel Performance Matrix for a cable assembly.

Channel Performance Metric: Distilling Data to a Single Figure of Merit

Taking Channel Performance Matrix charts a step further can yield yet another useful piece of information. By standardizing on a certain channel configuration, we can use these calculations to establish a baseline figure of merit that allows comparing relative signal integrity performance of various interconnect components. This provides us with a single “one number” starting point for making connector and cable choices.

To establish this number, we use a channel with “average” or typical performance levels in the other non-connector or cable components.

Transceiver Model

We use the “TX/RX 2” transceiver configuration (see Figure 13), with 3-tap equivalent equalization on both transmit and receive ends. This implementation is usually easily implemented and has a small latency and power penalty.

<u>TX/RX 1 (most stringent)</u> <ul style="list-style-type: none"> • Transmit equalization: none • Receive CTLE filter: none • Receive DFE: none 	<u>TX/RX 2</u> <ul style="list-style-type: none"> • Transmit equalization: 3-taps (1pre. 1 post) • Receive CTLE filter: none • Receive DFE: none 	<u>TX/RX 3</u> <ul style="list-style-type: none"> • Transmit equalization: 3-taps (1pre. 1 post) • Receive CTLE filter: 9 dB • Receive DFE: none
<u>TX/RX 4</u> <ul style="list-style-type: none"> • Transmit equalization: 3-taps (1pre. 1 post) • Receive CTLE filter: 9 dB • Receive DFE: 1-tap 	<u>TX/RX 5 (most lenient)</u> <ul style="list-style-type: none"> • Transmit equalization: 3-taps (1pre. 1 post) • Receive CTLE filter: 9 dB • Receive DFE: 5-tap 	

Figure 13: Signal condition levels with CPM choice highlighted.

Package Model

We use the same reference package model described earlier ($C_p=0.09$ pF, $C_d=0.13$ pF, $T_L=78.2$ Ohm, 12 mm.)

PCB Trace Model

A generic loss model is assumed, which includes any associated via or footprint effects.

Cable Model

We use a 0.5-meter cable length.

Connector/BOR Model

We choose an interior pair, with an optimal signal integrity orientation, and include all nearby aggressors in crosstalk considerations.

Example: Determine the CPM for a Mated Connector Set

After a Channel Performance Matrix is calculated using the above assumptions, a channel loss of 5 dB is chosen on the horizontal axis (see Figure 14). Then we follow that column up until we reach the highest performing orange box. This number represents the highest usable data rate in a 5 dB channel with Level 2 signal processing. In this case, we would define the Channel Performance Metric (CPM) to be 32 Gb/sec.

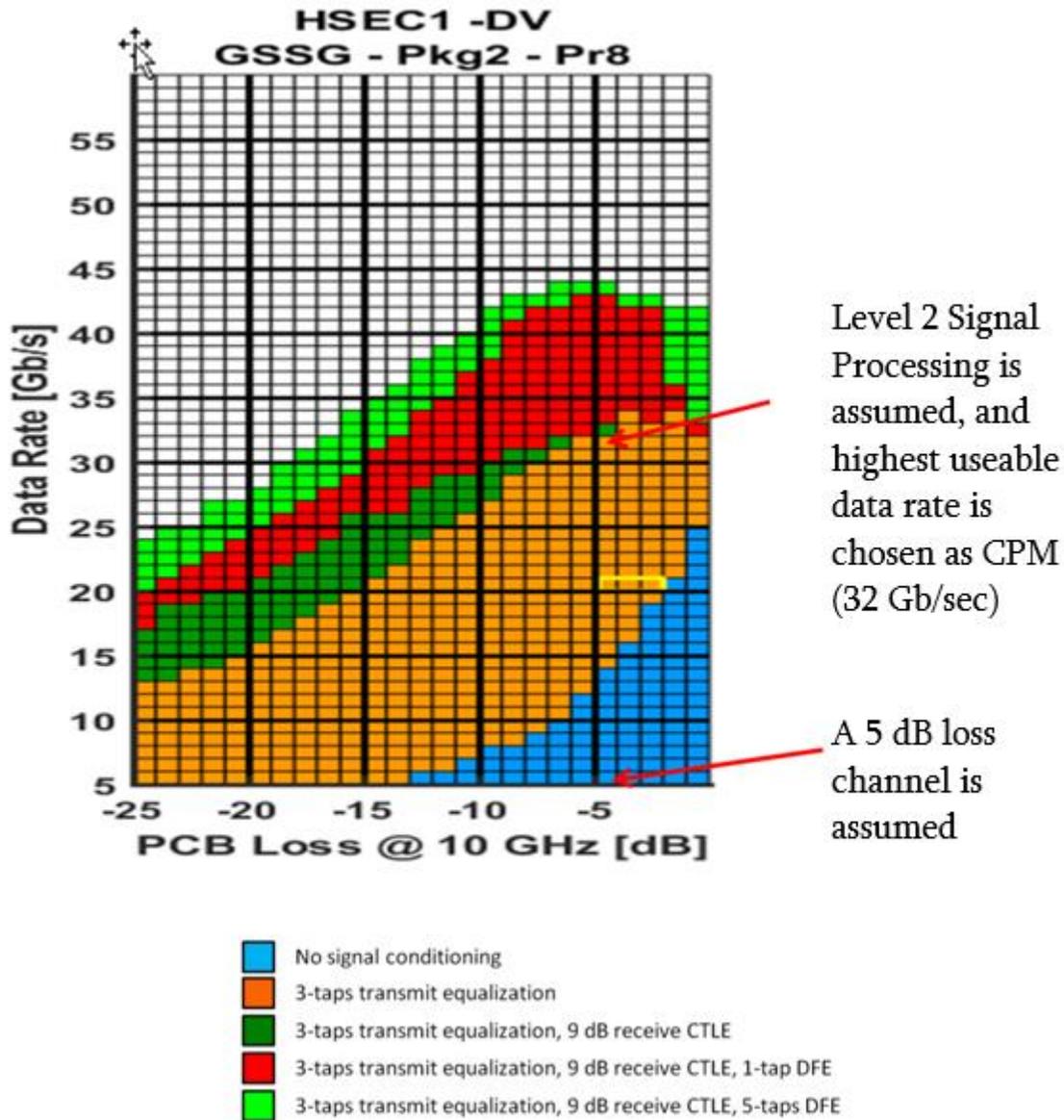


Figure 14 : Example of Channel Performance Metric Determination of 32 Gbps.

Using the Tools to Choose a Connector or Cable Assembly

The combination of Channel Performance Metric and Channel Performance Matrix, allows a system designer to quickly zero-in on a potential connector or cable assembly by following this step-by-step process:

1. Consider the Channel Performance Metric to compare various connectors or cable assemblies. This number is readily available in the catalog, on the web, and on basic data sheets. Keep in mind that CPM is based on very basic levels of signal processing, so a CPM number may underrate actual performance.
2. Decide acceptable level of signal processing, if any.
3. Decide substrate material performance level.

4. Use the Channel Performance Matrix to determine suitability of the component under the particular system assumptions.

Conclusion

We have shown how component specifications evolved and lead to a new “one number” rating system, which we call the Channel Performance Metric (CPM). This approach allows system designers to quickly compare the relative performance of connectors and cable assemblies while factoring in noise contributions from other parts of the channel and minimal signal conditioning.

We explained the development of the Channel Performance Matrix chart, explaining how to use it to estimate a component’s performance in channels with varying loss and signal conditioning schemes. We defined the channel parameters on which the Channel Performance Metric is based.

Finally, we described how the Channel Performance Metric and Channel Performance Matrix are used together to determine if a particular connector or cable assembly is appropriate for a specific system design. For a greater understanding of your system design and its associated Channel Performance Matrix, contact sig@samtec.com.

Resources

1. [gEEK® spEEK: IEEE Channel Operating Margin](#)
2. Dillinger, Tom. “[Channel Operating Margin—A Standard for SI Analysis](#),” Semiwiki, 2016.