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Validation of Achieving 100 Gb/s Signaling per Electrical Lane over 2 Meters of Passive Twinaxial Copper Cable

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Abstract

The IEEE 802.3ck Task Force is developing physical layer (PHY) specifications for operating speeds of 100 Gb/s, 200 Gb/s and 400 Gb/s based on 100 Gb/s signaling per electrical lane. The IEEE 802.3 PHY specifications contain the transmission medium as well as the mechanical and electrical interfaces between the transmission medium. The Task Force objectives include supporting operation over electrical backplanes, with an insertion loss ≤28 dB at 26.56 GHz as well as supporting operation over twinaxial copper cables with lengths up to at least 2 m; for single-lane (100 Gb/s), two-lane (200 Gb/s), and four-lane topologies (400 Gb/s).

The paper will provide a detailed technical overview of the process of validation of achieving 100 Gb/s signaling per electrical lane over 2 meters of passive twinaxial copper cable assemblies utilizing predictive simulation models and measurements. Predictive simulation models include the channel operating margin (COM) and associated parameters as well as s-parameter models for cable assemblies, test fixtures, and channels. Identification of signal rise time to be used in predictive models as well as mated test fixture parameters such as integrated crosstalk noise (ICN) and insertion loss deviation (ILD) will be addressed. The transmission parameters of the test fixtures are explored as well as their usage in testing at the various channel test points. The channel insertion loss budget between the transmitter and the receiver consisting of the host printed circuit board, the media dependent interface (MDI) and the copper media will be considered in detail including assumed BGA and VIA insertion losses. The PHYs mechanical/electrical interfaces medium dependent interfaces (MDIs) SFP112, SFP112-DD, QSFP112, QSFP112-DD, microQSFP, QSFP-DD, and OSFP will be discussed as related to cable assembly and mated test fixture transmission and crosstalk characteristics and COM.

Biographies

Chris DiMinico is President of MC Communications a telecommunications consulting firm and President/CTO of PHY-SI, LLC producing high speed test fixtures. Chris has over 30 years of experience in the telecommunication industry and plays an active role in the development of a number of telecommunication industry standards. Chris is an active participant and technical contributor in IEEE 802.3; most recently participating in the technical and editorial development of 802.3cd (50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4), 802.3ck (100GBASE-CR, 200GBASE-CR2, 400GBASE-CR4), 802.3cg -10 Mb/s Single Twisted Pair Ethernet Task Force and 802.3ch -Multi-Gig Automotive Ethernet PHY Task Force. Chris is the liaison officer from IEEE 802.3 to TIA-TR42 and is the chair of 802.3.24.2 Iot Vertical Applications Task Group.

Mike Sapozhnikov is a Principal Engineer/Signal Integrity Manager at Cisco Systems. He is responsible defining Next Generation Architecture, IP selection, Methodology Development, Signal and Power Integrity for Enterprise Access Switching. Mike has over 20 years of experience developing ASIC and systems under various Signal Integrity and HW design roles as a Manager and Individual Contributor. Mike received his B.S. in electrical engineering from SJSU.

Mike Resso is the Signal Integrity Application Scientist in the Internet Infrastructure Group of Keysight Technologies and has over twenty-five years of experience in the test and measurement industry. His background includes the design and development of electrooptic test instrumentation for aerospace and commercial applications. His most recent activity has focused on the complete multiport characterization of high speed digital interconnects using Time Domain Reflectometry and Vector Network Analysis. He has authored over 30 professional publications including a book on signal integrity. He received a Bachelor of Science degree in Electrical and Computer Engineering from University of California.

Curtis Donahue is a lead Engineer in the Ethernet consortiums at the University of New Hampshire

InterOperability Laboratory (UNH-IOL), managing both the Backplane Ethernet Consortium and Automotive Ethernet Consortium. Curtis has been employed at the UNH-IOL since 2007 and oversees conformance testing of several Ethernet PHY groups. His main focus has been the development of test setups for physical layer conformance testing, and their respective test procedures, for High Speed Ethernet and Automotive Ethernet applications. Curtis also actively participates in IEEE 802.3 and contributes to several projects, including editorial duties for 100BASE-T1, 1000BASE-T1, and 40GBASE-T.

Michael Klempa is a lead Engineer in the Storage and Ethernets groups at the IOL. He has worked at the InterOperability Lab since 2010, performing physical layer conformance, interoperability testing and test suite development for various groups. In the past Michael has performed Platform Validation Engineering at Intel, and new efforts include 400G Ethernet.

O.J. Danzy is a Senior RF and Microwave Application Engineer at Keysight Technologies specializing in areas surrounding physical layer test, network analysis, test system design and automation. Most recently he has focused on standards-based test system design and development, fixture removal and in-fixture calibration methods and techniques for multiport network analysis applications. He received Bachelor of Science in Electrical Engineering from Tennessee State University and a Master of Electrical Engineering from Cornell University.

Richard Mellitz is presently a Distinguished Engineer at Samtec, supporting interconnect signal integrity and industry standards. Prior to this, he was a Principal Engineer in the Platform Engineering Group at Intel. Richard was a principal member of various Intel processor and I/O bus teams including Itanium®, Pentium®, PCI Express®, SAS®, and Fabric (Ethernet, IB, and proprietary). Additionally, he has been a key contributor for the channel sections IEEE802.3 backplane and cabling standards, and for the Time domain ISI analysis for IEEE802.3 Ethernet, known as COM (Channel Operating Margin), which is now an integral part of Ethernet standards due to Rich's leadership. He founded and chaired an IPC (Association Connecting Electronics Industries) committee delivering IPC's first PCB loss test method. Prior to this, Rich led industry efforts at IPC to deliver the first TDR (time domain reflectometry) standard which is presently used throughout the PCB industry. Richard holds many patents in interconnect, signal integrity, design, and test. He has delivered numerous signal integrity papers at electronic industry design conferences.

Jane Lim is a Senior Signal Integrity Manager at Cisco Systems, working on high-speed signaling and product development of high-end data center routers and switches. She has been working at Cisco since 2003, specialized in front panel interface design, optical modules testing and qualification, high-speed SerDes electrical requirements, high bandwidth channel modeling, and SI/PI system solutions. Prior to joining Cisco, she worked for LSI Logic Corp on advanced packaging solutions, and IC/Package/PCB co-design. Jane is an active member of IEEE 802.3 Ethernet groups related to optical and electrical interfaces, she is currently working on .3ck 100G per lane electrical interface. Jane received her Ph.D and MPhil degrees in Electrical Engineering from University of Cambridge, U.K.

Contributors

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Validation of twinaxial copper objectives

The 802.3ck project objectives represent a distilled set of high-level technical requirements approved by the 802.3 Working Group and then executed by the 802.3ck Task Force. Examples of objectives include operating speed (bit rate), media type, reach, BER, coexistence, compatibility etc. The 802.3 Working Group uses the 802,3ck Task Force objectives to assess project completion therefore the Task Force carefully crafts objectives as succinct "must have" requirements.

The IEEE 802.3ck 100 Gb/s per electrical lane Task Force includes objectives for defining operation over:

- electrical backplanes supporting an insertion loss ≤ 28 dB at 26.56 GHz for single-lane 100 Gb/s PHY, two-lane 200 Gb/s PHY, and four-lane 200 Gb/s PHY
- twinaxial copper cables with lengths up to at least 2 m for single-lane 100 Gb/s PHY, two-lane 200 Gb/s PHY, and four-lane 200 Gb/s PHY.

In addition to "shall have" explicit objectives, Task Groups will generally have a number of implicit "should have" objectives. For the 802.3ck Task Group "should have" objectives include;

- A common channel insertion loss for backplane and copper cable to enable economies of scale for suppliers of devices supporting operation over both.
- Support at least `4.5" signal routing length from chip to MDI-host receptacle, electrically referred to as host insertion loss.
- Maximum copper cable outer dimensions consistent with 26 AWG copper cable outer diameter (OD)

The process of validation of the twinaxial copper cable up to at least 2 m objective is given below;

- Develop channel insertion loss budget;
    - Insertion loss consistent with backplane ≤ 28 dB at 26.56 GHz
    - Insertion loss to support up to at least 2 m consistent with 26 AWG copper cable
    - Insertion loss to support a minimum of 4.5" host routing length, BGA, and via.
    - Insertion loss of MDI connector and via
- Demonstrate 3 dB Channel Operating Margin (COM) for maximum insertion loss channel and near-end crosstalk and far-end crosstalk paths.

The 802.3ck Task Group is essentially challenged to double the Baud with approximately the same channel insertion loss budget at twice the frequency. Signaling rate and related specification frequencies are given in Table 1. Associated comparisons to 50GBASE-R PHYs and 100GBASE-R PHYs are provided for consideration of specification implementation differences. Notation of "to be determined" (TBD) are provided with proposed target values not yet approved by 802.3ck Task Group.

Baseband media type	Signaling Rate (GbD) = f_b	$f_b/2$ (GHz)	Cable Assembly (GHz) ~.75* f_b	Receiver Bandwidth (GHz) .75* f_b
50GBASE-CR 100GBASE-CR2 200GBASE-CR4	26.5625	13.28125	19	19.92
100GBASE-CR1 200GBASE-CR2 400GBASE-CR4	53.125	26.5625	38 (TBD)	39.84

Table 1 – Signaling rate and related specification frequencies

Test Point Definitions

The channel and cable assembly test points are provided for conformance testing and as a reference for specification parameters. Table 2 describes the five test points. Figure 1 illustrates the test points and channel definition. Cable assembly measurements are to be made between TP1 and TP4. The specified cable assembly test fixture, or its equivalent, is required for measuring the cable assembly specifications at TP1 and TP4. The electrical transmit signal is defined at the output end of the mated connector (TP2) and all receiver measurements and tests are made at the input end of the mated connector (TP3).

Test Points	Description
TP0 to TP5	The channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	Test points for all cable assembly measurements. The cable assembly test fixture, or its equivalent, is required for measuring the cable assembly specifications in 162.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair is included in both the transmitter and receiver specifications. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is specified.
TP2	Unless specified otherwise, all transmitter measurements are made at TP2 utilizing the specified test fixture.
TP3	Unless specified otherwise, all receiver measurements and tests are made at TP3 utilizing the specified test fixture.

Table 2 – Test points

The channel is defined between the transmitter and receiver blocks to include the transmitter and receiver differential controlled impedance printed circuit board and the cable assembly illustrated in Figure 1. For the 100GBASE-CR1, 200GBASE-CR2 and 400GBASE-CR4 port types the link consists of a copper cable assembly. The Media Dependent Interfaces (MDIs) refer to the connector interfaces. The MDI couples the PMDs to the cable assembly.

The components of the channel that may have different impedances are identified with yellow labels in Figure 1; PMD device package mounting, PCBs, connectors, cable attachments, and cable.

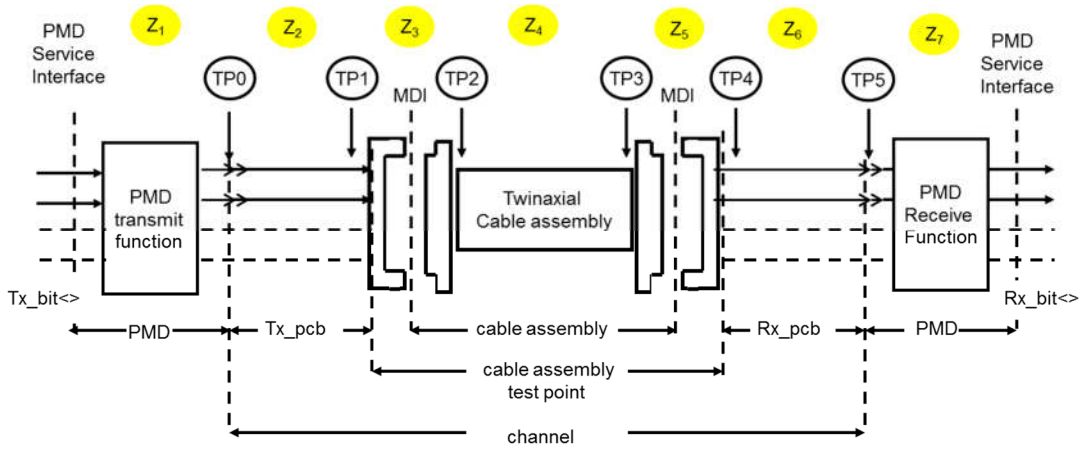


Figure 1 - Channel and Test Points

Channel insertion losses

The IEEE 802.3ck PHY specifications include the transmission medium as well as the mechanical and electrical interfaces for backplane and twinaxial copper cables. Channel transmission characteristics for backplane and twinaxial copper cables are specified to ensure the bit error ratios (BERs) or the frame loss ratio equivalent for 100 Gb/s, 200 Gb/s and 400 Gb/s are met.

The backplane channel is illustrated in Figure 2 supporting an insertion loss of ≤28 dB at 26.56 GHz.

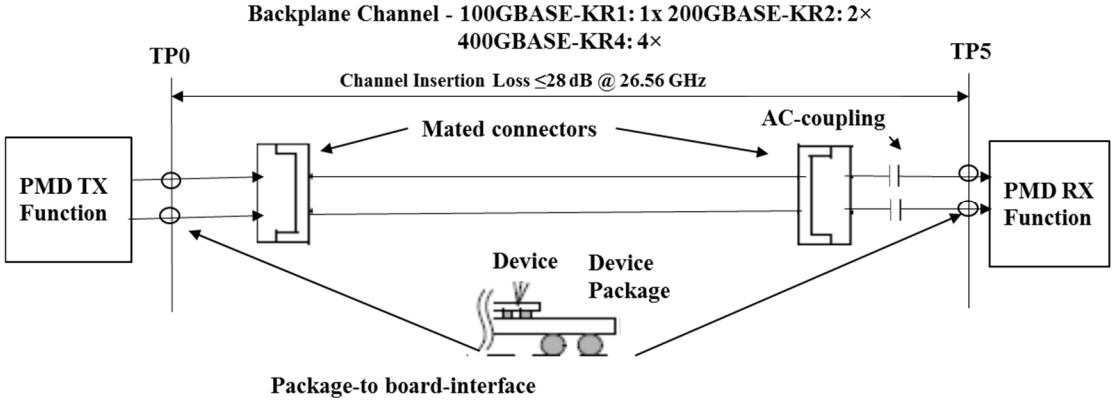


Figure 2 – Backplane channel

The channel for the twinaxial copper cable is illustrated in Figure 3 supporting operation with lengths up to at least 2 m with a channel insertion loss of ≤28.5 dB at 26.56 GHz. The insertion loss allocation for the cable assembly is constrained by the maximum allowable insertion loss at 26.56 GHz of the channel (28.5 dB), host (6.875 dB), and connector (1.6 dB). The cable assembly including plug PCB wire termination, connector, and host insertion budgets are shown to describe their contributions to the channel insertion loss budget. The host loss includes via allowances for ball grid array (BGA) and connector footprint

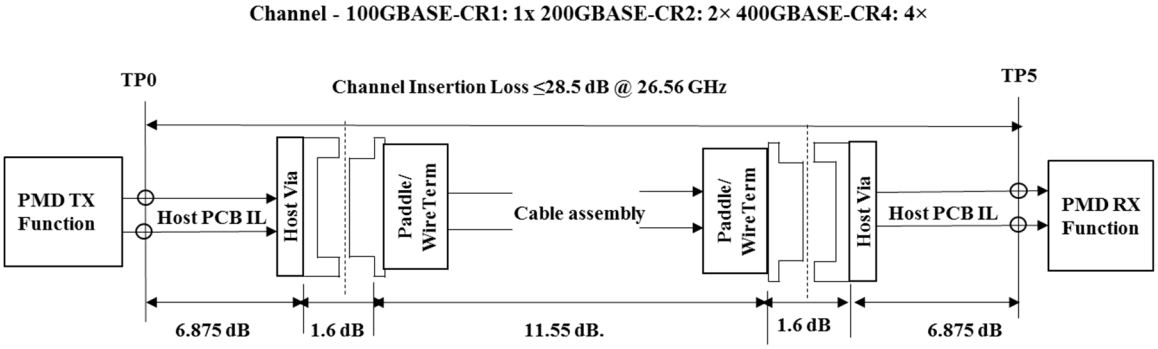


Figure 3 – Channel twinaxial copper up to 2 m (dB @26.56 GHz)

The test fixture and host insertion losses @26.56 GHz are illustrated in Figure 4. The MCB PCB insertion loss of 2.3 dB includes the test point insertion loss (SMA). The module compliance board (MCB) connector insertion loss includes via allowance of 0.2 dB. The host PCB IL of 6.875 dB includes via allowances for BGA footprint via and connector footprint via.

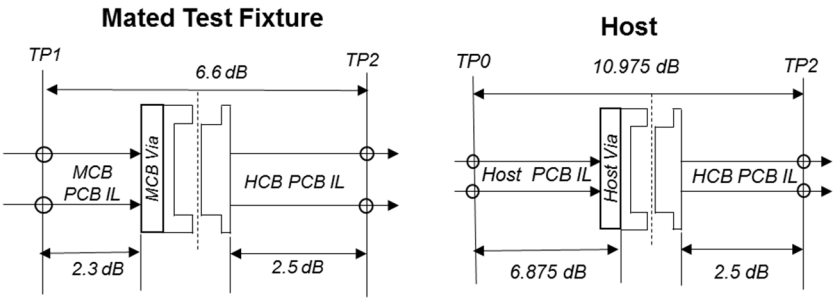


Figure 4 – Mated test fixture and host insertion loss @ 26.56 GHz

The channel and test fixture insertion loss allocation is given in Table 3 for 50GBASE-R PHYs and 100GBASE-R PHYs for comparisons.

Component	50GBASE-CR,100BASE-CR2, 200GBASE-CR4 Insertion Loss dB @ 13.28 GHz	100GBASE-CR1,200GBASE-CR2, 400GBASE-CR4 Insertion Loss dB @ 26.56 GHz
Module Compliance Board (MCB) PCB	1.2	2.3
Host Compliance Board (HCB) PCB	1.38	2.5
Host PCB IL	7	6.875
Host Connector	1.69	1.6
Host	10.07	10.975
Mated Test Fixture (MTF)	3.65	6.6
MTF connector	1.07	1.6
Bulk cable and wire attachment	12.62	11.55
Channel	30	28.5

Table 3 –Channel: twinaxial copper insertion loss allocation

100GBASE-CR1, 200GBASE-CR2, 400GBASE-CR4 defines a full set of cabled channel electrical specifications including insertion loss, return loss, crosstalk, channel operating margin (COM), and effective return loss (ERL). Table 4 summarizes the specified channel parameters and frequency range as well as the cable assembly, host, and test fixture insertion loss budgets @ 26.56 GHz.

Parameter description	f(GHz)	Unit
Transmitter and receiver differential printed circuit board trace loss (host PCB insertion loss 6.875 dB @26.56 GHz)	0.05≤f≤38(TBD)	dB
Host Channel insertion loss (10.975 @26.56 GHz)	0.05≤f≤38(TBD)	dB
Maximum cable assembly insertion Loss (19.75 dB @26.56 GHz) including cable assembly test fixtures (TP1-TP4)	0.05≤f≤38(TBD)	dB
Minimum cable assembly insertion loss (11.08 dB @26.56 GHz)	0.05≤f≤38(TBD)	dB
Maximum channel insertion loss (28.5 dB @26.56 GHz)	0.05≤f≤38(TBD)	dB
Minimum channel insertion loss (19.84) dB @26.56 GHz)	0.05≤f≤38(TBD)	dB
Channel ERL at TP0 and at TP5 shall be ≥ (TBD)		dB
Channel operating margin (3 dB)		dB

Table 4 – Channel differential electrical specifications

Channel operating margin

The Channel Operating Margin (COM) is a figure of merit for a channel derived from a measurement of its scattering parameters. COM is related to the ratio of a calculated signal amplitude to a calculated noise amplitude at a receiver input. Given "n" transmitters are used to transfer data between PHYs, there are "n" near-end crosstalk paths and "n-1" far-end crosstalk paths into a victim receiver illustrated in Figure 5. The specific number of paths depend on the number supported lanes.

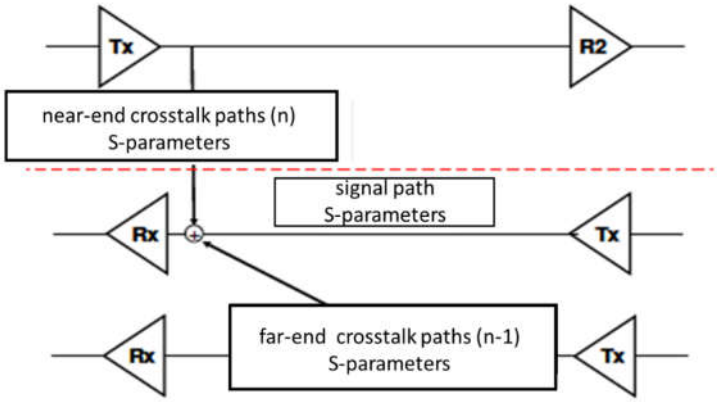


Figure 5 COM signal paths and crosstalk paths

COM is computed using defined path calculations and a specified procedure. In addition to S-parameters, COM accepts parameter values such as signaling rate, frequency (min, max, and step) and device package model to use in the computation. For convenience, and to ensure consistency in computational results, the COM procedure has been implemented in a MATLAB® script. An accompanying spreadsheet referred to as "COM configuration file" is used to load the parameter values into the MATLAB® procedure script. Configuration files are version numbered and labeled "CR" for twinaxial cable and "KR" for backplane.

A “CR” COM configuration file is illustrated in Figure 6. Versioned configuration files and MATLAB® procedure scripts are available in 802.3ck public tools http://www.ieee802.org/3/ck/public/tools/. The example configuration file depicted here is the latest released version COM 2.76.

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	53.125	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.415	V	vp/vf=.694
A_fe	0.415	V	vp/vf=.694
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02: 0]		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	12	UI	
b_max(1)	0.85		
b_max(2..N_b)	0.2		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	21.25	GHz	
f_p1	21.25	GHz	
f_p2	53.125	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.6640625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\100GEL_CR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10	dB
DER_0	1.00E-04	
T_r	6.16E-03	ns
FORCE_TR	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.3407E+09	
rho_x	0.21	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	12	UI
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	9.00E-09	V^2/GHz
SNR_TX	32	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
benartsi_3ck_01_0119 & mellitz_3ck_01_0119		
Table 92–12 parameters		
Parameter	Setting	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	1 dB / in
board_tl_tau	5.790E-03	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	110.3	mm
z_bp (NEXT)	110.3	mm
z_bp (FEXT)	110.3	mm
z_bp (RX)	110.3	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	1	logical
Floating Tap Control		
N_bg	3	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	40	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
B_float_RSS_MAX	0.03	RSS tail tap limit
N_tail_start	25	(UI) start of tail taps limit
ICN parameters		
f_v	0.723	*Fb
f_f	0.723	*Fb
f_n	0.723	*Fb
f_2	39.844	GHz
A_ft	0.600	V
A_nt	0.600	V
heck_3ck_03b_0319	Adopted Mar 2019	kasapi_3ck_02_1119
walker_3ck_01d_0719	Adopted July 2019	Adopted Nov 2019
result of R_d=50		under consideration
benartsi_3ck_01a_0719	require COM 2.72 or later	
mellitz_3ck_03_0919	mellitz_3ck_03_1119	

Figure 6 COM configuration spreadsheet

Cable assembly COM is computed from path measurements between TP1 and TP4. A mathematical model of a printed circuit board (PCB) routing is added to extend the channel to TP0 and TP5 illustrated in Figure 7.

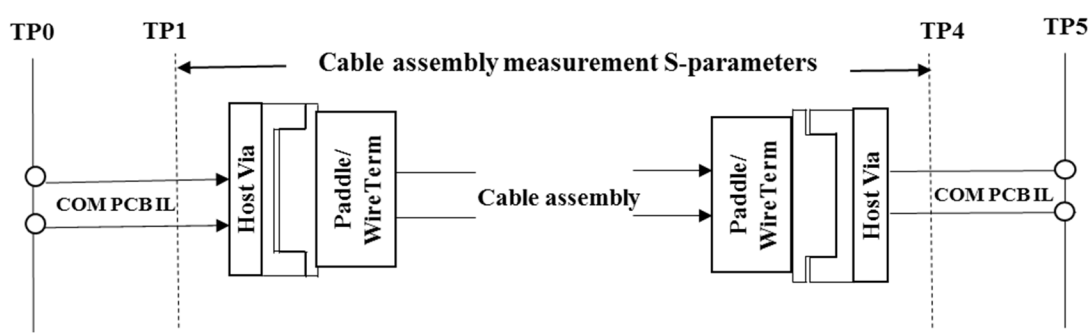


Figure 7 Cable assembly COM added PCB IL

For 50GBASE-R PHYs, once the PCB routing is added to the cable assembly measurement, the COM computation for “CR” and “KR” are identical. For 100GBASE-R PHYs, this is mostly true with a few expectations;

- CR additional PCB uses improved material assumptions from Megtron 6-like to Megtron 7-like.
- Two capacitors are added to emulate reflections at BGA and connector footprints.

For 100GBASE-R PHYs a single side of the differential pair circuit is for the PCB is shown in Figure 8. Also, Figure 8 depicts the IEEE802.3 Annex 93A transmission line parameters for Megtron 7-like construction with approximately 1 dB/inch loss at 26.56 GHz. Details of this are also shown in Figure 9 as a clip from the configuration spreadsheet.

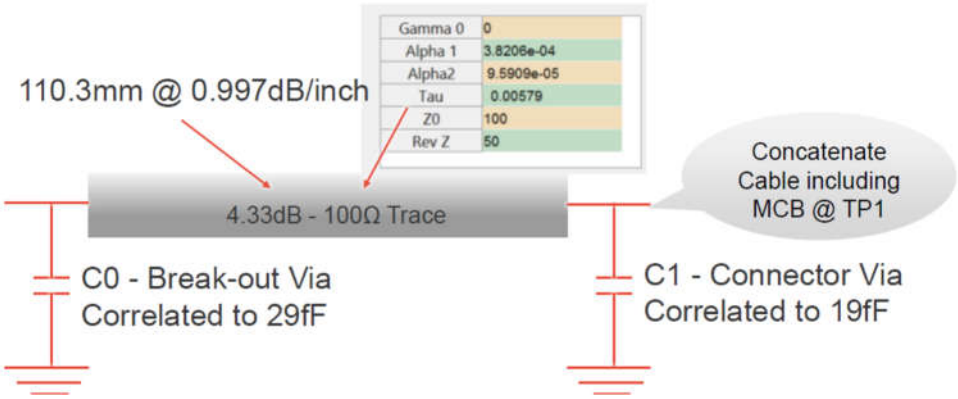


Figure 8 100GBASE-CR PHYs capacitors and material assumptions

Table 92–12 parameters1	100GBASE-CR1/CR2/CR4	Units
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	110.3	mm
z_bp (NEXT)	110.3	mm
z_bp (FEXT)	110.3	mm
z_bp (RX)	110.3	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	**1**	**logical**

Table 92–12 parameters	50GBASE-CR/CR2/CR4	Units
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 4.114e-4 2.547e-4]	
board_tl_tau	6.191E-03	ns/mm
board_Z_c	100	Ohms
z_bp (TX)	151	mm
z_bp (NEXT)	110	mm
z_bp (FEXT)	110	mm
z_bp (RX)	151	mm
Include PCB	**1**	**Value**

Figure 9 COM CR configuration file parameter differences PCB and capacitors

Highlights are illustrated in Figure 10 of the COM differences between 50GBASE-R PHYs and 100GBASE-R PHYs. These apply to both CR and KR with the exception that the transmitter and receiver noise increase is only applicable to CR.

- DFE Floating taps
  - 3 groups of 3 taps
- Pre cursor Tx FFE tap -3
- Tail tap power limits
  - RSS limit for table taps (COM 2.76 and later)
- N_bx added to spread sheet for ERL
- Lower loss package traces
- Multi segment package traces
- Added model for T-coil equivalent to device/package
- Transmitter and receiver noise increased to emulate additional crosstalk in vias, break-outs, and routing

filter and Eq		
f_r	0.75	*fb
c(0)	0.54	
c(-1)	[-0.34:0.02:0]	
c(-2)	[0:0.02:0.12]	
c(-3)	**[-0.06:0.02: 0]**	
c(1)	[-0.2:0.05:0]	
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3000	
beta_x	2.3407E+09	
rho_x	0.21	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	**12**	**UI**

- **DFE Floating taps**
  - 3 groups of 3 taps
- **Pre cursor Tx FFE tap -3**
- **Tail tap power limits**
  - RSS limit for table taps
- **N_bx added to spread sheet for ERL**

Floating Tap Control		
N_bg	3	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	40	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
B_float_RSS_MAX	0.03	rss tail tap limit
N_tail_start	25	(UI) start of tail taps limit

Figure 10 COM configuration file DFE, FFE, Tail tap, N_bx

The reference package model received a performance upgraded for 100G KR and CR COM computations as illustrated in Figure 11. The top of the figure is the single sided package with device load circuit model. Note that the package transmission line model is segment and a capacitor and inductor pair were added to emulate performance of a T-coil. The bottom of Figure 11 is a clip from the configuration spreadsheet of the package/device loading parameters.

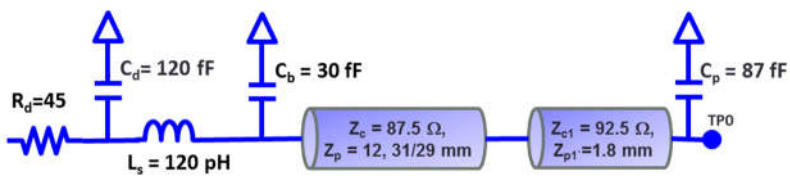


Table 93A-1 parameters			
Parameter	Setting	Units	Information
C_d	[1.2e-4 1.2e-4]	nF	[TX RX]
L_s	[0.12, 0.12]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 2990; 1.8 1.8]	mm	[test cases]
C_p	[0.87e-4 0.87e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.141E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm

- Lower loss package traces
- Multi segment package traces
- Added model for T-coil equivalent to device/package

Figure 11 COM configuration file parameters T-coil equivalent

The transmitter and receiver noise in the COM configuration were increased to reflect additional noise in the BGA and connector breakout routing. The transmitter noise SNR_Tx is the limit of SNDR (signal to noise and distortion ratio) allowed for a device. Part of which includes the crosstalk of an actual package. The decrease in SNR_TX (Figure 12), compared to KR, represents the allowable crosstalk in the Host PCB's BGA breakout. This value is assured with SNDR measurements at TP2. In addition to the transmitter host's noise increase the receiver's noise, eta_0 (Figure 12), is increase as well.

Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	**9.00E-09**	V^2/GHz
SNR_TX	**32**	dB
R_LM	0.95	

Figure 12 COM configuration file parameters eta_0, SNR_TX

Cable assembly mechanicals

The twinaxial copper cable assembly consists of shielded signal pairs utilized for differential signaling at 100 Gb/s per differential signal pair.

- 100GBASE-CR1: two differential signal pairs or lanes in each direction are used for a total of four differential signal pairs. The 100GBASE-CR1 is a single-lane cable assembly enabling a 2 m length (and can also be implemented as a multiple version using a four-lane or eight-lane plug for high density applications).
- 200GBASE-CR2: four differential signal pairs or lanes in each direction are used for a total of eight differential signal pairs. The 100GBASE-CR2 is a two-lane cable assembly enabling a 2 m length (and can also be implemented as a multiple version using a four-lane and eight-lane plug for high density applications).
- 400GBASE-CR4: eight differential signal pairs or lanes in each direction are used for a total of sixteen differential signal pairs. The 400GBASE-CR4 is a four-lane cable assembly enabling a 2 m length..

The 100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4 physical layer devices are referred to as hosts. The Media Dependent Interface (MDIs) mechanical connectors for 100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4 couples the host to the cable assembly. Hosts have six specified MDI connectors: single-lane (SFP112), two-lane (SFP112-DD, DSFP), and eight-lane (QSFP112-DD, OSFP). This enables six host interface types and multiple cable assembly types with different combinations of the connectors at each end. These host and cable assembly types are referred to as form factors, distinguishing both the host receptacle (MDI) and the cable assembly plug. Table 5 lists the MDI types and lane options.

MDI types	100GBASE-CR1	200GBASE-CR2	400GBASE-CR4
SFP112	1	—	—
QSFP112	1, 2, 4	1, 2	1
QSFP112-DD	1, 2, 4, 8	1, 2, 4	1, 2
OSFP	1, 2, 4, 8	1, 2, 4	1, 2
SFP112-DD	1,2	1	—
DSFP	1, 2	1	—

Table 5 – MDIs types and lane options

A subset of the possible cable assembly form factors are provided in Figure 13. The examples are: one-plug to one-plug, one-plug to two-plug, one-plug to four-plug, and one-plug to eight-plug. Cable assembly form factors consisting of any combination of plugs and number of lanes that meet the electrical requirements are acceptable.

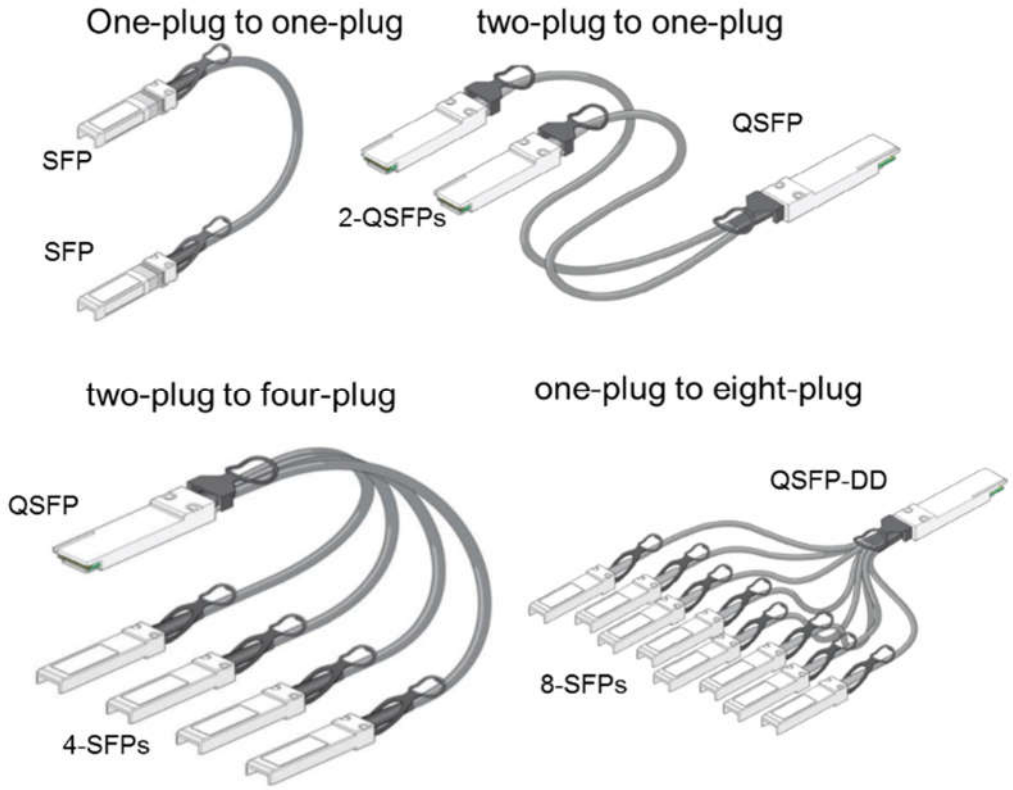


Figure 13 – Host Form Factors

Cable assembly electricals

Channel validation with 2 m 26 AWG cable is demonstrated with positive Channel Operating Margin (COM) for the maximum channel insertion loss with 2 m 26 AWG cable with QSFP-DD host form factor near-end crosstalk and far-end crosstalk paths.

Results are provided for end-to-end channel illustrated in Figure 14 using COM KR configuration file (version 2.75 as modified) in Table 6 and using COM CR configuration file (version 2.75 as modified) and the cable assembly (TP1-TP4) in Table 7. Note that the CR channel insertion loss (≤ 28.5 dB at 26.56 GHz) does not align with KR (≤ 28 dB at 26.56 GHz) as many 802.3ck members would prefer but achieved consensus to adopt.

End-to-End channel model overview;

- Host PCB stack-up is 30 layers, 150 mil thick, with Meg7 material
- Host PCB via stub length is modelled as 7 mil
- Diff pair trace width/spacing is 4.5 mil/8.5 mil
- ASIC package BGA footprint is extracted in HFSS using the same PCB stack-up
- 16 pairs (8 Tx, 8 Rx) QSFP-DD Connector and host PCB footprint and wire termination are solved in HFSS

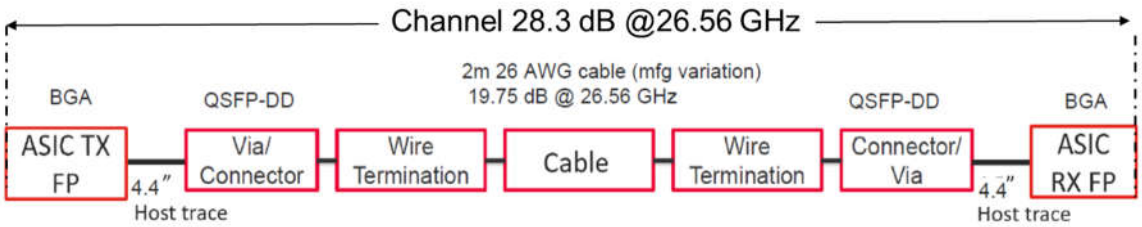


Figure 14 – Channel validation with 2 m 26 AWG cable

COM script version 2.75 for "KR" configuration with channel model in Figure 14.

- Case 1: z_p (TX) = 12 mm; z_p (RX) = 12 mm
- Case 2: z_p (TX) = 31 mm; z_p (RX) = 29 mm
- Floating taps up to 40 UI
- Except set b_max (2..N_b) = 0.3
- Set SNR_TX = 32 dB; eta_0 = 8.2E-9

DUT	Com Case 1 (dB)	Com Case 2 (dB)	ERL11 (dB)	ERL22 (dB)	FOM_{ILD} (dBrms)	ICN (mV)	IL@26.56 GHz TP0-TP5
TP1-TP4 (QSFP-DD, new pair)	4.15	3.24	17.58	16.89	0.37	1.38	28.3
TP1-TP4 (QSFP-DD, legacy pair)	4.85	3.60	15.50	15.26	0.22	1.47	28.0

Table 6 –COM results– KR configuration - 2 m 26 AWG cable

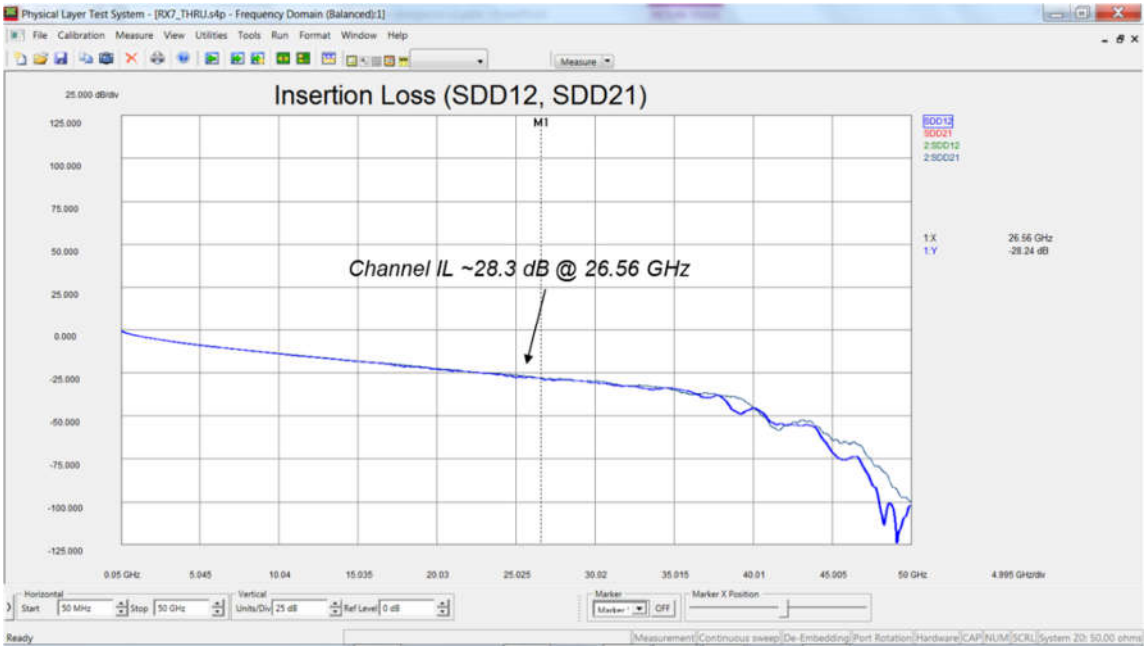


Figure 15 – Channel IL – KR configuration - 2 m 26 AWG cable

COM script version 2.75 for "CR" configuration with TP1-TP4 cable assembly s-parameters and added PCB material as in Figure 7.

- Case 1: z_p (TX) = 12 mm; z_p (RX) = 12 mm
- Case 2: z_p (TX) = 31 mm; z_p (RX) = 29 mm
- Floating taps up to 40 UI
- Include PCB = 1 (4.33 dB @26.56 GHz)
- Except set b_max (2..N_b) = 0.3
- Set SNR_TX = 32 dB; eta_0 = 9.0E-9

DUT	Com Case 1 (dB)	Com Case 2 (dB)	ERL11 (dB)	ERL22 (dB)	FOM_{ILD} (dBrms)	ICN (mV)	IL@26.56 GHz TP1-TP4/ TP0-TP5
TP1-TP4 (QSFP-DD, new pair)	4.55	3.31	16.28	15.47	0.18	0.89	19.8/28.46
TP1-TP4 (QSFP-DD, legacy pair)	4.85	3.60	15.50	15.26	0.22	0.78	19.5/28.16

Table 7 – COM results – CR configuration - 2 m 26 AWG cable

The copper cable assembly specifications are the worst-case transmission requirements specified to support the objective BER. Signaling rate and specification frequency range comparisons between 50GBASE-R PHYs (26.5625 GbD) and 100GBASE-R PHYs (53.125 GBd) are provided in Table 8. The "R" designation refers to the Reed-Solomon Forward Error Correction (RS-FEC) sublayer for the PHYs.

The 100GBASE-CR1,200GBASE-CR2, and 400GBASE-CR4 cable assemblies are specified to provide a point-to-point link segment with a minimum reach of 0.5m (11.08 dB @26.56 GHz) and up to at least 2 m (19.75dB @ 26.56 GHz) between the connector receptacles (MDIs) of the network devices.

All cable assembly measurements between TP1 and TP4 are performed with specified test fixtures illustrated in Figure 16.

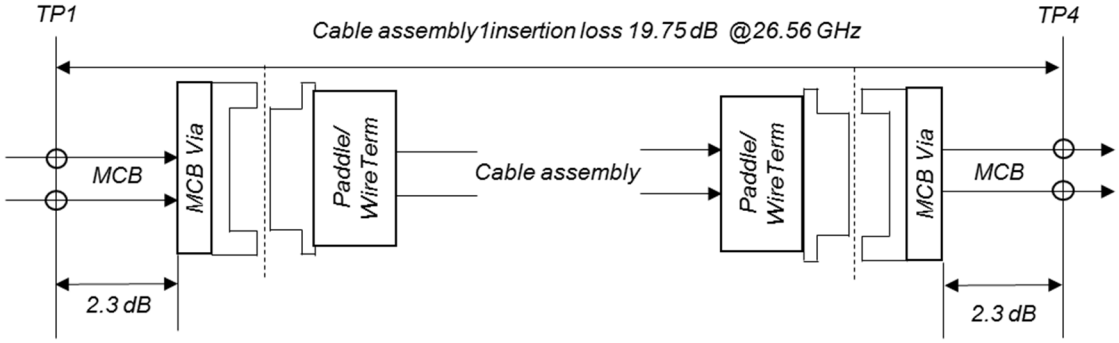


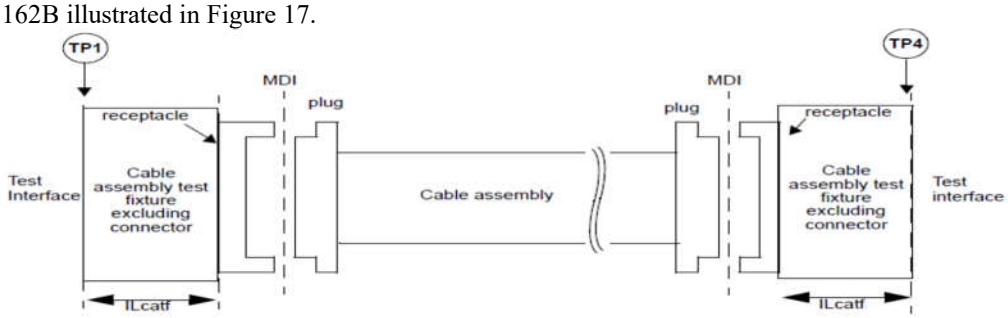
Figure 16 – Cable assembly insertion loss

The differential transmission parameters of the copper cable assembly link segment include maximum insertion loss, minimum insertion loss, minimum return loss, differential to common-mode return loss, differential to common-mode conversion loss and common-mode to common–mode return loss Table 8 lists the cable assembly specifications for differential parameters and the frequency range specified, along with the channel operating margin.

Parameter description	f(GHz)	Unit
Maximum insertion loss (19.75 dB)	@26.56GHz	dB
Minimum Insertion loss (11.08 dB @ 26.56 GHz)	0.05≤f≤38(TBD)	dB
Minimum return loss (not specified)	0.05≤f≤38(TBD)	dB
Cable Assembly ERL ≥ (TBD) for cable assemblies that have a COM < (TBD)		dB
Differential to common-mode conversion loss	0.05≤f≤38(TBD)	dB
Common-mode to common–mode return loss	0.05≤f≤38(TBD	dB
Common-mode to common–mode return loss	0.05≤f≤38(TBD)	dB
Cable assembly Channel Operating Margin (3 dB)		dB

Table 8 – Cable assembly differential specification description

All cable assembly measurements between TP1 and TP4 are performed with the test fixtures specified in Annex 162B illustrated in Figure 17.



Source: IEEE 802.3bj

Figure 17 – Cable assembly measurements

Test Fixture Specifications

The test fixtures used for the transmitter, the receiver, and cable assembly measurements are specified in a mated state to enable connections to measurement equipment as illustrated in 14. The TP2/TP3 test fixture (also known in the industry as Host Compliance Board) is required for measuring the transmitter specifications at TP2 and the receiver return loss at TP3 for the 100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4 host form factors. The cable assembly test fixture (also known in the industry as Module Compliance Board) is required for measuring the cable assembly specifications at TP1 and TP4 for the 100GBASE-CR1, 200GBASE-CR2, and 400GBASE-CR4 host form factors.

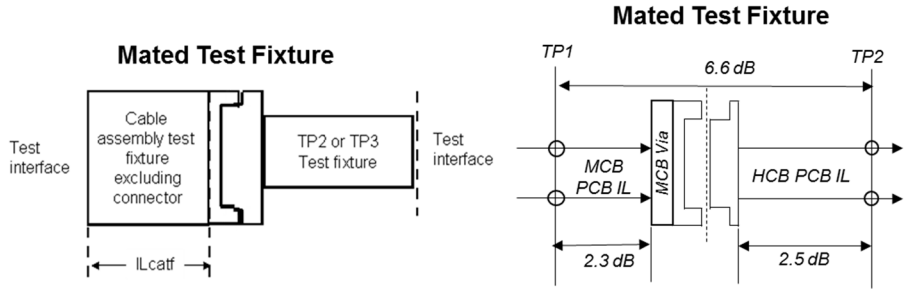


Figure 18 – Mated test fixture measurements

The test fixture specifications apply to all of the MDIs and cable assembly form factors. QSFP112-DD and OSFP support up to eight transmit and eight receive lanes; a total of sixteen differential lanes (thirty two single-ended). Breaking out thirty two single ended connections from inside the HCB cage while maintaining the insertion loss constraint of 2.5 dB @ 26.56 dB is challenging; an example implementation is illustrated in Figure 19.

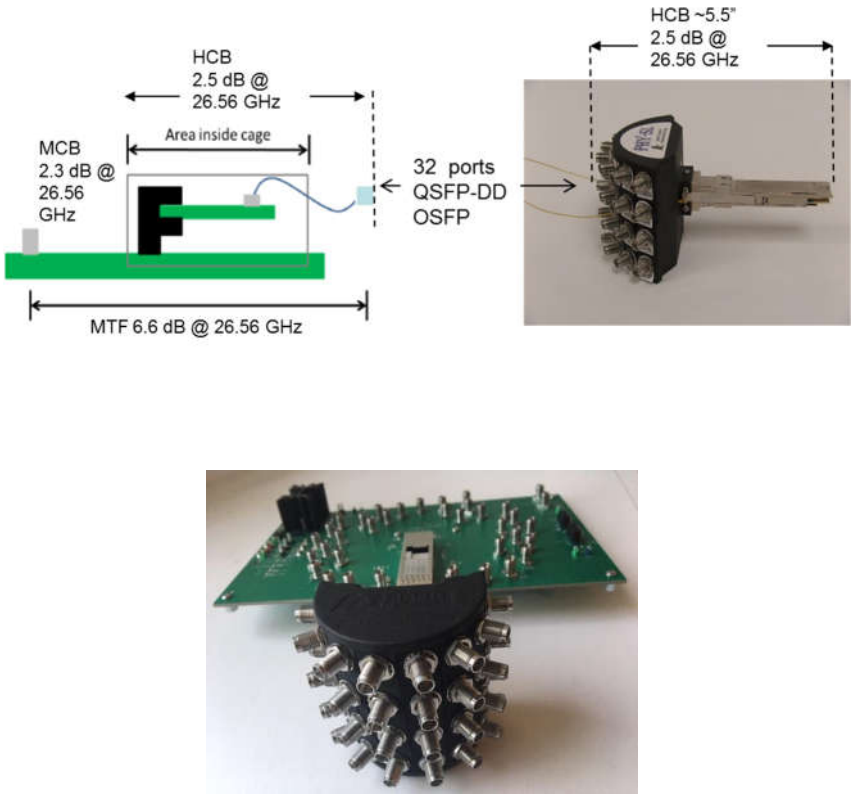


Figure 19 –QSFP-DD/OSFP 32 Port test fixtures

Mated test fixture measurement results are illustrated in Figure 20 that achieve the reference insertion loss of 6.6 dB @26.56 GHz with proposed limits with comparison 50GBASE-R. The figure limits are a proposal for the maximum and minimum insertion loss, which effectively constrains the peak ILD, but is not a proposal for the derived figure of merit insertion loss deviation (FOMILD) from the measurement. The measurement (FOMILD) is 0.2680 dB assuming a bandwidth of 0.75*53.125 GBd, risetime of 6.5 ps and frequency start and stop of 0.01 GHz to 39.84 GHz respectively. The mated test fixture FOM_{ILD} is still under consideration but will likely be less than the 0.2680 dB.

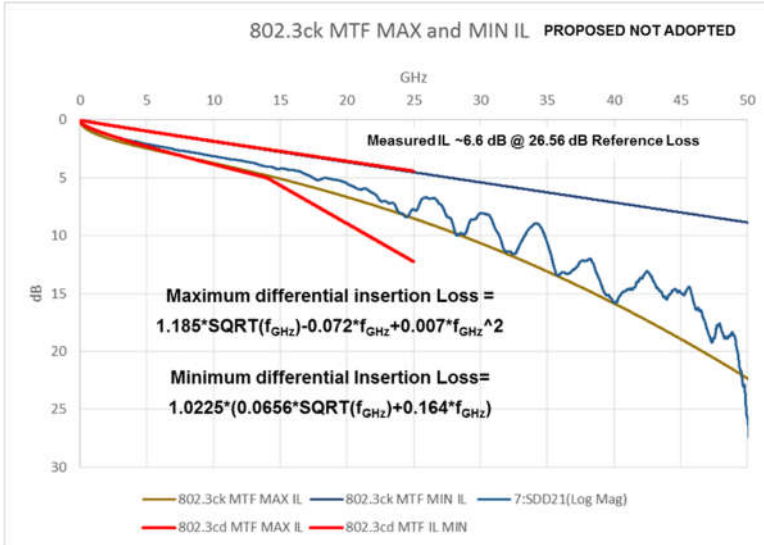


Figure 20 – Mated test fixture measurements

The parameters specified for the mated test fixtures includes insertion loss, return loss, differential to common-mode return loss, differential to common-mode conversion loss, common-mode to common–mode return loss and integrated crosstalk noise (ICN). Table 9 lists the mated test fixture parameters and the frequency range specified where applicable.

Parameter description	**f(GHz)**	**Unit**
Maximum insertion loss	0.01≤f≤40(TBD)	dB
Minimum insertion loss	0.01≤f≤40(TBD)	dB
Minimum return loss	0.01≤f≤40(TBD)	dB
Common-mode conversion insertion loss	0.01≤f≤40(TBD)	dB
Common-mode return loss	0.01≤f≤40(TBD)	dB
Common-mode to differential –mode return loss	0.01≤f≤40(TBD)	dB
Integrated crosstalk noise	(TBD)	

Table 9 – Mated test fixture specifications

Summary

The paper provided a detailed technical overview of the process of validation of achieving 100 Gb/s signaling per electrical lane over 2 meters of passive twinaxial copper cable assemblies utilizing predictive simulation models and measurements. Predictive simulation models include the channel operating margin (COM) and associated parameters as well as s-parameter models for cable assemblies, test fixtures, and channels.

The importance of accurate multiport S-parameter measurements and models for boards, connectors, and cables is paramount. The methodologies outlined in this paper help clarify the confusion and misunderstanding in the specification trade-offs required between transmitter, receiver and interconnect. The connector/cable providers are focused on enabling this methodology by providing adequate models. Measurement and simulation co-design and predictive analysis tools such as COM are now a requirement for predictive system performance.