VITA 57.4 FMC+ Loopback Cards

For VITA 57.4 Applications

Samtec Inc.
520 Park East Boulevard
New Albany, IN 47151-1147
1-800-SAMTEC-9
info@samtec.com
COPYRIGHTS, TRADEMARKS AND PATENTS

Product names used herein are trademarks of their respective owners. All information and material in this publication are property of Samtec, Inc. All related rights are reserved. Samtec, Inc. does not authorize customers to make copies of the content for any use.

Terms of Use

Use of this publication is limited to viewing the pages for evaluation or purchase. No permission is granted to the user to copy, print, distribute, transmit, display in public, or modify the contents of this document in any way.

Disclaimer

The information in this publication may change without notice. All materials published here are "As Is" and without implied or express warranties. Samtec, Inc. does not warrant that this publication will be without error, or that defects will be corrected. Samtec, Inc. makes every effort to present our customers an excellent and useful publication, but we do not warrant or represent the use of the materials here in terms of their accuracy, reliability or otherwise. Therefore, you agree that all access and use of this publication's content is at your own risk.

Updated Documentation

Please visit www.samtec.com to get access to the latest documentation and to ensure that you have the latest version of this document.

NEITHER SAMTEC, INC. NOR ANY PARTY INVOLVED IN CREATING, PRODUCING, OR DELIVERING THIS PUBLICATION SHALL BE LIABLE FOR ANY DIRECT, INCIDENTAL, CONSEQUENTIAL, INDIRECT, OR PUNITIVE DAMAGES ARISING OUT OF YOUR ACCESS, USE OR INABILITY TO ACCESS OR USE THIS PUBLICATION, OR ANY ERRORS OR OMISSIONS IN ITS CONTENT.
1 Abstract

FPGA carrier card developers require easy-to-use options to confirm the operation of the VITA 57.4 FMC+ expansion connector typically found on these platforms. With Samtec’s VITA 57.4 FMC+ Loopback Cards, testing the HSPC and HSPCe interfaces on FPGA carrier cards becomes much easier to manage.

Samtec’s family of VITA 57.4 FMC+ Loopback Cards include the HSPC Loopback Card (REF-197618-01) and the HSPC/HSPCe Loopback Card (REF-197693-01). The VITA 57.4 FMC+ Loopback Cards are ideal for benchtop testing, system debugging, probing, or FPGA development.

Both cards provide FPGA designers an easy to use loopback option for testing low-speed interfaces and high-speed multi-gigabit transceivers on any FPGA development board or FPGA carrier card. It can run system data or BER testing on all channels in parallel. This makes evaluation and development with an FPGA much easier and an ideal substitute for 28 Gbps test equipment.

This paper will explore the following details of the VITA 57.4 FMC+ Loopback Cards:

- Mechanical Dimensions and Assembly Features
- Connector Pin Assignments and Block Diagrams
- Software Reference Designs
- Qualification testing set-up and test results
2 Mechanical Dimensions

Both the HSPC Loopback Card and the HSPC/HSCPe Loopback Card conform to the mechanical dimensions of FMC+ Manual as defined within ANSI/VITA 57.4-2019 Section 3. Specific mechanical dimensions for both cards are highlighted below.

Figure 1 - Mechanical Dimensions for HSPC Loopback Card
Figure 2 - Mechanical Dimensions for HSPC/HSPCe Loopback Card
3 Mechanical Design Features

Since many of the applications that involve VITA 57.4 systems are on highly populated with sensitive components, it is important to have an easy way to access the FMC+ carrier. The FMC+ Loopback Cards provide several mechanical features that ease mating and unmating.

The FMC+ Loopback Cards feature:

1. The FMC+ Loopback cards have been designed to work in conjunction with the Micro Jack Screw Standoff (JSOM).
2. Use JSOMs to carefully mate and unmate the FMC+ Loopback Cards to the FPGA carrier to avoid damages.
3. An Allen-key unscrews and expands the jack screw, dividing the PCBs in a steady, even motion until the mezzanine is safely separated from its host.
4  Connector Pin Assignments

Both the HSPC Loopback Card and the HSPC/HSPCe Loopback Card conform to the Connector Pin Assignments of HSPC and HSPCe connectors as defined within ANSI/VITA 57.4-2019 Section 5. Specific pin assignments for both cards are highlighted below.

---

Figure 3 - HSPC Connector Pin Assignments

---

Figure 4 - HSPCe Connector Pin Assignments
5 Block Diagrams

Both the HSPC Loopback Card and the HSPC/HSCPe Loopback Card provide basic loopback functionality for testing general FPGA carrier cards that contain the HSPC and/or HSPCe interfaces. Each loopback card routes core signals to enable loopback functionality as defined within ANSI/VITA 57.4-2019 Section 5.

Signals routed include:

- Gigabit data signals (MGTs)
- Gigabit reference clocks
- Control lines including JTAG (including IPMI support), I2C, addressing, and reserved signals
- All required power rails, sequencing, and control lines

Specific high-level signal routing for both cards are highlighted below.

![Figure 5 - HSPC Loopback Card Block Diagram]
Additional signal routing and circuitry details are contained in the schematics for both the HSPC Loopback Card and the HSPC/HSPCe Loopback Card. Schematics are available from Samtec under NDA. Please e-mail KitsAndBoards@samtec.com for more details.

6 Software Reference Design

Both the HSPC Loopback Card and the HSPC/HSPCe Loopback Card are pre-programmed with essential firmware and register setting to enable basic functionality. Firmware, register settings and accompanying software documentation are available from Samtec under NDA.

Please e-mail KitsAndBoards@samtec.com for more details.
7 Testing the FMC+ Loopback Cards Transceivers

The HSPC Loopback Card and HSPC/HSPCe Loopback Card have been designed to test low-speed signals and high-speed multi-gigabit transceivers on any FPGA development board or FPGA carrier card with the FMC+ interface.

7.1 Test Setup

General functional testing of power, control and low-speed signal are assumed with a successful power-up of the card. Key testing results are focused on verifying full-speed operation of the MGTs routed via the HSPC connectors.

To determine electrical performance of the HSPC Loopback Card, a Xilinx VCU118 was utilized as the FMC+ carrier along with the two different loopback cards. Test Setup 1 utilizes the HSPC Loopback Card. Test Setup 2 utilizes the HSPC/HSPCe Loopback Card.

![Figure 7 - Test Setup 1 Utilizing the HSPC Loopback Card](image)

![Figure 8 - Test Setup 2 Utilizing the HSPCe Loopback Card](image)
7.2 Testing Results

Test Setup 1 ran over 24 channels and was found to be error free for over 15 hours of testing with a BER < 5.6e-15. There was no pre-emphasis and DFE was enabled for the test. The resulting data in Figure 9.

Figure 9 - Data for Test Setup 1

Test Setup 2 ran over 24 channels and was found to be error free for over 15 hours of testing with a BER < 1e-14. There was no pre-emphasis and DFE was enabled for the test. The resulting data in Figure 10.

Figure 10 - Data for Test Setup 2
8 Conclusions

FPGA carrier card developers require easy-to-use options to confirm the operation of the VITA 57.4 FMC+ expansion connector typically found on these platforms. With Samtec's VITA 57.4 FMC+ Loopback Cards, testing the HSPC and HSPCe interfaces on FPGA carrier cards becomes much easier to manage.

Samtec's family of VITA 57.4 FMC+ Loopback Cards include the HSPC Loopback Card (REF-197618-01) and the HSPC/HSPCe Loopback Card (REF-197693-01). The VITA 57.4 FMC+ Loopback Cards are ideal for benchtop testing, system debugging, probing, or FPGA development.

Both cards provide FPGA designers an easy to use loopback option for testing low-speed interfaces and high-speed multi-gigabit transceivers on any FPGA development board or FPGA carrier card. The FMC+ Loopback Cards have been tested on numerous, popular FPGA evaluation kits and carrier cards. Data rates on the MGTs have been confirmed to 28 Gbps and beyond.

Additional details on can be found at www.samtec.com/kits.