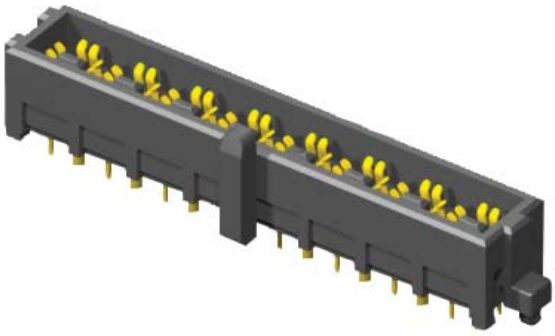
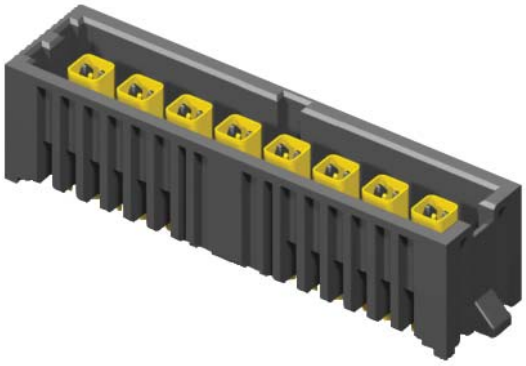
High Speed Characterization Report

IJ5-4-5.0-L-S



Mates with

IP5-4-5.0-L-S



Description:
IsoRate Series, 4.0 mm Centerline
Vertical Board-to-Board, 10mm Stack Height

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Report Revision: 3/16/2010

Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

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Connector Overview

The 4mm (0.157") pitch jack (IJ5) and plug (IP5) provides 1, 2, 4 or 8 positions per row. The IP5/IJ5 Series is a through-hole mount with single and double row options. When mated, the IP5/IJ5 system provides a 10mm (0.394") stack height. The data presented in this report is applicable only to the 4mm pitch; 10 mm stack height IP5/IJ5 Series.

Connector System Speed Rating

IP5/IJ5, 4mm Centerline, Through Hole Vertical

Signaling	Speed Rating
Single-Ended:	**10.5 GHz / 21 Gbps**

The Speed Rating is based on the -3 dB insertion loss point of the connector system. The -3 dB point can be used to estimate usable system bandwidth in a typical, two-level signaling environment.

To calculate the Speed Rating, the measured -3 dB point is used which includes the connector, the connector footprint and approximately 200 mils of test board trace. The resulting loss value is then doubled to determine the approximate maximum data rate in Gigabits per second (Gbps).

For example, a connector with a -3 dB point of 7.8 GHz would have a Speed Rating of 8 GHz/ 16 Gbps. A connector with a -3 dB point of 7.2 GHz would have a Speed Rating of 7.5 GHz/15 Gbps.

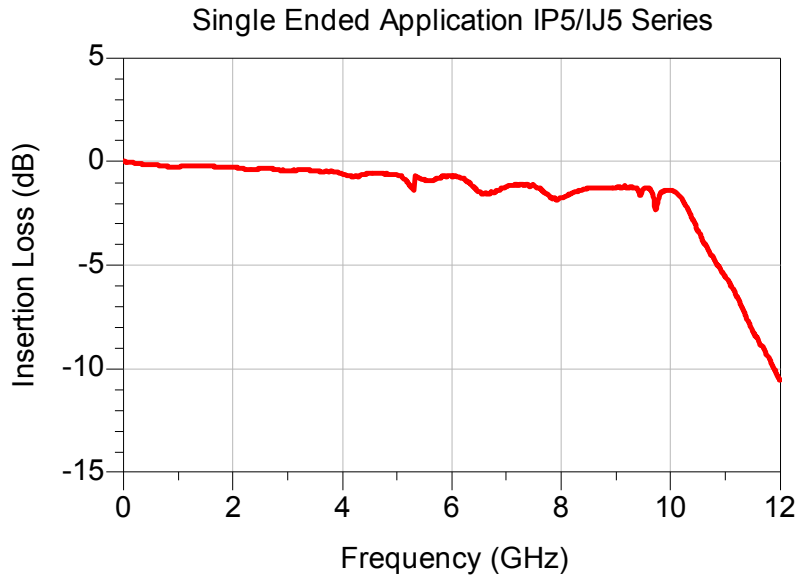
Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

Frequency Domain Data Summary

Table 1 - Single-Ended Signaling System Performance				
Test Parameter	**Test Port**	**Source**	**Victim**	
Insertion Loss	port 1 to port 2	Port 1= TST31 J31-4 Port 2-=TST32 J32-4		-3 dB @10.5 GHz
Return Loss	port 1 to port 2	Port 1= TST31 J31-4 Port 2-=TST32 J32-4		<-10dB to 10.5 GHz
Near-End Crosstalk	port 1 to port 3	TST31 J31-4	TST31 J31-3	<-26 dB to 10.5GHz
		TST31 J31-4	TST31 J31-2	<-29 dB to 10.5 GHz
		TST31 J31-4	TST31 J31-1	<-25 dB to 10.5 GHz
Far-End Crosstalk	port 1 to port 4	TST31 J31-4	TST32 J31-3	<-27 dB to 10.5 GHz
		TST31 J31-4	TST32 J31-2	<-33 dB to 10.5 GHz
		TST31-J31-4	TST32 J31-1	<-24 dB to 10.5 GHz

Bandwidth Chart – Insertion Loss

IJ5/IP5 Series Board-to-Board 10mm Stack Height



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

Time Domain Data Summary

Table 2 - Impedance (Ω) (TST31 J31-4)							
Signal Rise time	**35±5ps**	**50 ps**	**100 ps**	**250 ps**	**500 ps**	**750 ps**	**1 ns**
Maximum Impedance	59	54	52	51	50	50	50
Minimum Impedance	39	42	47	48	50	50	50

Table 3 - Single-Ended Crosstalk (%)							
Input (t_r)		**Source**	**Victim**	**35±5ps**	**50ps**	**100ps**	**250ps**
NEXT	Port 1 to port 3	TST31 J31-4	TST31 J31-3	0.06%	0.037%	0.008%	0.005%
	Port 1 to port 3	TST31 J31-4	TST31 J31-2	0.025%	0.02%	0.0025%	0.004%
	Port 1 to port 3	TST31 J31-4	TST31 J31-1	0.05%	0.035%	0.005%	0.001%
FEXT	Port 1 to port 4	TST31 J31-4	TST32 J31-3	0.06%	0.037%	0.005%	0.002%
	Port 1 to port 4	TST31 J31-4	TST32 J31-2	0.025%	0.015%	0.0025%	0.0006%
	Port 1 to port 4	TST31 J31-4	TST32 J31-1	0.05%	0.035%	0.005%	0,0005%

Table 4 - Propagation Delay			
Configuration		**Signal Path**	Mated Connector + BOR
Single-Ended	Port 1 to Port 2	TST31 J31-4 to TST31 J32-4	176 ps

Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

Characterization Details

This report presents data that characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the connector and footprint effects on a typical multi-layer PCB. PCB effects (trace loss) are de-embedded from test data. Board related effects, such as pad-to-ground capacitance, are included in the data presented in this report.

Additionally, intermediate test signal connections can mask the connectors' true performance. Such connection effects are minimized by using high performance test cables, adapters, and microwave probes. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented only for single-ended drive scenarios, as this is the target application for the IJ5/IP5 connector.

Frequency Domain Data

Frequency domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the frequency domain are insertion loss, return loss, and near-end and far-end crosstalk. Other parameters or formats, such as VSWR or S-parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated directly from network analyzer measurements.

Time Domain Data

Time Domain parameters indicate impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. The measured S-parameters from the network analyzer are post-processed using Agilent Advanced Design System to obtain the time domain response. Time Domain data is provided in Appendix E of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

Reference plane impedance is 50 ohms for single-ended measurements and 100 ohms for differential measurements. The fastest rise time signal exciting the SUT is 35 ± 5 picoseconds.

In this report, propagation delay is defined as the signal propagation time through the connector and connector footprint. It includes 200mils of PCB trace n each end of the connector. Delay is measured at 35 ± 5 picoseconds signal rise time. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Crosstalk data in this report is labeled as "4-3", "4-2 "or "4-1". The IP5/IJ5 connector tested in this report has 4 positions. A "4-3" crosstalk configuration excites position 4 and monitors the coupled noise on position 3. Position 4 is at the end of the connector and position 3 is directly adjacent.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. However, modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

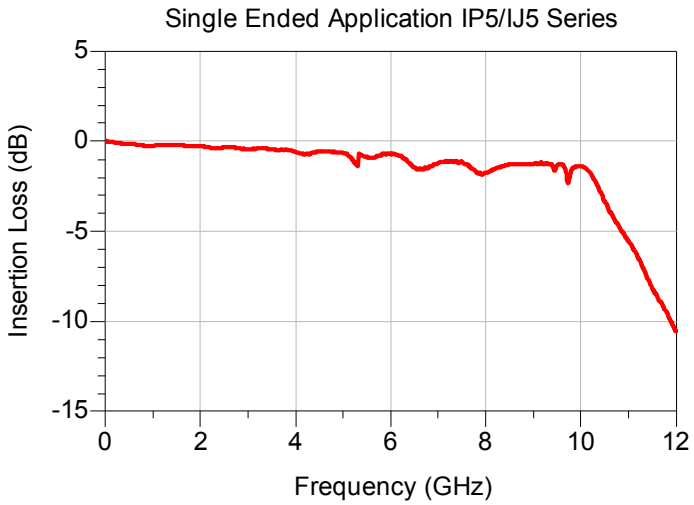
Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

Appendix A – Frequency Domain Response Graphs

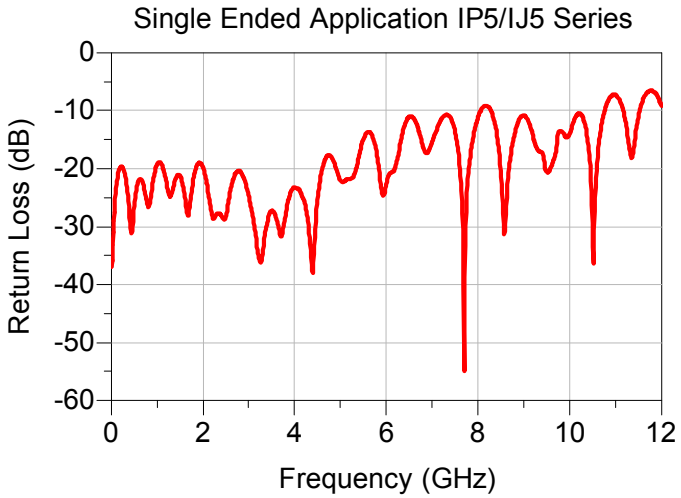
Single-Ended Application – Insertion Loss

Configuration: port 1=J31-4 , port 2=J32-4



Single-Ended Application – Return Loss

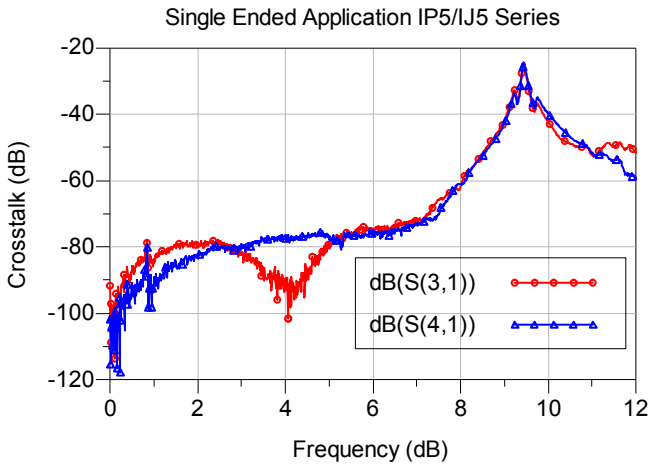
Configuration: port 1=J31-4



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

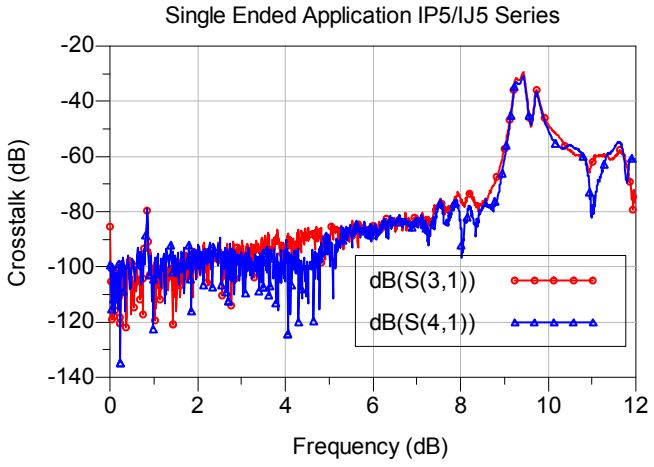
Single-Ended Application – NEXT and FEXT, "4-3" Configuration

S31=NEXT, port 1 (TST31 J31-4) to port 3 (TST31 J31-3)
S41=FEXT, port 1 (TST31 J31-4) to port 4 (TST32 J31-3)



Single-Ended Application – NEXT and FEXT, "4-2" Configuration

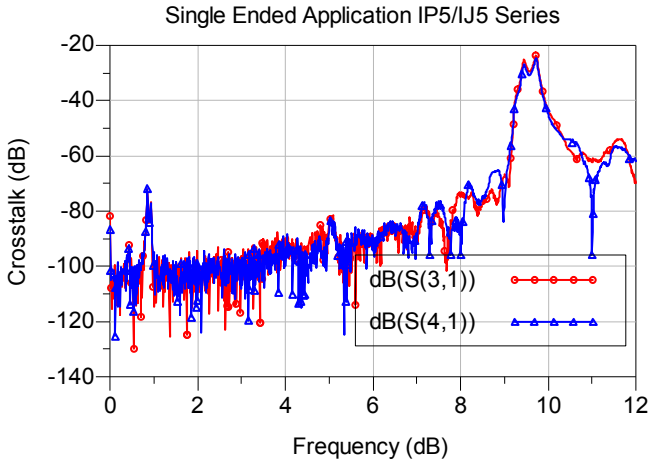
S31=NEXT, port 1 (TST31 J31-4) to port 3 (TST31 J31-2)
S41=FEXT, port 1 (TST31 J31-4) to port 4 (TST32 J31-2)



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

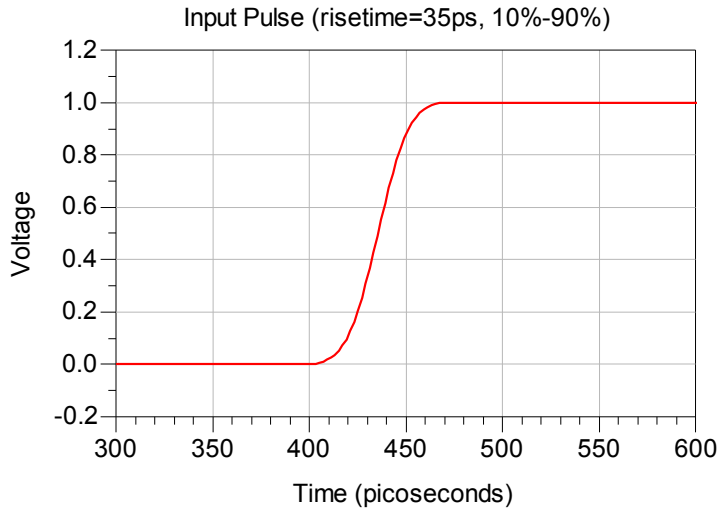
Single-Ended Application – NEXT and FEXT, "4-1" Configuration

S31=NEXT, port 1 (TST31 J31-4) to port 3 (TST31 J31-1)
S41=FEXT, port 1 (TST31 J31-4) to port 4 (TST32 J31-1)



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

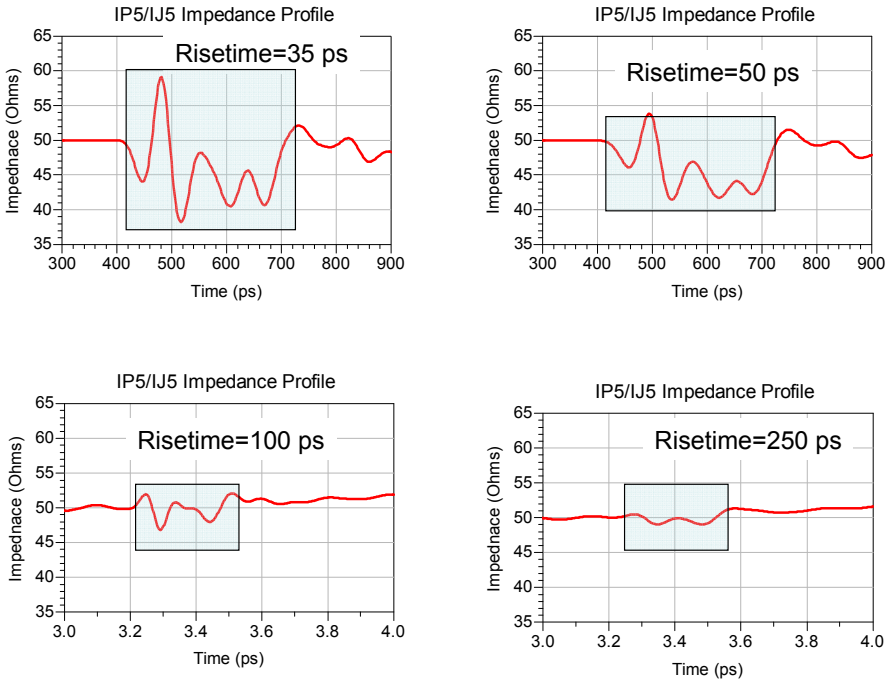
Appendix B – Time Domain Response Graphs
Single-Ended Application – Input Pulse



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

Single-Ended Application – Impedance

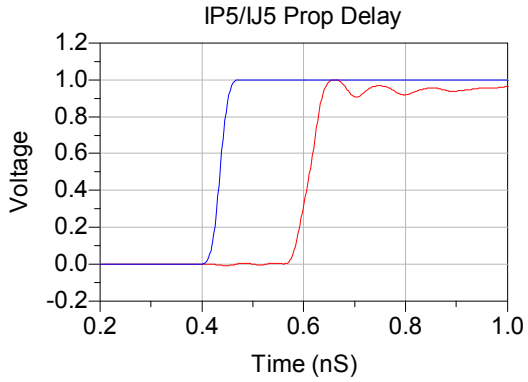
Configuration: port 1=J31-4, port 2=J32-4, port 3=J31-3, port 4=J32-3



Risetime is 10%-90%
Highlighted region is connector and footprint

Single-Ended Application – Propagation Delay

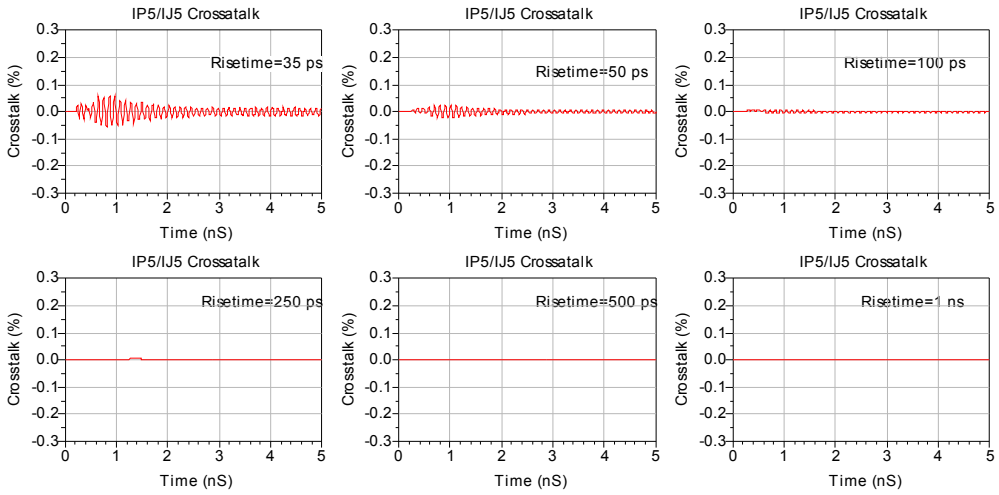
Configuration: port 1=J31-4, port 2=J32-4, port 3=J31-3, port 4=J32-3



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

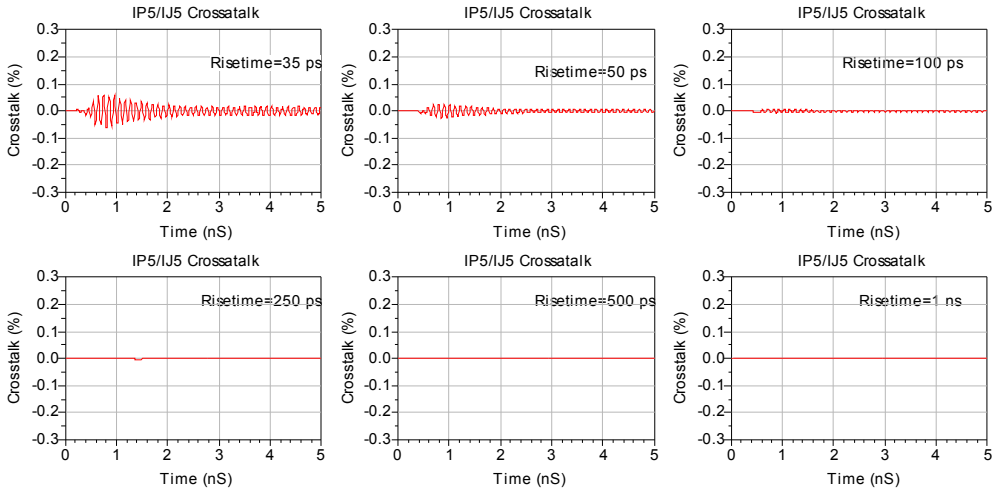
Single-Ended Application – NEXT, "4-3" Configuration

Configuration: port 1=J31-4, port 2=J32-4, port 3=J31-3, port 4=J32-3



Single-Ended Application – FEXT, "4-3" Configuration

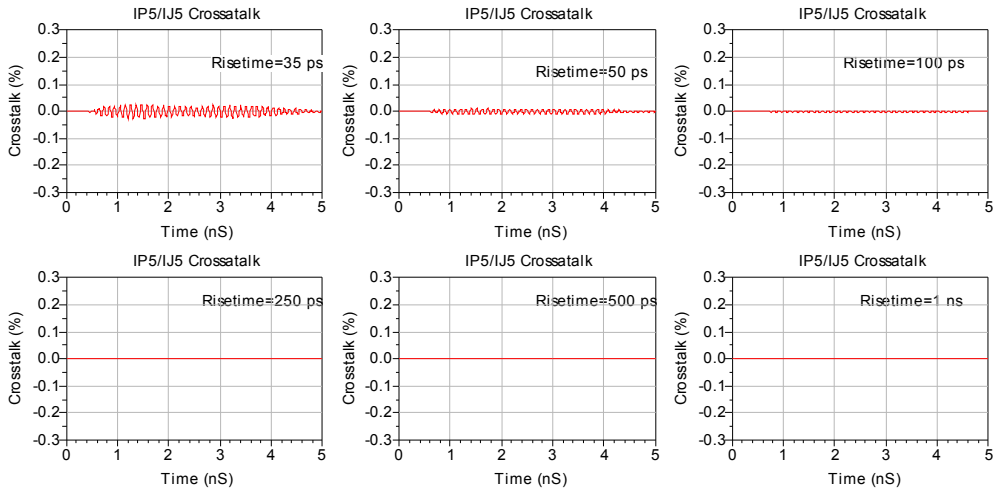
Configuration: port 1=J31-4, port 2=J32-4, port 3=J31-3, port 4=J32-3



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

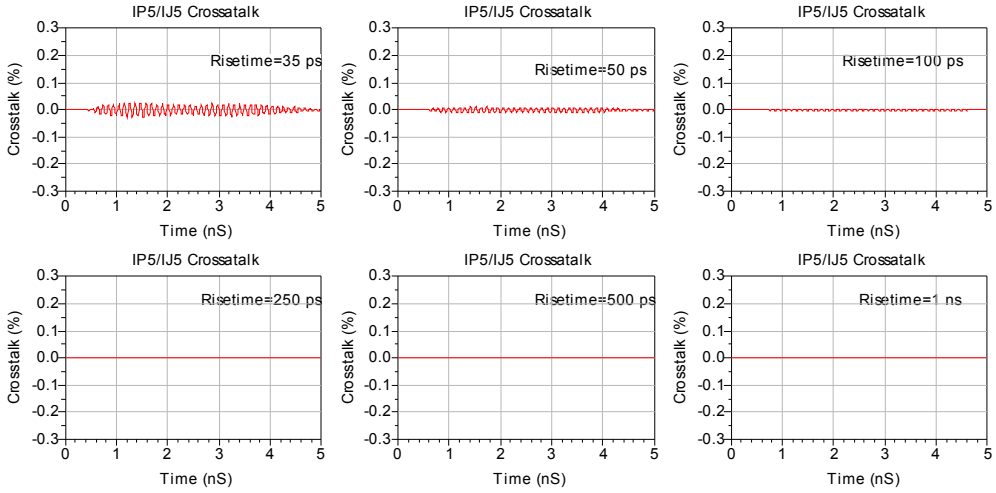
Single-Ended Application – NEXT, "4-2" Configuration

Configuration: port 1=J31-4, port 2=J32-4, port 3=J31-2, port 4=J32-2



Single-Ended Application – FEXT, "4-2" Configuration

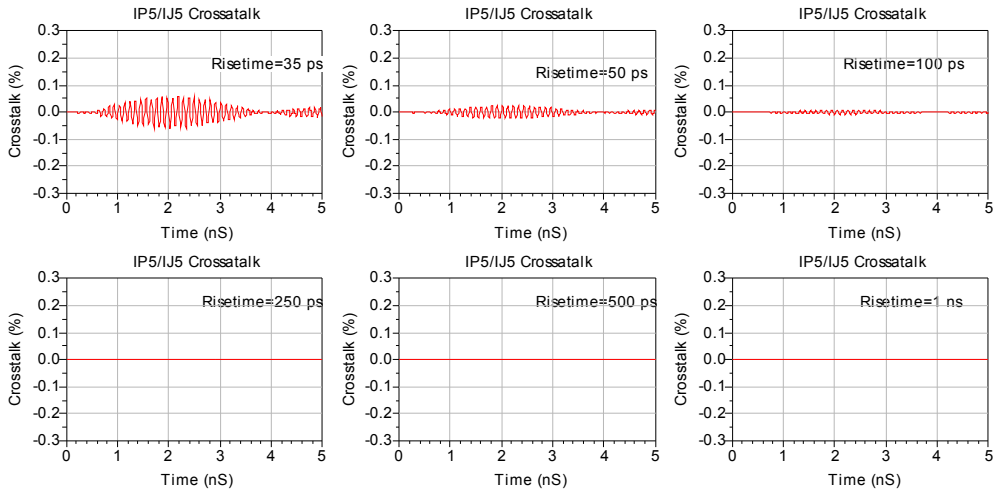
Configuration: port 1=J31-4, port 2=J32-4, port 3=J31-2, port 4=J32-2



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

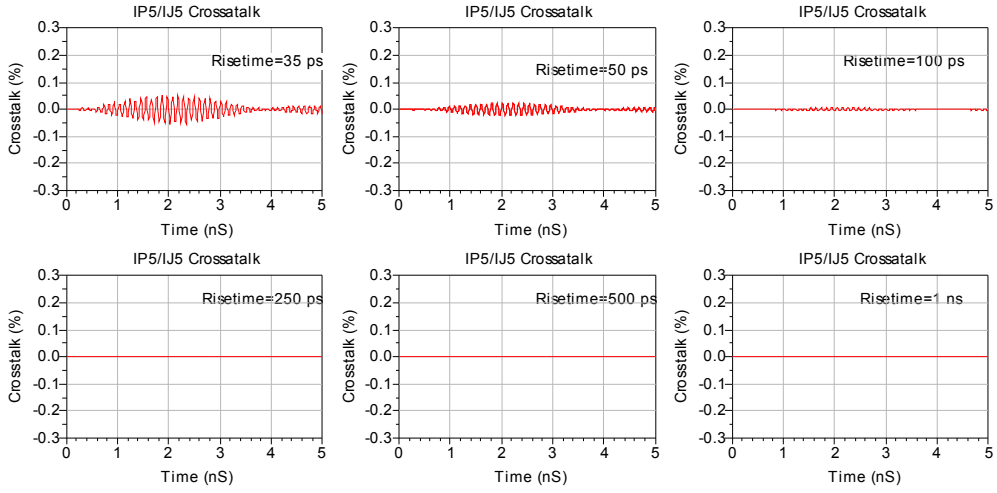
Single-Ended Application – NEXT, "4-1" Configuration

Configuration: port 1=J31-4, port 2=J32-4, port 3=J31-1, port 4=J32-1



Single-Ended Application – FEXT, "4-1" Configuration

Configuration: port 1=J31-4, port 2=J32-4, port 3=J31-1 port 4=J32-1



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

Appendix C – Product and Test System Descriptions

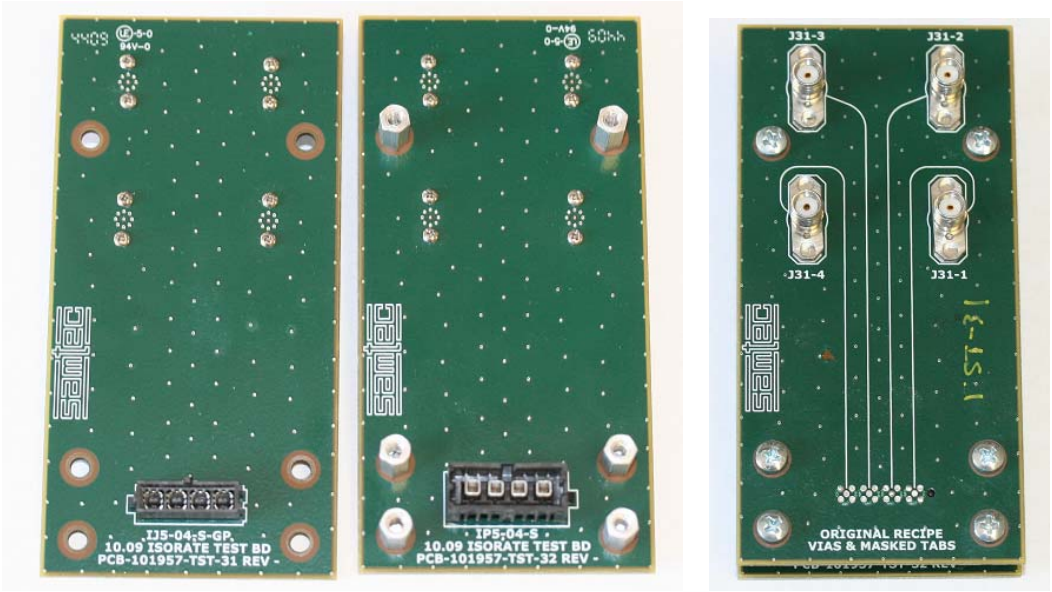
Product Description

Product test samples are the IJ5 jack, part number IJ5-04-05.0-L-S-1-TR and the plug part number IP5-04-05.0-L-S-1-TR. The connector parts are PCB surface mount. When mated a 10mm (.1575") stack height exists between the PCB connector mounted surfaces. Each connector structure consists of one row of coaxial connectors. Center contacts are evenly spaced at a 4mm (.1575") pitch.

Test System Description

The test fixtures are composed of 6-layer FR-4 material with 50Ω signal trace and pad configurations designed for the electrical characterization of Samtec hi-speed connector products. The test fixtures are specific to the IJ5/IP5 connector series and identified by part numbers PCB-101957-TST-31 and PCB-101957-TST-32. Odd numbered boards 31 serve as the signal launch board and terminate to the specified IP5 plug connector product. Even numbered fixtures 32, terminate to the specified IJ5 connector product. Electrical continuity exists between all the labeled test points when board numbers 31 & 32 are mated. Reference plane and calibration standards specific to the IJ5/IP5 series are located on the calibration board IP5/IJ5, PCB-101957-TST-99. All data and wave-forms presented are results from an IP5 plug side launch. Pictured on page13 and 14 are the mated test samples and a printed circuit board layout panel.

PCB-101957-TST –XX Test Fixtures



Series: IJ5/IP5
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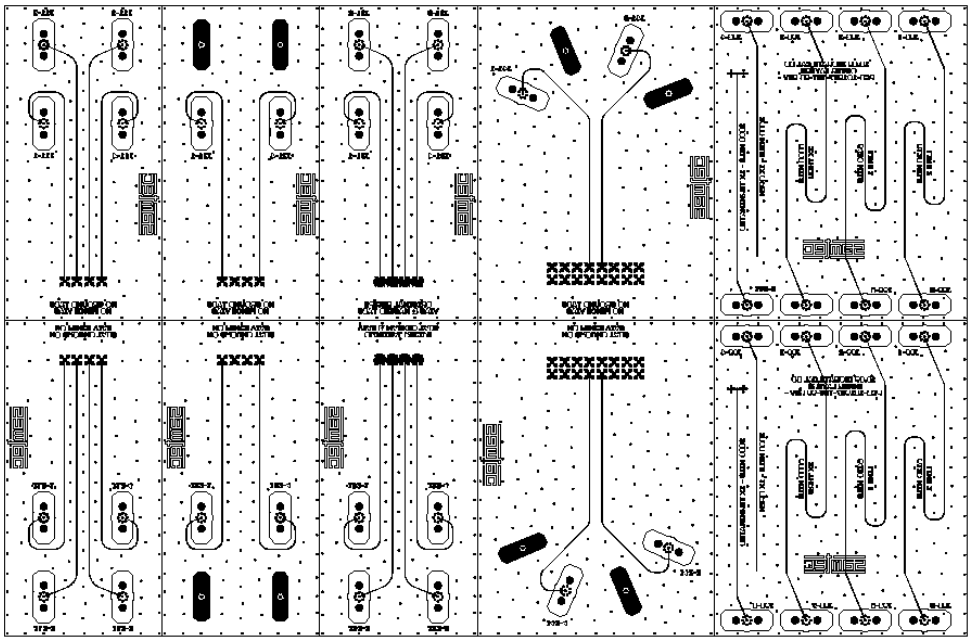
PCB-101957-TST PCB Layout Panel



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

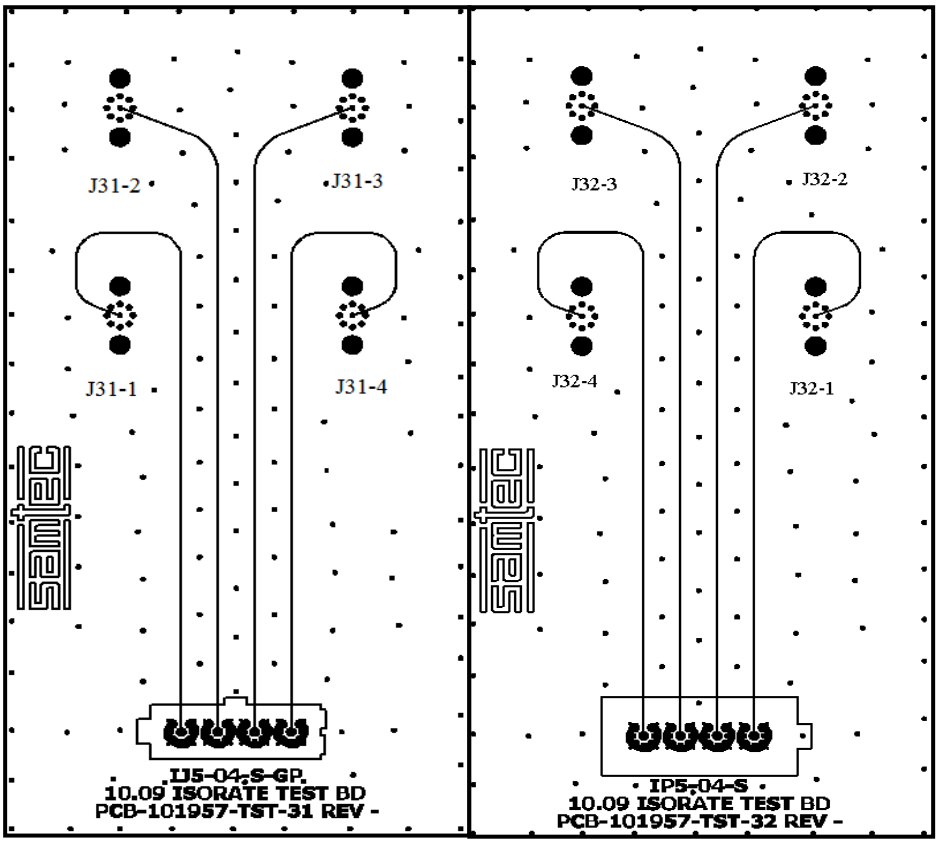
PCB Fixture Set I

Fixture Identity

PCB-101957-TST-32 Rev – IP5 Test Board
PCB-101957-TST-31 Rev – IJ5 Test Board

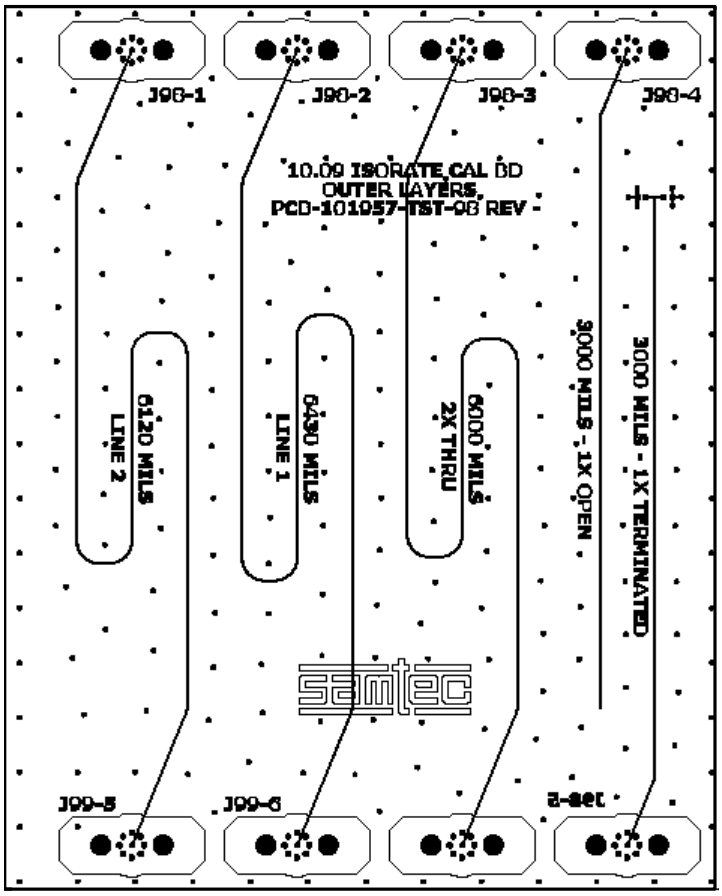
Crosstalk Test Parameters – TD NEXT, TD NEXT, FD FEXT, TD FEXT,

4-3, Single-Ended
Near-End Aggressor: J31-4, Victim; J31-3
Far-End Aggressor: J31-4, Victim; J32-3
4-2, Single-Ended
Near-End Aggressor: J31-4, Victim; J31-2
Far-End Aggressor: J31-4, Victim; J32-2
4-1, Single-Ended
Near-End Aggressor: J31-4, Victim; J31-1
Far-End Aggressor: J31-4, Victim; J32-1



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

Calibration Board



Thru line – 6000 mils
Open Reflect – 3000 mils
Line 1 – 6430 mils
Line 2 – 6120 mils

Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

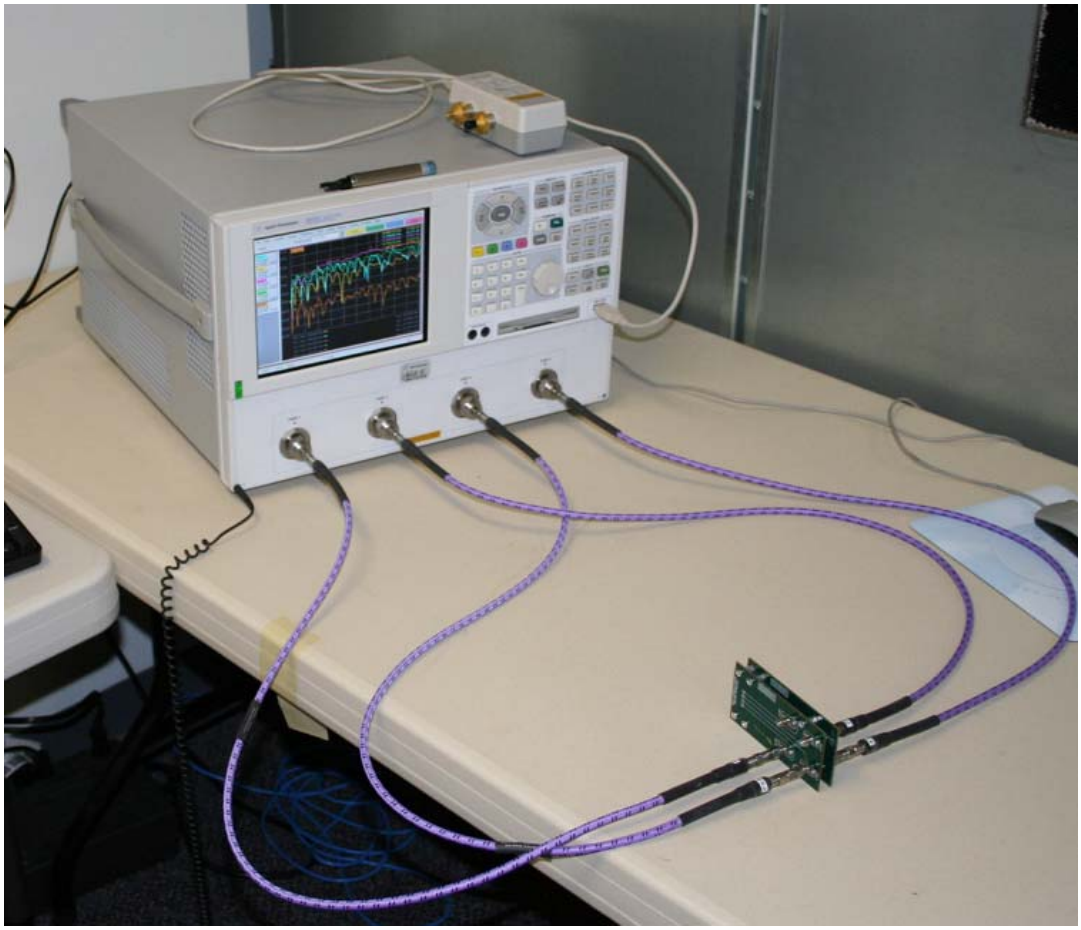
Appendix D – Test and Measurement Setup

The test instrument is the Agilent N5230A PNA-L network analyzer. Frequency domain data and graphs are obtained directly from the instrument. Post-processed time domain data and graphs are generated using convolution algorithms within Agilent ADS. The network analyzer is configured as follows:

Start Frequency – 300 KHz
Stop Frequency – 16 GHz
Number of points -1601
IFBW – 100 Hz

With these settings, the measurement time is approximately 5 minutes.

N5230A Measurement Setup



Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

Test Instruments

QTY	Description
1	Agilent N5230A PNA-L Network Analyzer (300 KHz to 20 GHz)
1	Agilent N4433A ecal module (300 KHz to 20 GHz)

Test Cables & Adapters

QTY	Description
4	WL Gore Phaseflex Test Cables

Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

Appendix E - Frequency and Time Domain Measurements

Frequency (S-Parameter) Domain Procedures

The quality of any data taken with a network analyzer is directly related to the quality of the calibration standards and the use of proper test procedures. For this reason, extreme care is taken in the design of the LRM calibration standards, the SI test boards and the selection of the PCB vendor.

The measurement process begins with a measurement of the LRM calibration standards. A coaxial SOLT calibration is performed using an N4433A ecal module. This measurement is required in order to obtain precise values of the line standard offset delay and frequency bandwidths. Measurements of the reflect and 2x through line standard can be used to determine the maximum frequency for which the calibration standards are valid. For the IP5/IJ5 test boards this is roughly 16 GHz.

From the LRM calibration standard measurements, a user defined calibration kit is developed and stored in the network analyzer. Calibration is then performed on all 4 ports following the calibration wizard within the Agilent N5230. This calibration is saved and can be recalled at any time. Calibration takes roughly 30 minutes to perform.

Time Domain Procedures

Mathematically, frequency domain data can be transformed to obtain a time domain response. Perfect transformation requires frequency domain data from DC to infinity Hz. Fortunately, a very accurate time domain response can be obtained with bandwidth-limited data, such as measured with modern network analyzer.

The time domain responses were generated using Agilent ADS 2009 update 1. This tool has a transient convolution simulator that can generate a time domain response directly from measured S-parameters. An example of a similar methodology is provided in the Samtec Technical Note on domain transformation
http://www.samtec.com/Technical_Library/reference/articles/pdfs/tech-note_using-PLTS-for-time-domain-data_web.pdf

Impedance (TDR)
A step pulse is applied to the touchstone model of the connector and the reflected voltage is monitored. The reflected voltage is converted to a reflection coefficient and then transformed into an impedance profile. All ports of the Touchstone model are terminated in 50 ohms.

Series: IJ5/IP5
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Propagation Delay (TDT)

The propagation delay is a measure of the time domain delay through the connector and footprint. A step pulse is applied to the touchstone model of the connector and the transmitted voltage is monitored. The same pulse is also applied to a reference channel with zero loss and the time domain pulses are plotted on the same graph. The difference in time, measured at the 50% point of the step voltage is the propagation delay.

Near-End Crosstalk (TDT) & Far End Crosstalk (TDT)

A step pulse is applied to the touchstone model of the connector and the coupled voltage is monitored. The amplitude of the peak-coupled voltage is recorded and reported as a percentage of the input pulse.

Series: IJ5/IP5
Description: IsoRate, 4.0mm (.157") Pitch, 10mm (.397") Stack Height

Appendix F – Glossary of Terms

TD – Time Domain
FD – Frequency domain
DUT – Device under test, term used for TDA IConnect & Propagation Delay waveforms
EC6 – Edge Card with a .635mm signal pad pitch
FEXT – Far-End Crosstalk
GSG – Ground–Signal-Ground; geometric configuration
GSSG - Ground–Signal-Signal-Ground; geometric configuration
LEC6 – Signal Launch Edge Card with a .635 mm signal pad pitch
NEXT – Near-End Crosstalk
PCB – Printed Circuit Board
SE – Single-Ended
SI – Signal Integrity
SUT – System Under Test
TDR – Time Domain Reflectometry
TDT – Time Domain Transmission
WC – Worst Case crosstalk configuration
BC – Best Case crosstalk configuration
Z – Impedance (expressed in ohms)
OV – Optimal Vertical
OH – Optimal Horizontal
HDV – High Density Vertical
PPO – Pin Population Option
S – Static (independent of PCB ground)