ASP-129637-03 (QMS) + ASP-129646-03 (QFS)

PCIe GEN 2 AND GEN 3

CHANNEL CHARACTERIZATION USING

RTD'S "DIVER 2" TEST PLATFORM

REVISION DATE: 02/21/2012

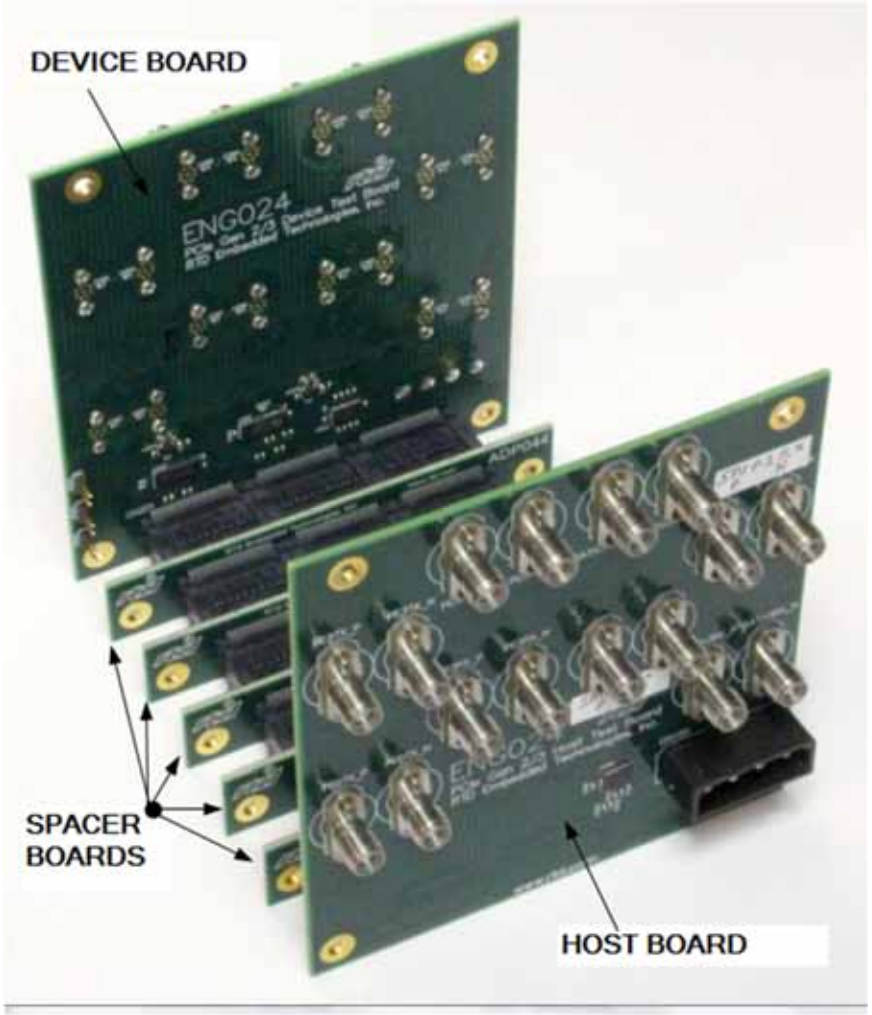
PROJECT SCOPE

- Several years back, QMS/QFS 0.6” mated stack height connectors (reference http://www.samtec.com/search/pc104_new.Aspx?s=ind#PC104EXPRESS) were qualified for use with PCIe Gen 1. This qualification enabled the PC/104 Express specification to proceed. We are now at the point where PCIe Gen 2 and Gen 3 need to be characterized. This qualification was done using a test fixture referred to as “Diver”.

- To perform this characterization, RTD (www.rtd.com) developed a revised test fixture, referred to herein as “Diver 2”. The Diver 2 Test Fixture is defined in RTD document “Diver2_Test-Specification.docx”

DIVER 2 TEST PLATFORM

- The Diver 2 Test Platform is made up of the following:



DIVER 2 TEST PLATFORM

- The Diver 2 Test Platform contains 8 “test paths”
  - 2 for PCIe Gen 2
  - 2 for PCIe Gen 3
  - 4 for SATA

Test Path	Signal Name	Host Signal Switch	Device Signal Switch
A	PE0TX	None	PI2PCIE2452
B	PE0RX	None	PI2PCIE2452
C	PE3TX	None	MAX4889A/PI3PCIE3412
D	PE3RX	None	MAX4889A/PI3PCIE3412
E	SATA0TX	None	None
F	SATA0RX	None	MAX4888C
G	SATA1TX	MAX4888C	MAX4888C
H	SATA1RX	MAX4888C	None

- Each Host trace shall be 6” +/- 0.050” in length and have 6 vias, plus the via at the RF connector.
- Each Device trace shall be 4” ” +/- 0.050” in length and have 6 vias, plus the via at the RF connector.
- Length matching within a differential pair shall be +/- 0.010”.
- There is no “Shifting” between the Host test board and the Device test board. Only non-shifting spacers shall be used.
- The Host shall have bus connectors on both top and bottom, with all pins connected. Only the bottom connector shall be populated.

TEST TOPOLOGIES

- The scope of this project was to focus on the PCIe test paths.
  - PCIe Gen 2 test path highlighted in yellow
  - PCIe Gen 3 test path highlighted in blue
  - Configurations using 3, 5, and 9 spacer boards were characterized

Test ID	Spacers	Test Path	Data Rate Goal	Signal Name	Host Signal Switch	Device Signal Switch
D2-5-A		A	5 Gbps	PE0TX	None	PI2PCIE2452
D2-5-C1		C	5 Gbps	PE3TX	None	MAX4889A
D2-5-C2	5	C	8 Gbps	PE3TX	None	PI3PCIE3412
D2-5-E		E	8 Gbps	SATA0TX	None	None
D2-5-F		F	8 Gbps	SATA0RX	None	MAX4888C
D2-5-G		G	8 Gbps	SATA1TX	MAX4888C	MAX4888C
D2-9-A		A	5 Gbps	PE0TX	None	PI2PCIE2452
D2-9-C1		C	5 Gbps	PE3TX	None	MAX4889A
D2-9-C2	9	C	8 Gbps	PE3TX	None	PI3PCIE3412
D2-9-E		E	8 Gbps	SATA0TX	None	None
D2-9-F		F	8 Gbps	SATA0RX	None	MAX4888C
D2-9-G		G	8 Gbps	SATA1TX	MAX4888C	MAX4888C
D2-3-A		A	5 Gbps	PE0TX	None	PI2PCIE2452
D2-3-C1		C	5 Gbps	PE3TX	None	MAX4889A
D2-3-C2	3	C	8 Gbps	PE3TX	None	PI3PCIE3412
D2-3-E		E	8 Gbps	SATA0TX	None	None
D2-3-F		F	8 Gbps	SATA0RX	None	MAX4888C
D2-3-G		G	8 Gbps	SATA1TX	MAX4888C	MAX4888C

MEASUREMENT AND SIMULATION

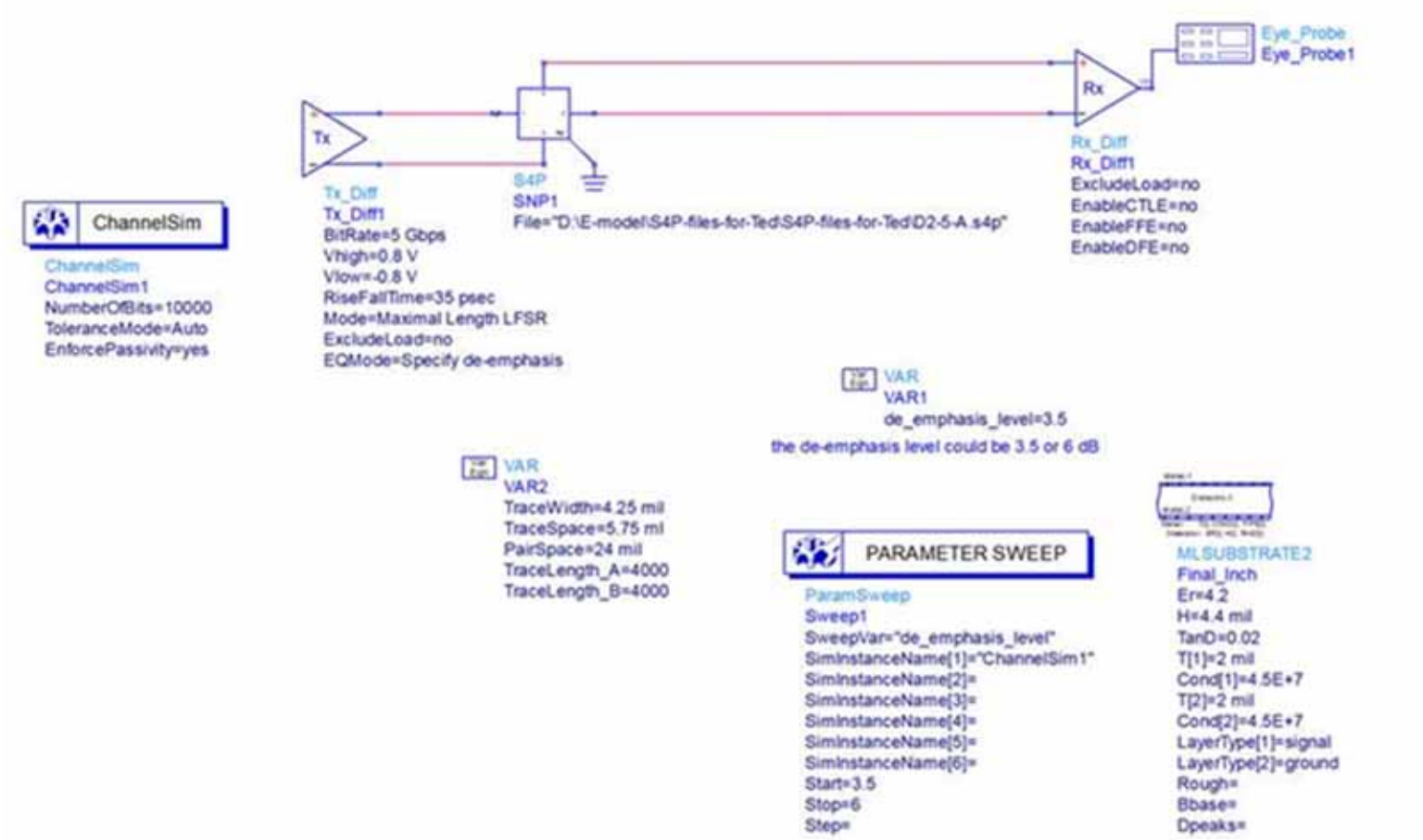
- Measurements were taken using an Agilent PLTS E8364B Signal Analyzer
  - 4-port, 10 MHz – 20 GHz

- 4-port Touchstone files were extracted using Agilent PLTS Model Extraction and Simulation Software Suite

- Channel simulations performed using Agilent ADS

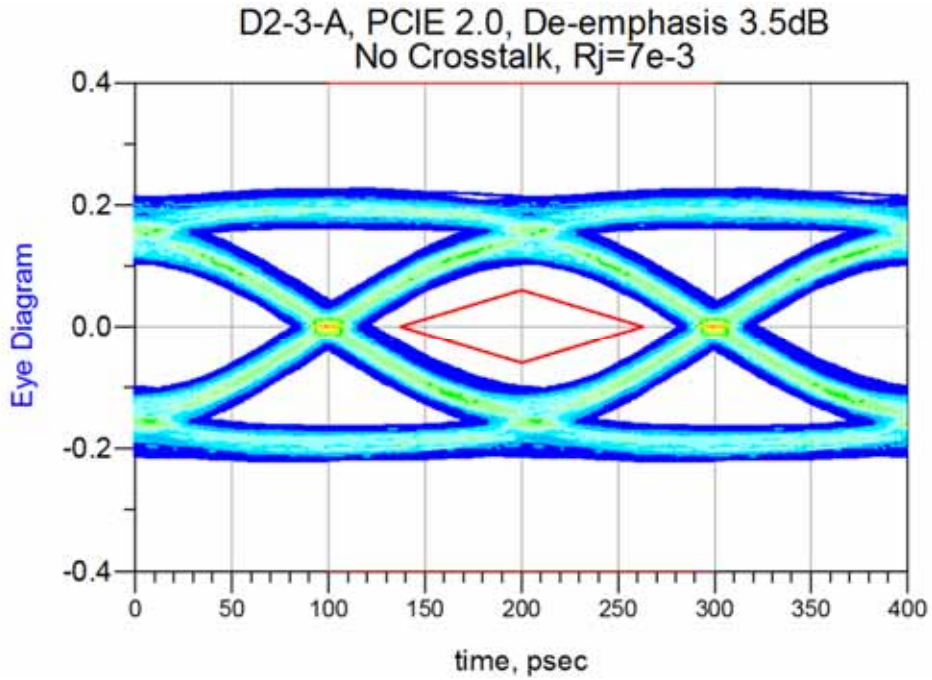
AGILENT ADS DESIGN TEMPLATE

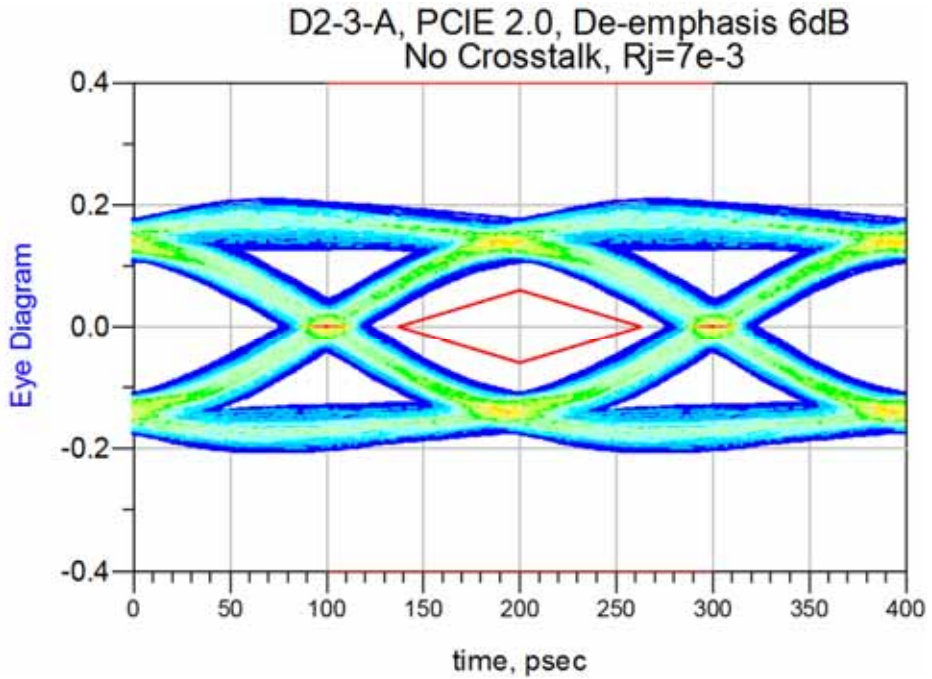
- PCIe Gen 2 (5 Gbps)
  - Since model is S4P (only one diff pair), crosstalk removed from the channel analysis.



CHANNEL SIMULATION RESULTS

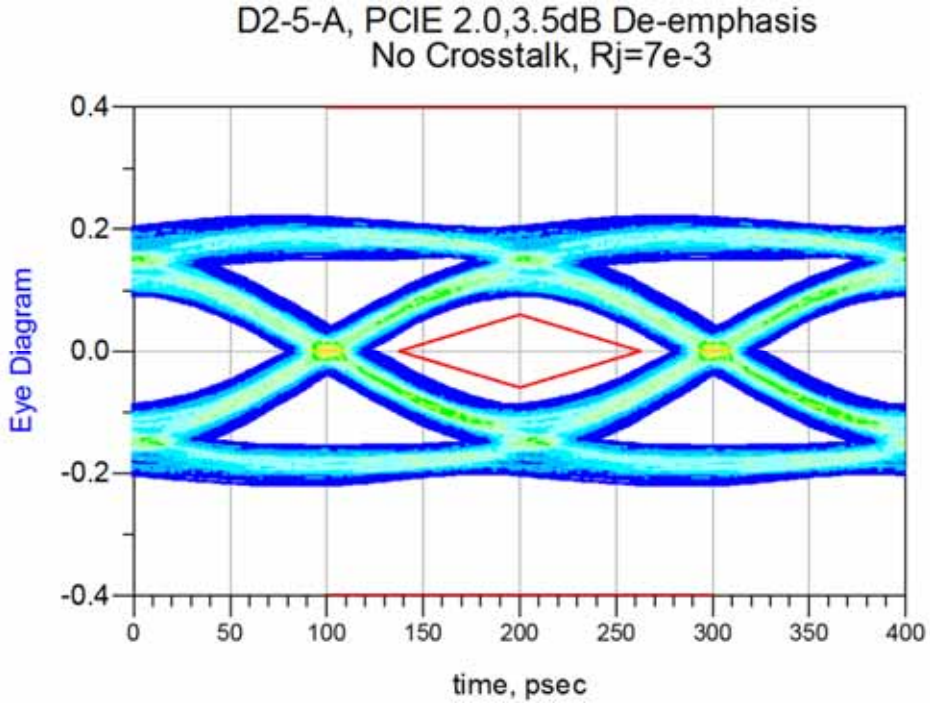
D2-3-A: PCIE 2.0, 5Gbps

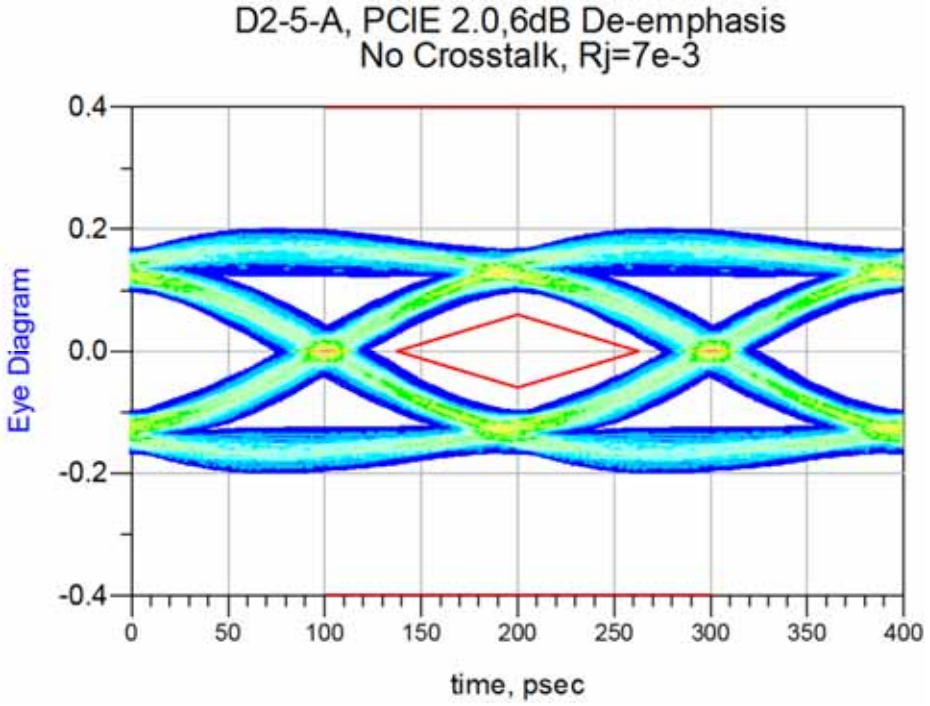




CHANNEL SIMULATION RESULTS

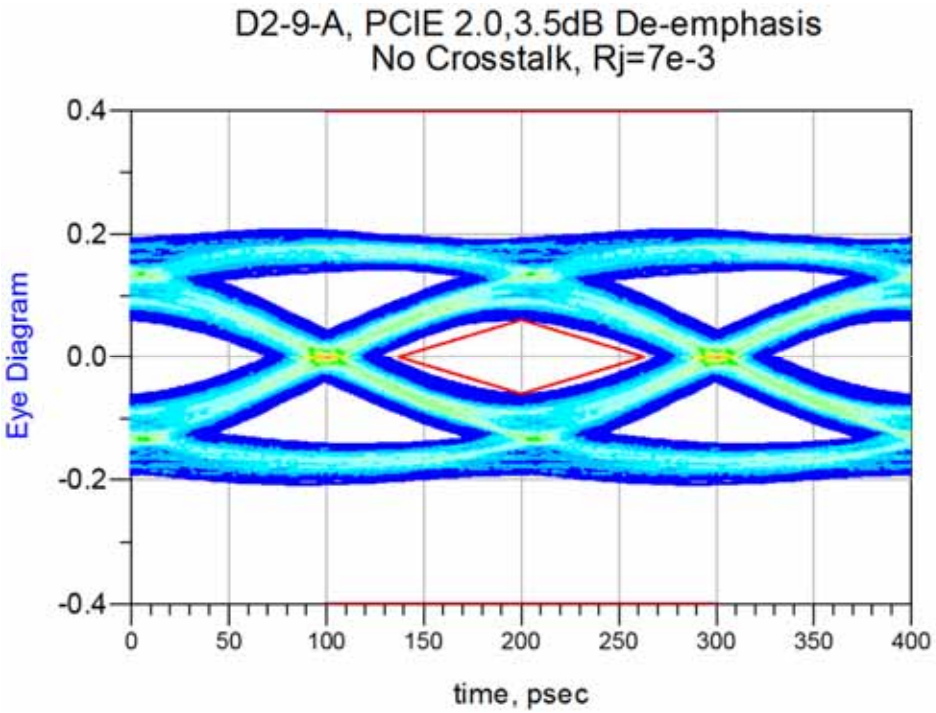
D2-5-A: PCIE 2.0, 5Gbps

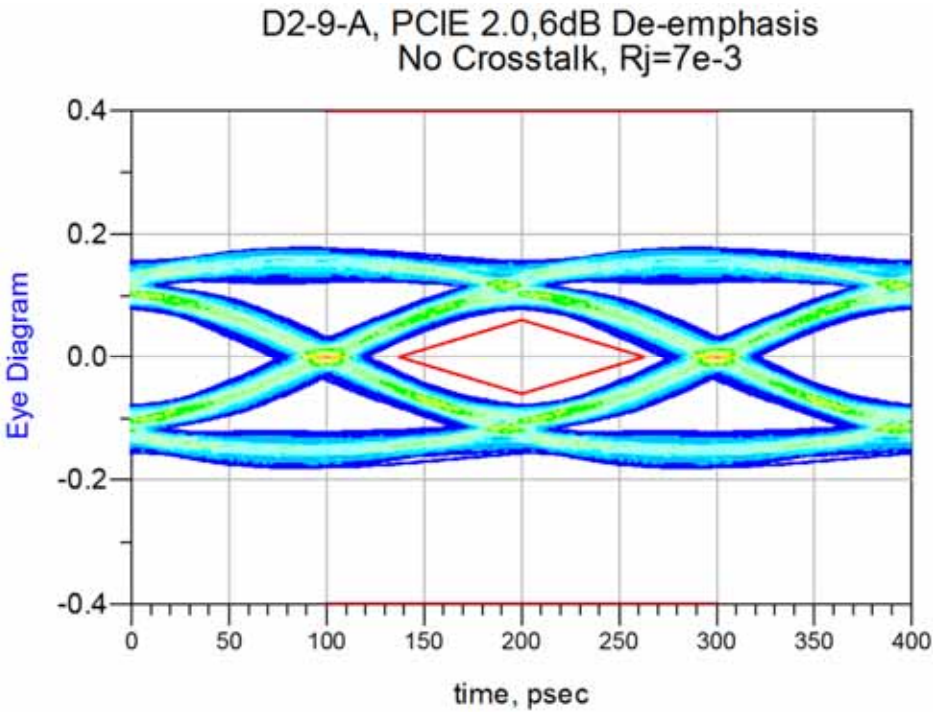




CHANNEL SIMULATION RESULTS

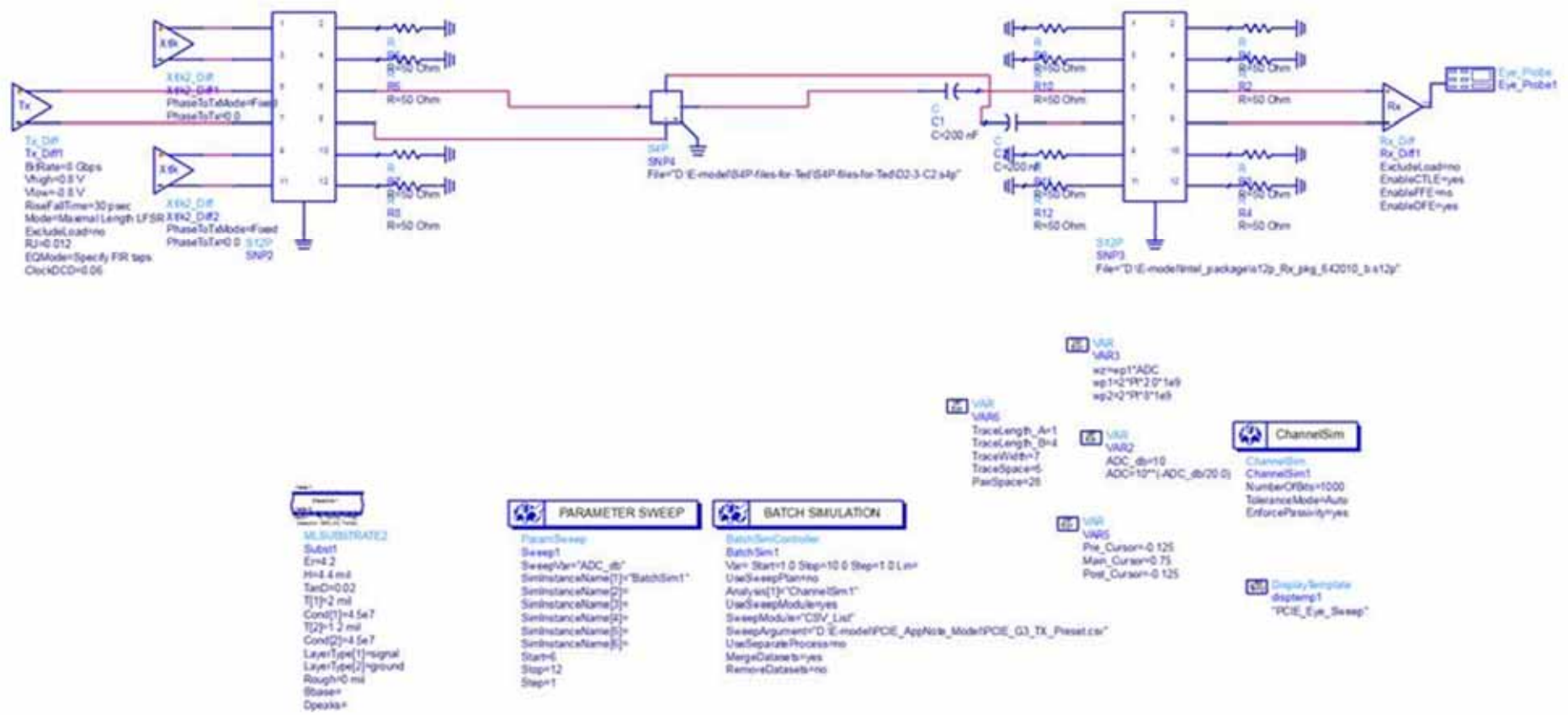
D2-9-A: PCIE 2.0, 5Gbps





AGILENT ADS DESIGN TEMPLATE

- PCIe Gen 3 (8 Gbps)
  - Since model is S4P (only one diff pair), crosstalk removed from the channel analysis.



CHANNEL SIMULATION RESULTS

D2-3-C2: PCIE 3.0, 8Gbps

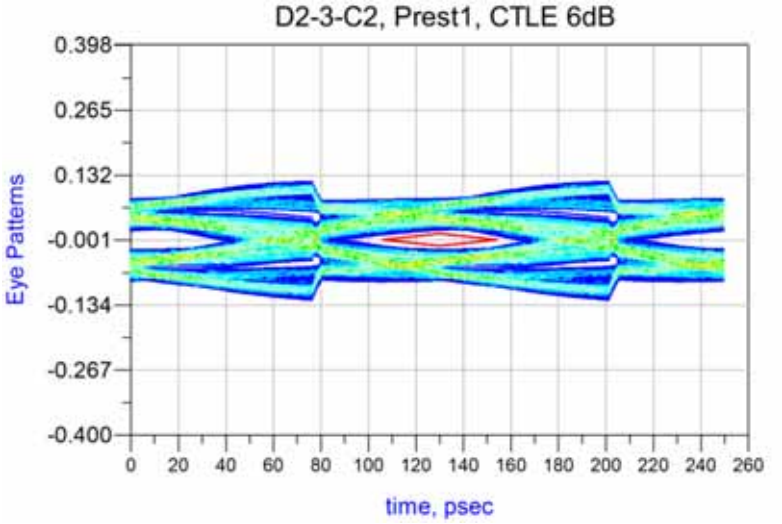
Eqn height=25 mV Eqn width=3.75e-11

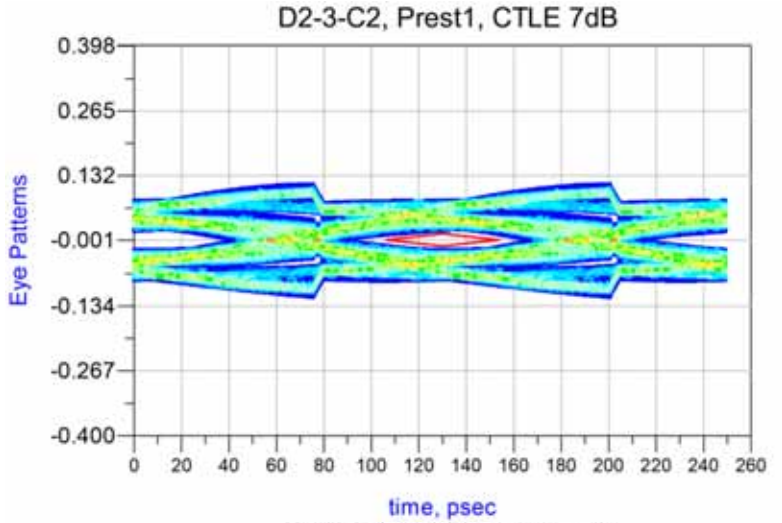
ADC_db	Preset1_Height	Preset1_Width	Preset1_result
6.000	0.039	7.625E-11	Pass
7.000	0.037	7.625E-11	Pass
8.000	0.031	7.313E-11	Pass
9.000	0.026	6.500E-11	Pass
10.000	0.022	5.562E-11	Fail
11.000	0.015	4.625E-11	Fail
12.000	0.013	3.813E-11	Fail

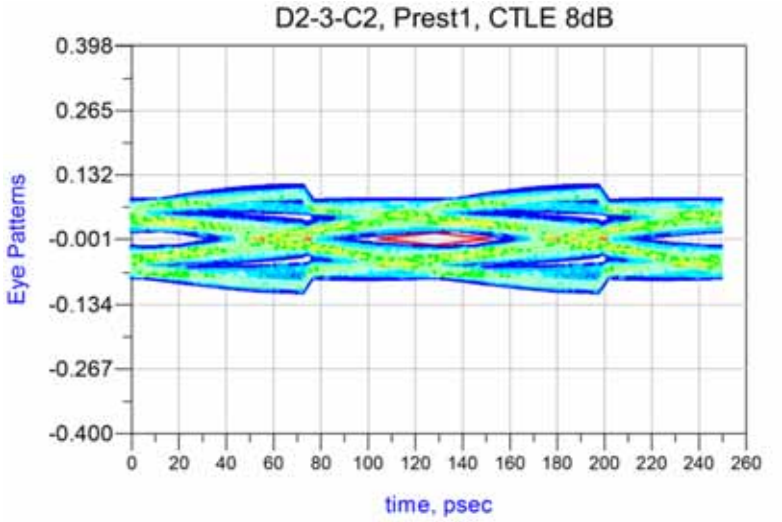
ADC_db	Preset8_Height	Preset8_Width	Preset8_result
6.000	0.035	7.813E-11	Pass
7.000	0.035	7.938E-11	Pass
8.000	0.033	7.938E-11	Pass
9.000	0.030	7.813E-11	Pass
10.000	0.028	7.250E-11	Pass
11.000	0.026	6.500E-11	Pass
12.000	0.022	5.938E-11	Fail

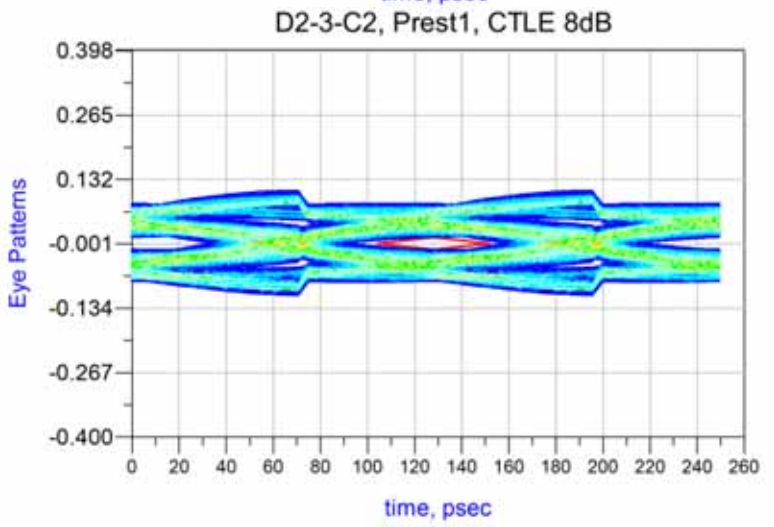
ADC_db	Preset7_Height	Preset7_Width	Preset7_result
6.000	0.029	7.813E-11	Pass
7.000	0.028	7.438E-11	Pass
8.000	0.027	7.000E-11	Pass
9.000	0.023	6.437E-11	Fail
10.000	0.021	5.812E-11	Fail
11.000	0.018	5.250E-11	Fail
12.000	0.016	4.688E-11	Fail

D2-3-C2: Passing Results

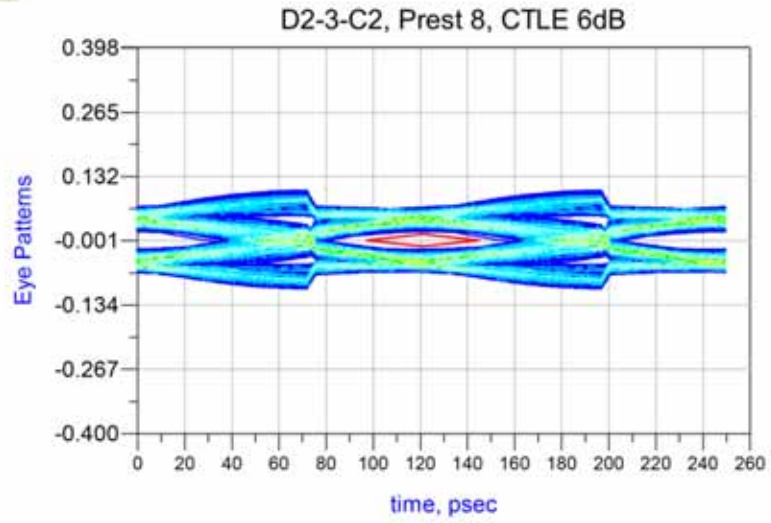


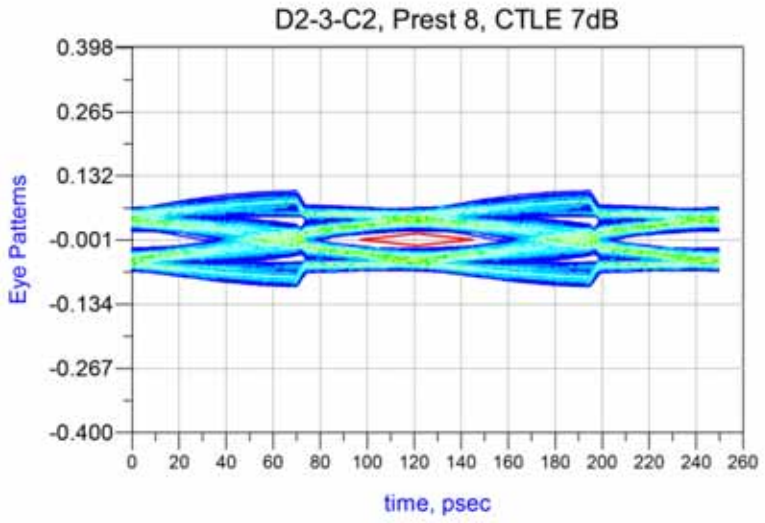


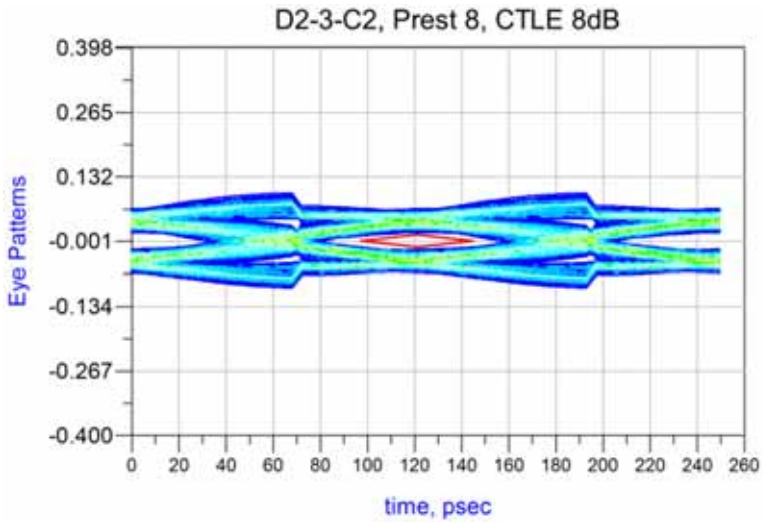


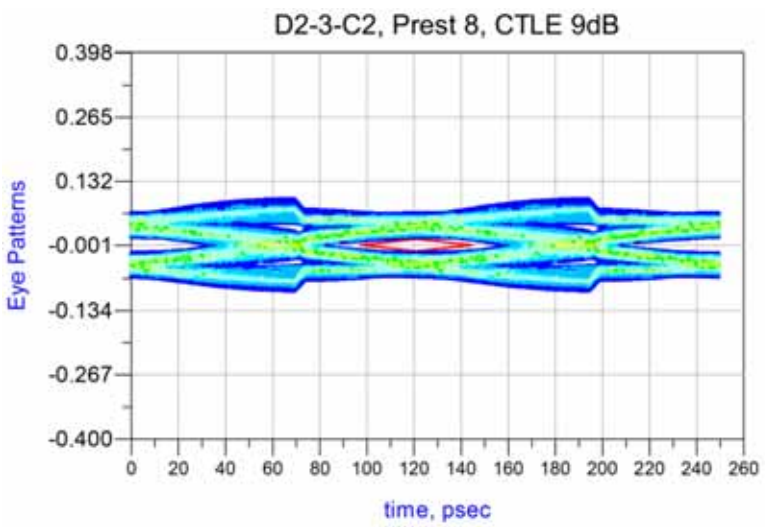


D2-3-C2: Passing Results

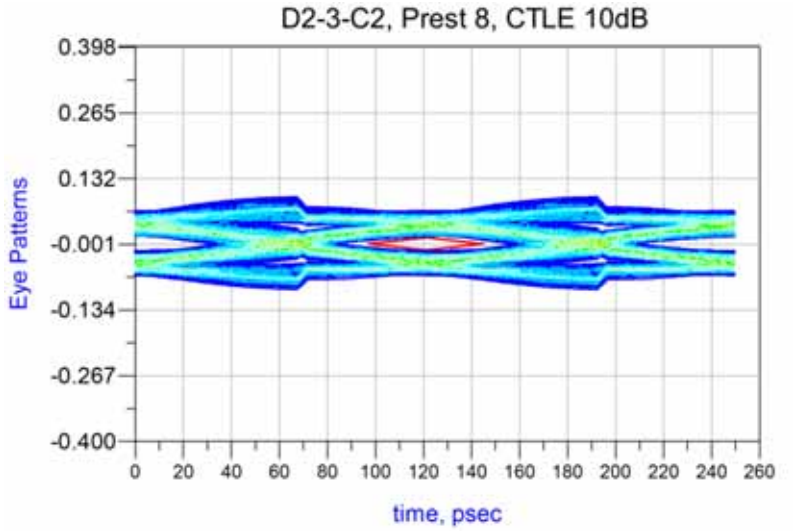


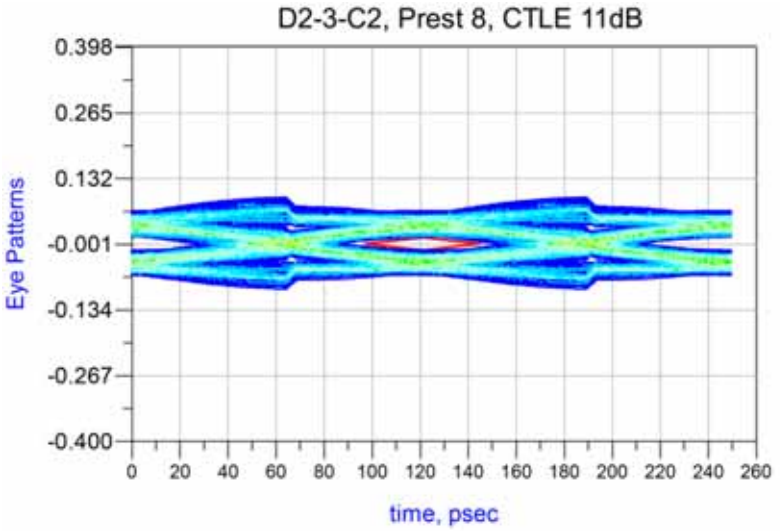




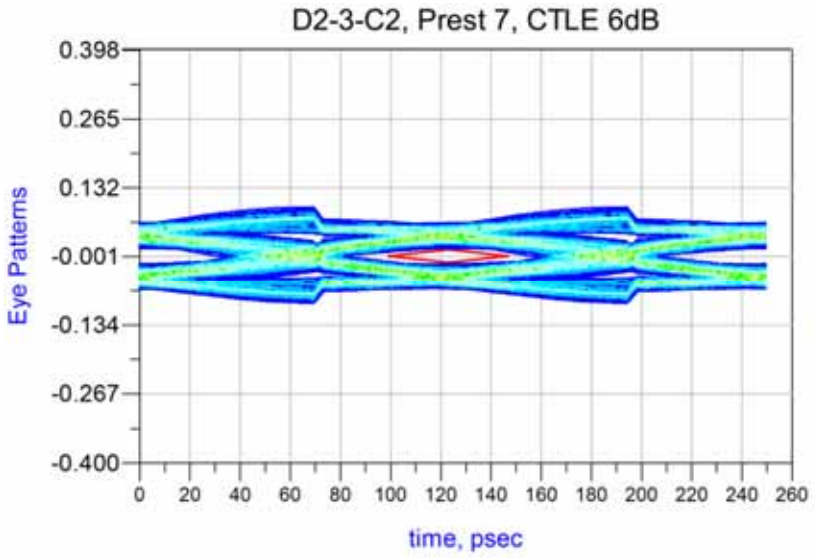


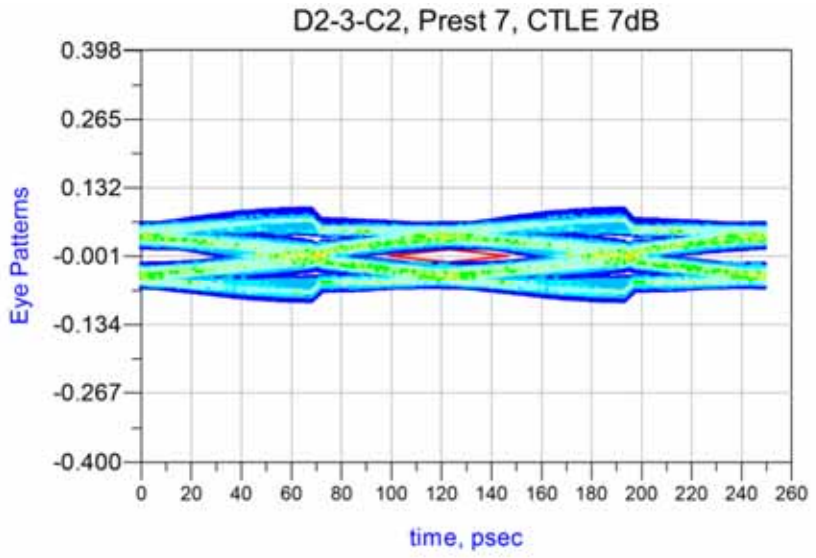
D2-3-C2: Passing Results

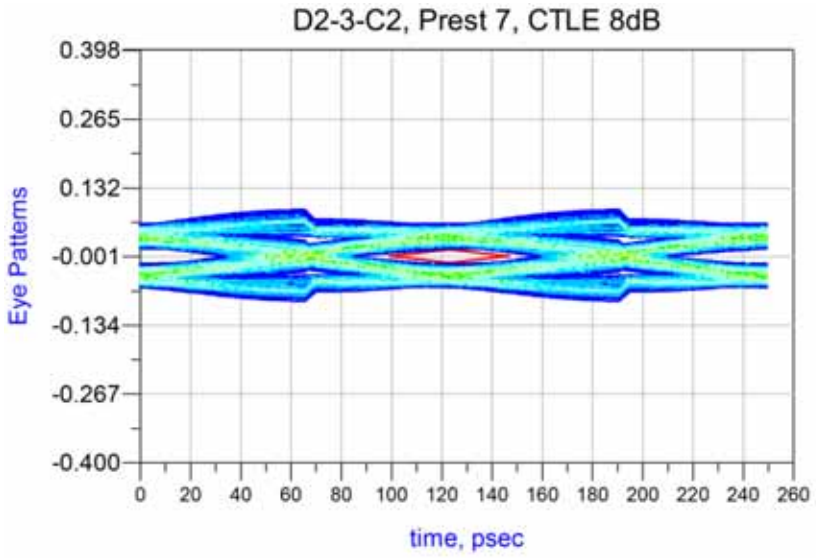




D2-3-C2: Passing Results







CHANNEL SIMULATION RESULTS

D2-5-C2: PCIE 3.0, 8Gbps

Eqn height=25 mV Eqn width=3.75e-11

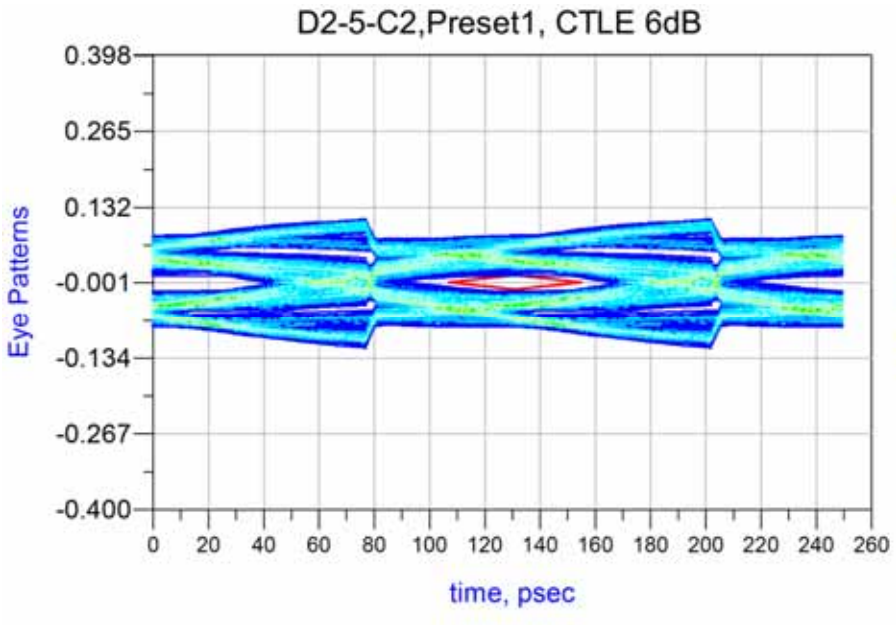
ADC_db	Preset1_Height	Preset1_Width	Preset1_result
6.000	0.026	7.625E-11	Pass
7.000	0.026	7.875E-11	Pass
8.000	0.021	7.313E-11	Fail
9.000	0.018	6.562E-11	Fail
10.000	0.015	5.500E-11	Fail
11.000	0.009	4.000E-11	Fail
12.000	0.006	2.937E-11	Fail

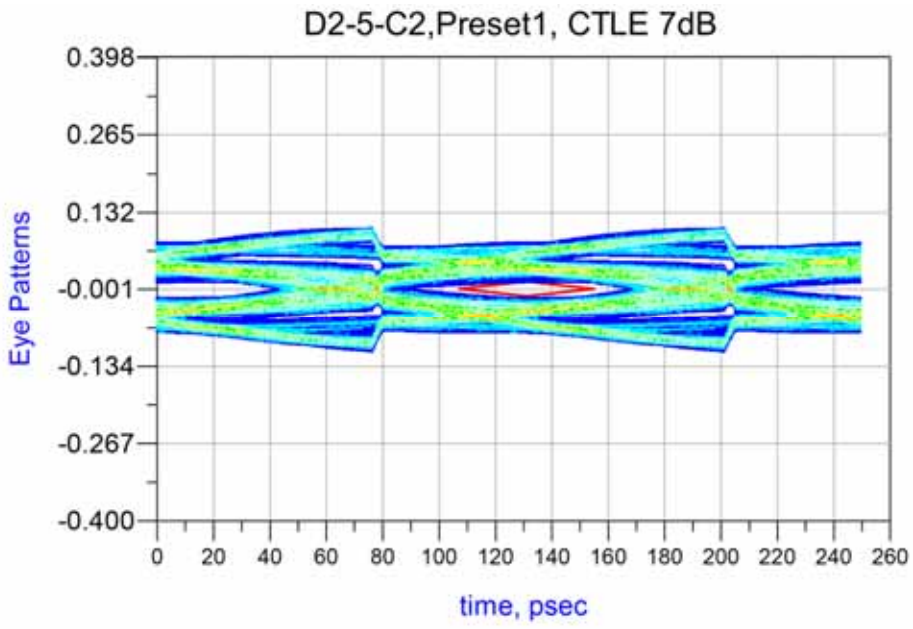
ADC_db	Preset8_Height	Preset8_Width	Preset8_result
6.000	0.021	7.688E-11	Fail
7.000	0.023	8.125E-11	Fail
8.000	0.022	8.188E-11	Fail
9.000	0.020	7.625E-11	Fail
10.000	0.018	7.125E-11	Fail
11.000	0.015	6.250E-11	Fail
12.000	0.014	5.562E-11	Fail

ADC_db	Preset7_Height	Preset7_Width	Preset7_result
6.000	0.018	7.813E-11	Fail
7.000	0.016	7.500E-11	Fail
8.000	0.016	7.000E-11	Fail
9.000	0.013	6.000E-11	Fail
10.000	0.012	5.188E-11	Fail
11.000	0.009	4.500E-11	Fail
12.000	0.008	3.875E-11	Fail

CHANNEL SIMULATION RESULTS

D2-5-C2: Passing Results





CHANNEL SIMULATION RESULTS

D2-9-C2: PCIE 3.0, 8Gbps

Eqn height=25 mV Eqn width=3.75e-11

ADC_db	Preset1_Height	Preset1_Width	Preset1_result
6.000	0.018	7.563E-11	Fail
7.000	0.017	7.688E-11	Fail
8.000	0.015	7.625E-11	Fail
9.000	0.013	7.625E-11	Fail
10.000	0.010	6.750E-11	Fail
11.000	0.007	5.438E-11	Fail
12.000	0.004	3.937E-11	Fail

ADC_db	Preset8_Height	Preset8_Width	Preset8_result
6.000	0.015	7.875E-11	Fail
7.000	0.015	8.563E-11	Fail
8.000	0.014	8.500E-11	Fail
9.000	0.012	8.250E-11	Fail
10.000	0.012	8.125E-11	Fail
11.000	0.012	7.625E-11	Fail
12.000	0.010	6.688E-11	Fail

ADC_db	Preset7_Height	Preset7_Width	Preset7_result
6.000	0.011	8.188E-11	Fail
7.000	0.011	8.063E-11	Fail
8.000	0.009	7.875E-11	Fail
9.000	0.008	7.125E-11	Fail
10.000	0.007	6.000E-11	Fail
11.000	0.006	4.937E-11	Fail
12.000	0.005	4.125E-11	Fail

CONCLUSIONS / THINGS TO CONSIDER

- ASP-129637-03 (QMS) + ASP-129646-03 (QFS) looks to be able to easily support the PCIe/104 architecture goal of having a Host + 5 Peripheral boards running PCIe @ 5 Gbps.
  - Preliminary results show that up to 10 peripheral boards can be supported (Host Board + 9 Stacking + 1 Device board)

- ASP-129637-03 (QMS) + ASP-129646-03 (QFS) looks to be able to support the PCIe/104 architecture of having a Host + 6 Peripheral boards running PCIe @ 8 Gbps.
  - Preliminary simulations demonstrate passing receive eyes with up to 6 peripheral boards (Host Board + 5 Stacking + 1 Device board)

CONCLUSIONS / THINGS TO CONSIDER

- The simulation results use the standard eye mask templates
  - By default, we utilize a 20% enlarged eye mask (both eye width and eye height are increased) to account for margin of error with how the channel is modeled (e.g., not being able to account for all T-line entities of the channel)
  - Since the model files used for this analysis are from measurement of a physical test fixture, we opted to use standard eye mask template
- The simulation results do not include any crosstalk induced jitter.
  - These are single aggressor measurements only; which is what the Diver 2 platform allowed.
  - Additional simulations would need to be done using multi-port electrical models of the Q2 ASP to show impact of crosstalk.
- The Diver 2 boards were designed using Samtec's Final Inch design approach for QMS/QFS
  - standard PCB materials and layout specifications
  - investigating more optimized PCB design techniques will require additional simulations and/or testing

CONCLUSIONS / THINGS TO CONSIDER

- Future analyses – SATA
  - The Diver 2 includes test topologies to evaluate SATA running at up to 8 Gbps.
  - Samtec is still working on an ADS “Design Template” based on SATA 3.0 specification

- Future Analyses – More optimized channel design
  - As mentioned previously, the Diver 2 platform was designed using what can be referred to as design practices that are not optimized for maximum signal integrity performance.
  - To help better assess PCIe Gen 3 and other SERDES protocols faster than 8 Gbps, a “Diver” platform utilizing design practices to optimize channel performance can be considered