Extending Co-packaged Copper for 448G

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***Abstract*— Copper remains highly valuable for short- and medium-reach 448 Gbps applications. At these distances, copper offers advantages in power efficiency, latency, and integration, provided that channel loss and bandwidth limitations are carefully managed.**

Keywords— interconnect, 448Gbps, co-packaged copper

I. Introduction

The scaling of AI and cloud infrastructure continues to drive per-lane data rates toward 448 Gbps. While optical interconnects are required for long reach, copper remains highly valuable for short- and medium-reach applications, including chip-to-chip and intra-tray links. At these distances, copper offers advantages in power efficiency, latency, and integration, provided that channel loss and bandwidth limitations are carefully managed.

Transitioning from 224 Gbps to 448 Gbps PAM4 doubles the Nyquist frequency from 56 GHz to 112 GHz, placing increasingly stringent demands on channel bandwidth and insertion loss. In practical systems, end-to-end channels typically exhibit bandwidth roll-off and non-ideal frequency responses below Nyquist. At the same time, the power required to recover signals from these impaired channels continues to increase with each generation. As a result, sub-Nyquist impairments become the expected regime at 448 Gbps rather than the exception, placing greater reliance on receiver equalization. Technical challenges remain in the design of 448 Gbps interconnects. This paper outlines the study of a co-packaged copper (CPC) interconnect prototype that is designed to operate at 448 Gbps and is based on an existing 224 Gbps CPX (co-packaged copper or optics) topology.

II. Technical Challenges

For 224 Gbps topologies, interconnect performance with a CPX architecture is well studied and documented [1-9]; our work examines using a CPX interconnect to 448 Gbps. Specifically, this work examines a high-performance CPC cable assembly representative of next-generation interconnects (Fig. 1). CPC places the high-speed separable electrical interface directly on the package substrate. In this topology, the twinax cable is not lossless, but it is better controlled with a larger copper cross-section medium than long package and PCB routing for high-speed links. The benefit comes from eliminating package-to-board transitions, PCB breakout, via fields, and connector launches from the highest-speed portion of the channel.

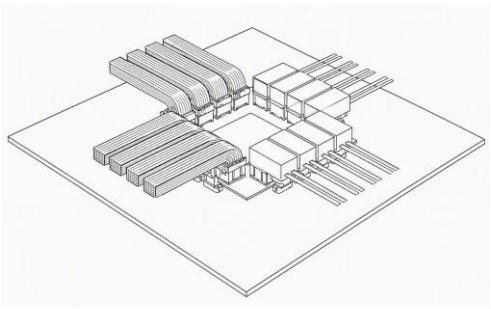


Fig. 1. Drawing of CPC Interconnect Used at 448 Gbps

Our work showed that two primary challenges dominate channel response performance for CPC interconnects at 448 Gbps: (1) achieving a smooth frequency response with minimal resonances, and (2) maintaining sufficient signal-to-noise ratio (SNR) to enable detection at a target symbol error rate.

III. Measured Results

The measured channel in our 448 Gbps CPX prototype interconnect includes precision RF interfaces, short PCB routing, and a twinax cable segment, resulting in approximately 20 dB insertion loss at frequencies slightly above 100 GHz (Fig. 2).

The channel response remains relatively smooth, with minimized impedance discontinuities and controlled reflections, underscoring the importance of careful channel design in mitigating resonance-induced impairments. We identified the following major areas of concern in channel design: electrical resonance, crosstalk and shielding, and ensuring manufacturability.

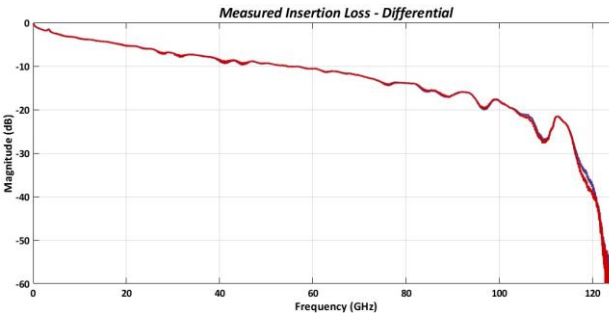


Fig. 2. 448 Gbps CPX prototype measurement including RF connectors, test fixture PCB routing, and twinax cable

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A. *Electronic Resonance*

At 224 Gbps PAM4, the Samtec CPX topology has industry leading performance with separable interface capability. This same topology, which features a short contact wipe (stub) was used as a basis for the 448 Gbps prototype. Our work showed that at 448G, it is necessary to further reduce stubs, which could impact mechanical tolerance (Fig. 3). For a separable interface to function properly, one or both beams have to function as springs. Obtaining >112 GHz of bandwidth from such structures necessitates extremely small feature sizes. Small features result in larger variations from manufacturing tolerances.

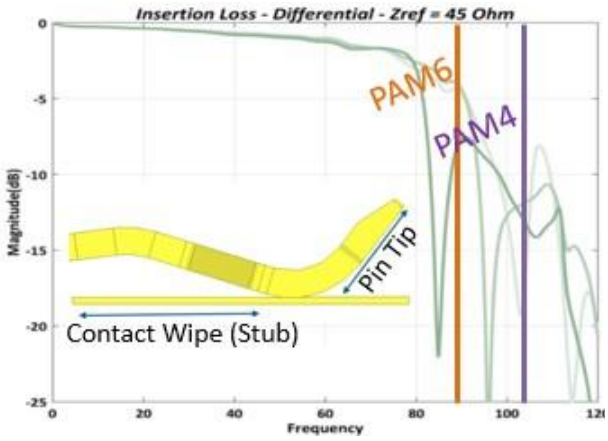


Fig. 3. Variations in Contact Wipe and Pin Tip

B. *Crosstalk and Shielding*

Reducing crosstalk at 448 Gbps required additional shielding and an improved return path as compared to a 224 Gbps topology. We found that shielding cavity modes must be managed simultaneously. The challenging aspect is that additional shielding and continuity paths increase the design size and lead to reduced density, requiring a higher component count. Our work identified solutions that include miniaturization and novel contact designs (Fig. 4).



Fig. 4. Shielding Concept: 224 vs 448 Gbps

Connector density should not be evaluated only as a mechanical placement issue. At 224 and 448G, it also controls the distribution of loss, skew, return loss, and crosstalk across the lane population. A lower-density connector can appear easier to route yet still produce a worst-case lane if added rows force long detours around the connector field.

The design target should, therefore, be the full lane distribution rather than only the nominal lane. A HDI topology with slightly higher typical loss but a much tighter tail can be easier to equalize, train, test, and manufacture than a topology with a few long, lossy outliers (Fig. 5).

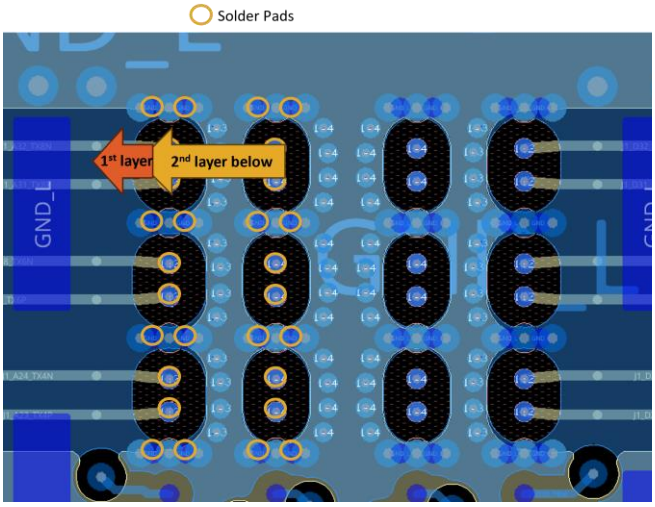


Fig. 5. HDI escape for dense co-packaged connectors. Terminated microvias and HDI layers (indicated by orange arrows) reduce detours and narrow lane-to-lane loss variation relative to row-wise non-HDI breakout.

C. *Design for Manufacturing*

While designing for optimal channel performance (SI) is a priority, real-world production introduces variability, which can result in impedance and return loss (RL) missing design targets. Current tooling capabilities are at their limit, and we can expect more RL at extreme frequencies. In addition, silicon capability is likely to absorb more of the SNR budget.

As a result, there is increased pressure to tighten tolerancing and creative solutions need to be found for manufacturing. Our work identified numerous possibilities to reduce variation in interconnect performance that require further study: increase coupling to highly controlled conductors; decrease coupling to highly variable conductors; incorporate more precise mating and latching features; use design variation-resistant structures; and incorporate compression and elastomers.

IV. BANDWIDTH AT UNCERTAIN NYQUIST

For new applications, interconnect topologies must reduce in size, but they are limited by reasonable manufacturing limits. Interconnect designers now struggle with determining what levels of performance are acceptable. This is especially challenging with targeted Nyquist frequency for 448 Gbps designs ranging from 86 to 90 GHz for PAM6 and 106 to 112 GHz for PAM4. At these data rates, interconnects with a typical 0.5 to 1.0mm pitch will experience cavity resonance near Nyquist frequency due to the shielding surrounding the diff pair, also shown in Fig. 4. The quality of the Rx filter will also be important and impact the performance calculation. At 224 Gbps PAM4, the Rx filter was 5% beyond Nyquist frequency, significantly derating more high frequency noise content than the previous generations (Fig. 6). It is unclear if that will be the same at 448 Gbps. Given the very wide bandwidth, every increase in operation frequency without impairment makes the manufacturability of cost-effective solutions very challenging. Further work is needed to determine if resonances or suck out below Nyquist will be acceptable.

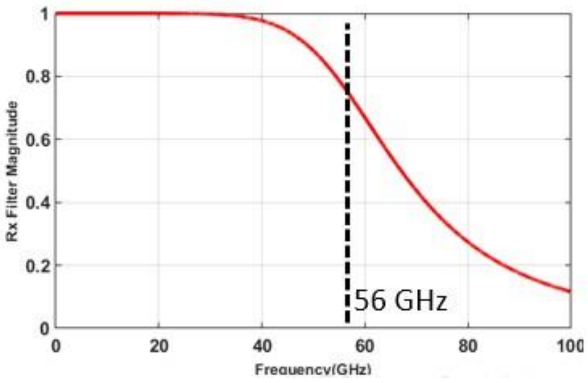


Fig. 6. 224G Rx Bessel-Thompson Filter fb*0.55

V. END 2 INTERCONNECT OPTIONS

Scaling 224 Gbps topologies to 448 Gbps invites an analysis of the impact on End 2 options. We studied CPC to CPC, CPC to backplane, and CPC to front panel optics with speculative loss budgets of 40dB. The CPC and connector backplane configurations assume 448 Gbps PAM6, while the fiber optics design presumes PAM4 (Fig. 7).

The CPC to CPC configuration scales 224G-PAM4 package loss capability to 448G-PAM6. The fully populated packages approach a 45mm trace length and the design manages twinax insertion loss for necessary reach.

The 1 or 2 connector backplane design includes a single connection because direct-mate orthogonal configurations improve the loss budget. The challenge is that a traditional 1.5mm wipe is now resonant at ~60GHz (in-band), so a spring and/or elastomer interface is needed to absorb tolerance. In addition, smaller twinax is required as CPC limits the maximum cable length. Considerations for cabled-backplane with 2 external connectors and approximately 1-meter of external cable become virtually untenable within a 40dB loss budget.

The front-panel optics design reflects the optics industry preference for PAM4. Here, the traditional use of a connector utilizing a PCB edge card interference appears to come to an end. High PCB-Edge-to-Connector crosstalk and large stubs (resonances) make it difficult to get above 80GHz in bandwidth and necessitate innovation to reach 448G-PAM4 capabilities. Overall, this design will experience high package losses.

VI. VALIDATION

A credible 448G validation flow requires more than a smooth insertion-loss plot from one typical lane. It should include package launch extraction, connector and cable models, de-embedding, time-domain reflectometry (TDR), return loss, NEXT/FEXT, mode conversion, skew, mate-cycle repeatability, thermal-mechanical sensitivity, link training, and post-forward error correction (FEC) error behavior. The package, connector, cable, optical engine, and FEC architecture must be reviewed as one system.

FEC is essential for PAM4 systems, but it is not free margin. DesignCon 2024 work on 200+ Gbps Ethernet FEC reviewed end-to-end, concatenated, and segmented FEC for multi-part electrical and optical links and noted that IEEE 802.3dj adopted Hamming (128,120) inner code as part of the 200G/lane IM-DD optics FEC solution [9]. That matters for package-first interconnects because residual error statistics can differ among passive copper, LPO, NPO, CPO, and DSP-retimed optics. Burst behavior, training convergence, and interoperability should be evaluated with the physical channel, not after it.

VII. DESIGN RULES

First, it is important to choose topology before optimizing details. If the signal is forced through long package routing, BGA escape, PCB breakouts, multiple vias, and a conventional front-panel launch, every element must be close to ideal. Direct package-to-cable or package-to-optics paths reduce the number of structures that require equalization.

Second, package edge length should be budgeted as carefully as insertion loss. Connector length, corner keep-outs, cable bend radius, power access, and cold-plate geometry should be included in the earliest channel-planning exercise. Third, optimize the lane population, not only the best lane. Fourth, use copper where copper is naturally strong: short passive links that benefit from low latency and low power. Finally, use optics where geometry, reach, or serviceable cable density dominates.

VIII. CONCLUSION

Wide bandwidth combined with a well-controlled channel profile, as demonstrated here, significantly improves achievable margins in bandwidth-limited PAM4 systems. These results suggest that co-packaged copper interconnects remain a viable solution for short-reach 448 Gbps links, particularly in applications where system constraints favor electrical connectivity over optical alternatives.

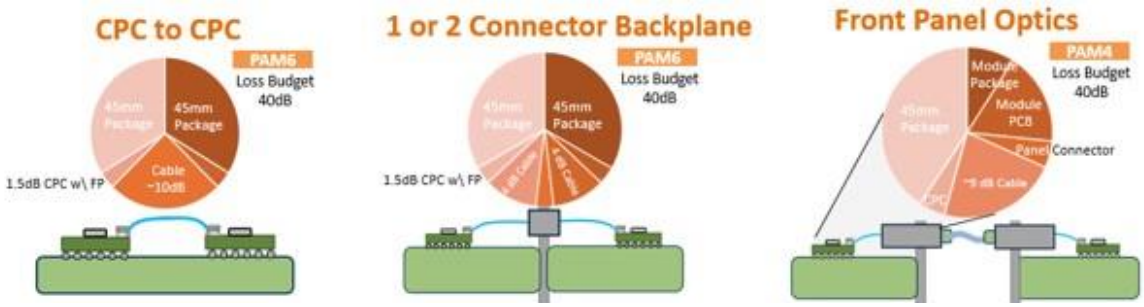


Fig. 7. End 2 Interconnect Options with Speculative Loss Budgets and Modulation Schemes

For practicing engineers, the shift is simple but consequential: we need to stop treating the package, PCB, connector, cable, optical engine, and FEC as separate optimization tasks. At 448G, they are the channel. The winning architecture will be the one that spends the fewest high-loss millimeters before the signal reaches the medium best suited for the job.

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