Application Note

Edge Rate ERM8/ERF8 Series 10mm Stack Height Final Inch® Designs in PCI Express Applications Generation 2 – 5.0 Gbps

Revision Date: December 28, 2007

Developed in conjunction with
Teraspeed Consulting Group LLC

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

COPYRIGHTS, TRADEMARKS, and PATENTS

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

Abstract

The PCI Express is primarily intended as a high performance serial interface targeted for use in desktop, mobile, workstation, server, communications platforms, and embedded devices. As with any modern high speed PCB design, the performance of an actual PCI Express interconnect is highly dependent on the implementation. This paper describes a measurement method applied to proven Samtec Final Inch® designs and this industry standard to help engineers deploy systems of two PCB cards mated through Samtec's family of high speed electrical connectors. To demonstrate the feasibility of using Samtec Edge Rate ERM8/ERF8 Series connectors with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through SPICE simulation and presented in spreadsheet format. Also, trace lengths on the motherboard side of the ERM8/ERF8 Series connectors will be gradually increased to show the limits of compliance.

In order to ensure interoperability between PCI Express transmitter and receiver devices, we will stress a typical interconnect design by stimulating their SPICE model components and devices with worst case data patterns as described in Section 4.3.6.2.4 of PCI Express Base Specification, Rev 2.0. This paper will cover techniques to stress the system with reduced driver amplitude as well as max transmit jitter and noise injection.

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

Introduction

Samtec has developed a full line of connector products that are designed to support serial speeds greater than 5.0 Gbps, the "Baud rate" of each PCI Express Generation 2 data lane. Working with Teraspeed Consulting, they have developed a complete breakout and routing solution for each member of Samtec's line of high speed connectors, called Final Inch®. To demonstrate the feasibility of using Samtec Edge Rate ERM8/ERF8 Series connectors in PCI Express applications with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through SPICE simulation and presented in a user-friendly spreadsheet format. Trace lengths will be varied to show the limits of compliance.

Analysis will consist of stimulating a typical trace-connector-trace circuit path with a worst case signal and then observing the corresponding eye closure related to reflections due to impedance discontinuities, loss, and stubs. Next, utility software will be used to extract, analyze, and format SPICE-measured voltage amplitudes and differential signal crossing times. Mask violations will be recorded in pass/fail format.

Definitions

Interconnect Budget – The amount of loss and jitter that is allowed in the interconnect and still meet the target specification.

Loss – The differential voltage swing attenuation from transmitter to receiver on the trace. The trace is subject to resistive, dielectric, and skin effect loss. Loss increases as trace length and and/or signal frequency increases. Vias and connectors also exhibit losses which must be included in the interconnect budget. Total loss allowed in the interconnect is 13.2 dB.

Jitter – The variation in the time between differential crossings from the ideal crossing time. Jitter includes both data dependent and random contributions on the interconnect. Total jitter allowed is 0.4UI, or 80 ps when UI = 200 ps.

PRBS – Pseudo Random Bit Sequence.

Tj – Total jitter, which is the convolution of the probability density functions for all the jitter sources, Random jitter (Rj) and Deterministic jitter (Dj). The UI allocation is given as the allowable Tj. The PCI Express specification does not specify allocation of Rj and Dj.

UI – Unit Interval. The time interval required for transmission of one data symbol. For a binary lane operating at 5.0 Gbps, the UI is 200 ps.

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

$\mathbf{V_{DIFF}}$ – Differential voltage, defined as the difference of the positive conductor voltage and the negative conductor voltage (V_{D+} - V_{D-}).

$\mathbf{V_{DIFFp-p}}$ – Differential peak-to-peak voltage, defined by the following equations:

$$V_{DIFFp-p} = (2*\max | V_{D+} - V_{D-} |) \text{ (Applies to a symmetric differential swing)}$$

$$V_{DIFFp-p} = (\max | V_{D+} - V_{D-} | \{ V_{D+} > V_{D-} \} + \max | V_{D+} - V_{D-} | \{ V_{D+} < V_{D-} \})$$
(Applies to a asymmetric differential swing)

The PCI Express Specification

PCI Express links are based on recent advances in point-to-point interconnect technology. A PCI Express link is comprised of a dual-simplex communications channel between two components physically consisting of two low-voltage, differential signal pairs. The PCI Express Base Specification defines one half of a link (one transmitter and receiver) an electrical sub-block. The design model used for this paper is of three electrical sub-blocks operating in tandem, the victim surrounded by multiple aggressors, with all bit streams heading in the same direction.

Detailed specifications for an electrical sub-block can be found in the PCI Express 2.0 Base Specification and will be referred to throughout the rest of this paper[1]. Measurement techniques specified in this section have been rigidly adhered to including the requirement for finding the median within the jitter for use in jitter measurements.

[1] The PCI Express Base 2.0 specification is available for purchase though the PCI Sig organization (http://www.pcisig.com/specifications/ordering_information).

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

Setup and Measurement

Input Stimulus Setup

A PRBS 2^7-1 pattern was used for victim stimulus pair and a repeating 1010… pattern used for the aggressor pairs surrounding the victim pair. Teraspeed has developed its own stimulus conversion tool that has the capability to selectively de-emphasize and/or add jitter to the HSPICE stimulus output, such as a vector file. This was used to add enough jitter and de-emphasis to just meet worst case PCI Express Generation 2 transmit jitter specifications.

The Test Circuit Model

The test circuit modeled is shown in Figure 1. It consists of the following:

- One set of Teraspeed behavioral driver models with programmable edge rate, amplitude, and de-emphasis.
- One set of six AC coupling capacitors, value = 100 nF.
- 1 Samtec Edge Rate Final Inch® HSPICE design, comprised of the connector SPICE model for Samtec P/N ERF8-xxx-05.0-x-DV mated to Samtec P/N ERM8-xxx-05.0-x-DV, with lossy differential trace models on both sides of the connector. Breakouts are included in the connector model as well as short sections of trace. These breakout trace lengths were compensated for in the lengths simulated and reported.
- One set of Teraspeed behavioral models for PCI Express receivers with on-die termination.

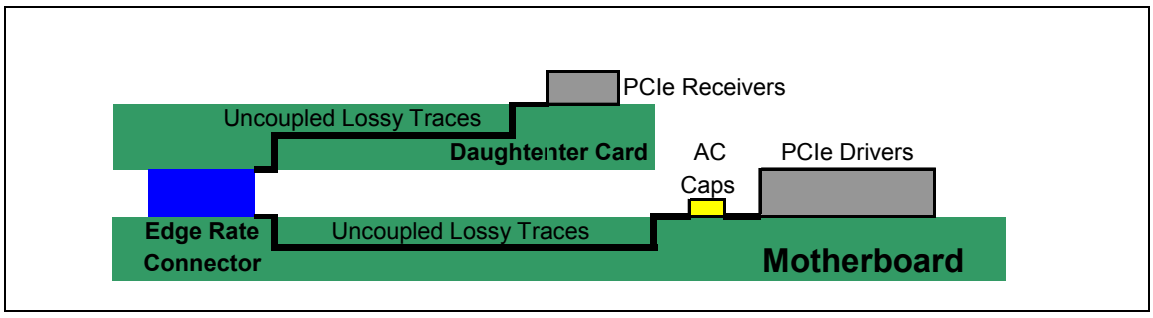

Figure 1 - PCI Express Test Circuit

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

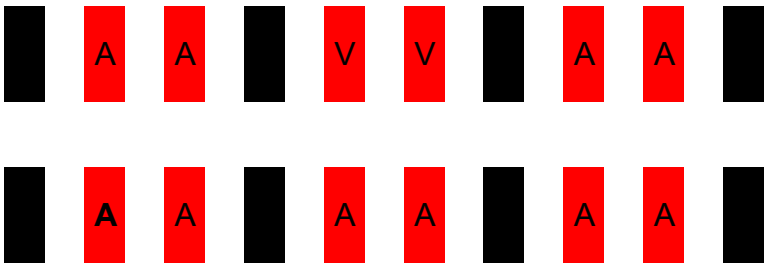

Figure 2 – Edge Rate ERM8/ERF8 Series connector test cases pad patterns for HSPICE simulations. V = Victim, A = Aggressor

Procedure

Interconnect Budget

The interconnect budget can be best illustrated by the mask shown in Figure 3. In order to pass the PCI Express constraints for loss and jitter, the simulated eye waveform must not touch any location within the grey areas shown. Calculated interconnect budget values are shown in Table 1.

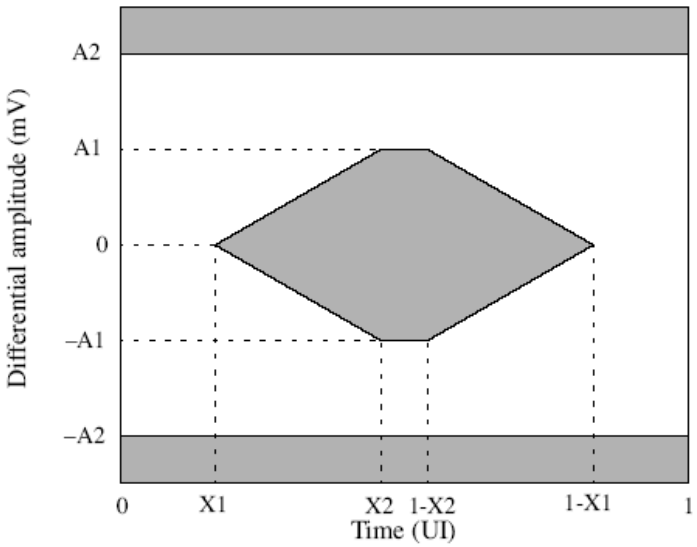

Figure 3 - Example eye mask template

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

	Low Power Differential Maximum Loss, A1 to –A1 (See example mask template) ($V_{DIFFp-p}$)	Normal Power Differential Maximum Loss, A1 to –A1 (See example mask template) ($V_{DIFFp-p}$)	Minimum Eye Width, X1 to 1-X1 (See example mask template) (UI_{p-p})
Driver at Package Pin	0.400	0.800	0.75
Receiver at Package Pin	0.120	0.120	0.60[2]
Interconnect budget:	10.5 dB loss	16.5 dB loss[1]	0.15 UI (30ps when UI = 200 ps)

Table 1 - PCI Express Gen 2 interconnect budgets: max loss and min eye width calculated values

[1]The worst case operational loss budget at 2.5 GHz Nyquist frequency is calculated by taking the minimum driver output voltage ($V_{TX-DIFFp-p}$ = 800 mV) divided by the minimum input voltage to the receiver ($V_{RX-DIFFp-p}$ = 175 mV). 175/800 = .219, which after conversion results in a maximum loss budget of 13.2 dB.

[2]Minimum width pulse at Rx after accounting for worst Tj at 10^{-12} BER. See Table 4-12 in the PCI Express Base Specification, Revision 2.0.

Transmitter Compliance Measurements

Setup for Tj for UI Measurements

Before the PCI Express circuit model can be simulated and measured, we must first set up the driver stimulus to provide minimum TX eye width (maximum jitter) and minimum amplitude for both low power and regular power driver models. As mentioned in the previous section, the driver stimulus' jitter can be adjusted until it just reaches the maximum total jitter allowed under the compliance load shown in the figure below. The AC coupling capacitor C_{TX} can be set anywhere between 75pF and 200pF. We set C_{TX} to 100nF for all simulations because it is a popular value in the industry. Table 2 shows the resulting output measurements. The eye pattern generated in the PCI Express driver compliance test simulation can be found in Figure 5.

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

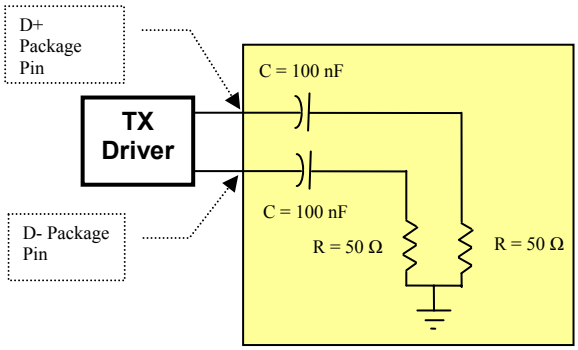

Figure 4 - PCI Express Compliance Test/Measurement load

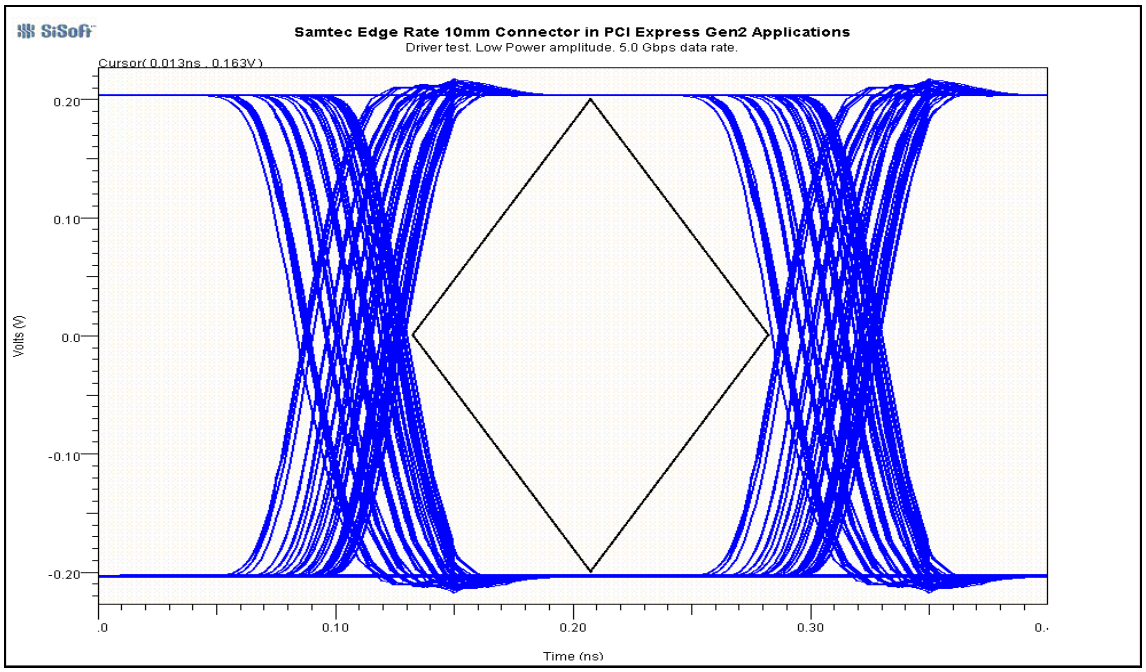

Figure 5 – Example of worst case stimulus eye waveform, probed at Teraspeed driver behavioral model nodes connected to PCIe compliance test/measurement load. Low power setting.

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

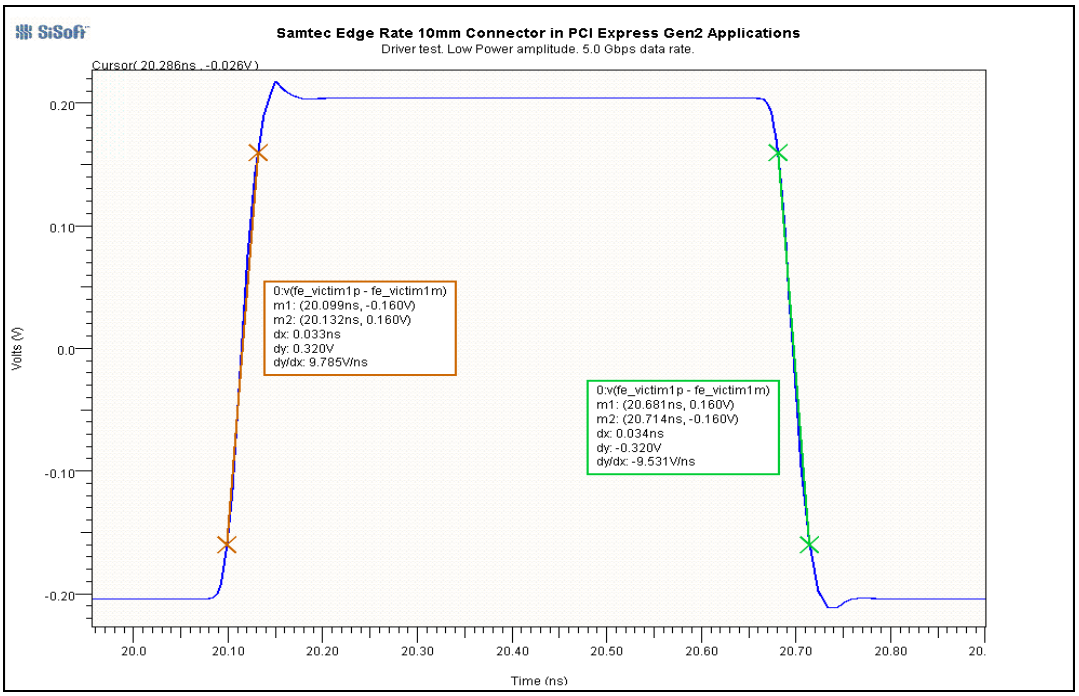

Figure 6 – Example of worst case stimulus edge rate measurement, probed at Teraspeed driver behavioral model nodes connected to PCIe compliance test/measurement load - Low power setting.

De-emphasis		Vdiff$_{p-p}$		Total Jitter	Edge Rate
		Transition Bit	De-emphasized Bit	≤0.25 UI, measured at crossings	≥0.15 UI, measured 20% to 80%
0dB (Low Power)	**Specification**	≥400 mV	None	≤50 ps	≥30ps
	Measured	398 mV[1]	-	49 ps	30ps
-3 dB	**Specification**	≥800 mV	≥566 mV	≤50 ps	≥30ps
	Measured	800 mV[1]	566 mV	49 ps	30ps
-4 dB	**Specification**	≥800 mV	≤505 mV	≤50 ps	≥30ps
	Measured	800 mV[1]	505 mV	49 ps	30ps
-5.5 dB	**Specification**	≥800 mV	≥425 mV	≤50 ps	≥30ps
	Measured	800 mV[1]	425 mV	49 ps	30ps
-6.5 dB	**Specification**	≥800 mV	≤378 mV	≤50 ps	≥30ps
	Measured	800 mV[1]	378 mV	49 ps	30ps

Table 2- PCI Express TX Silicon + Package Measurements at Package Pin

[1]The PCI Express Base Specification defines X2 to 1-X2 = 0. The minimum TX height measurements were taken at mid bit.

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

Measurements at the Receiver

Note: The total trace length specified is the sum of the mother board and daughter card differential traces as shown in Figure 1. Both trace lengths are equal in each simulation.

ERM8/ERF8 10mm Stack Height, Diff. Pair w/ Grounds Configuration

PCI Express with Edge Rate Connector Final Inch Circuit	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	**≥120 $mV_{DIFFp-p}$**	**≥120 ps**	-
10.0" total trace	286 mV	150 ps	Pass
20.0" total trace	221 mV	145 ps	Pass
30.0" total trace	165 mV	139 ps	Pass
39.0" total trace	121 mV	126 ps	Pass
40.0"total trace	118 mV	127 ps	Fail

Table 3 - PCI Express, Connector Far-end Measurements, Low Power Driver.

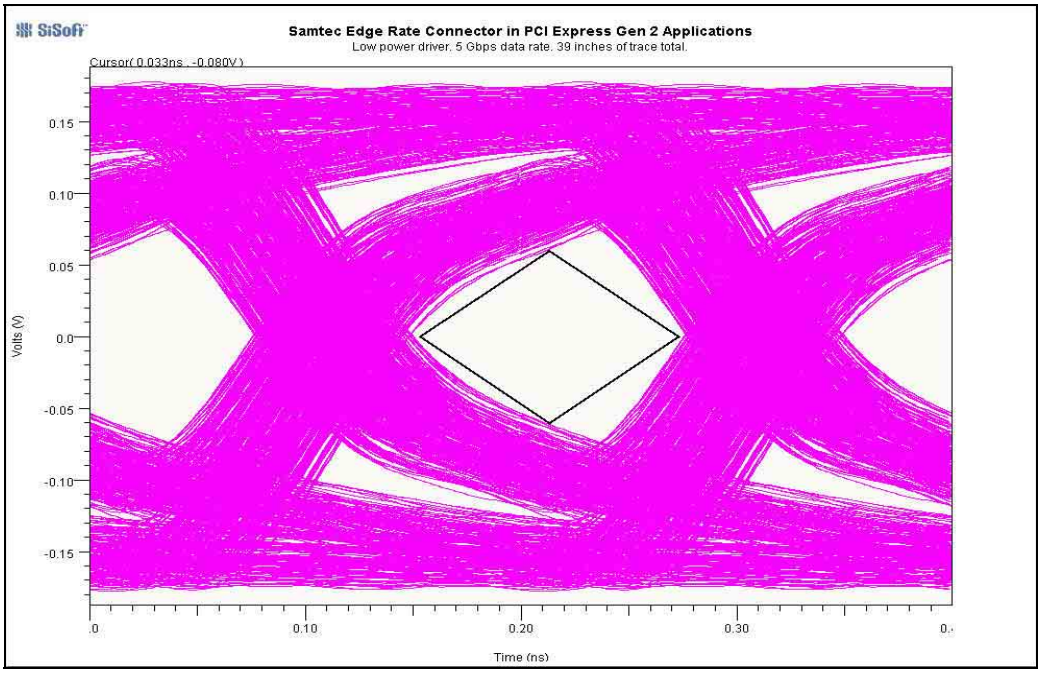

Figure 7 – Receiver eye measurement, probed at far end termination.
Low power driver setting with 0 dB de-emphasis.
Total trace length = 39 inches.

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

PCI Express with Edge Rate Connector Final Inch Circuit	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	**≥120 $mV_{DIFFp-p}$**	**≥120 ps**	-
10.0" total trace	395 mV	143 ps	Pass
20.0" total trace	366 mV	144 ps	Pass
30.0" total trace	303 mV	145 ps	Pass
40.0" total trace	232 mV	138 ps	Pass
50.0" total trace	160 mV	123 ps	Pass
55.0" total trace	153 mV	127 ps	Pass
59.0" total trace	137 mV	120 ps	Pass
60.0" total trace	133 mV	118 ps	Fail

Table 4 - PCI Express, Connector Far-end Measurements, Normal Driver with -3dB de-emphasis.

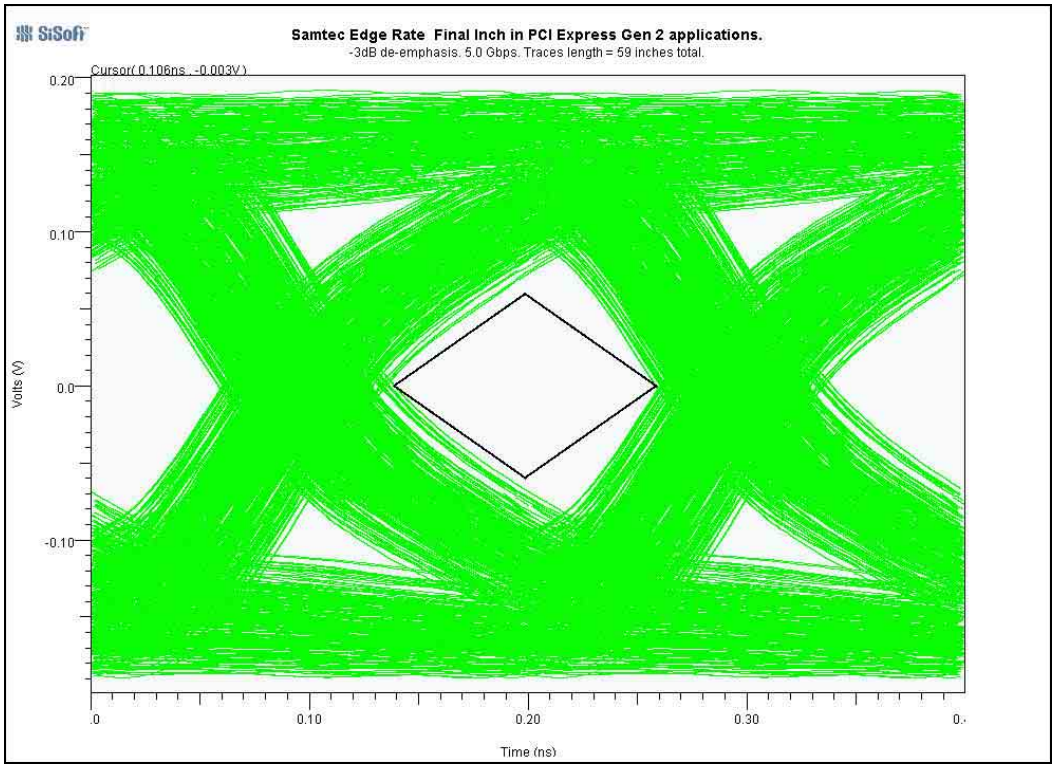

Figure 8 – Receiver eye measurement, probed at far end termination.
Normal power driver setting with -3 dB de-emphasis.
Total trace length = 59 inches.

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

PCI Express with Edge Rate Connector Final Inch Circuit	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	**≥120 $mV_{DIFFp-p}$**	**≥120 ps**	-
10.0" total trace	352 mV	140 ps	Pass
20.0" total trace	329 mV	143 ps	Pass
30.0" total trace	303 mV	143 ps	Pass
40.0" total trace	238 mV	142 ps	Pass
50.0" total trace	179 mV	135 ps	Pass
59.0" total trace	139 mV	126 ps	Pass
60.0" total trace	126 mV	119 ps	Fail

Table 5 - PCI Express, Connector Far-end Measurements, Normal Driver with -4dB de-emphasis.

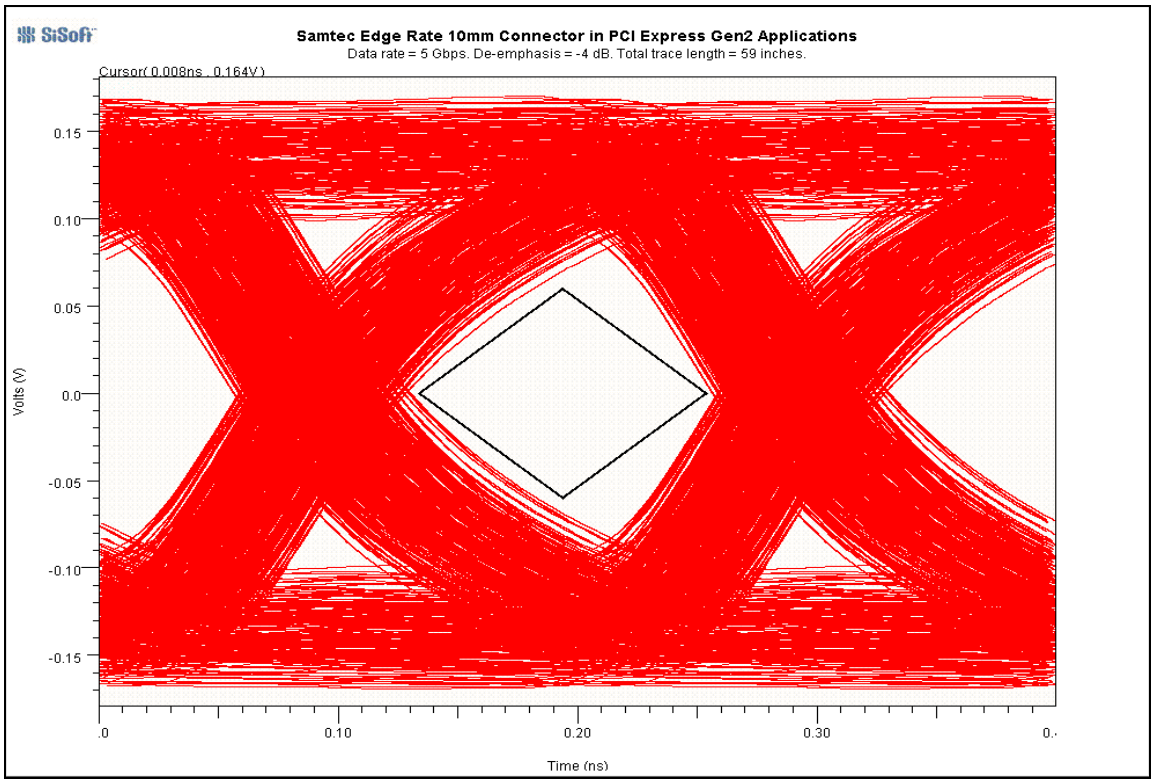

Figure 9 – Receiver eye measurement, probed at far end termination.
Normal power driver setting with -4 dB de-emphasis.
Total trace length = 59 inches.

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

PCI Express with Edge Rate Connector Final Inch Circuit	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	**≥120 $mV_{DIFFp-p}$**	**≥120 ps**	-
10.0" total trace	279 mV	144 ps	Pass
20.0" total trace	277 mV	141 ps	Pass
30.0" total trace	273 mV	143 ps	Pass
40.0" total trace	270 mV	144 ps	Pass
50.0" total trace	266 mV	142 ps	Pass
60.0" total trace	271 mV	145 ps	Pass
70.0" total trace	126 mV	129 ps	Pass
72.0" total trace	122 mV	127 ps	Pass
73.0" total trace	118 mV	126 ps	Fail

Table 6 - PCI Express, Connector Far-end Measurements, Normal Driver with -5.5dB de-emphasis.

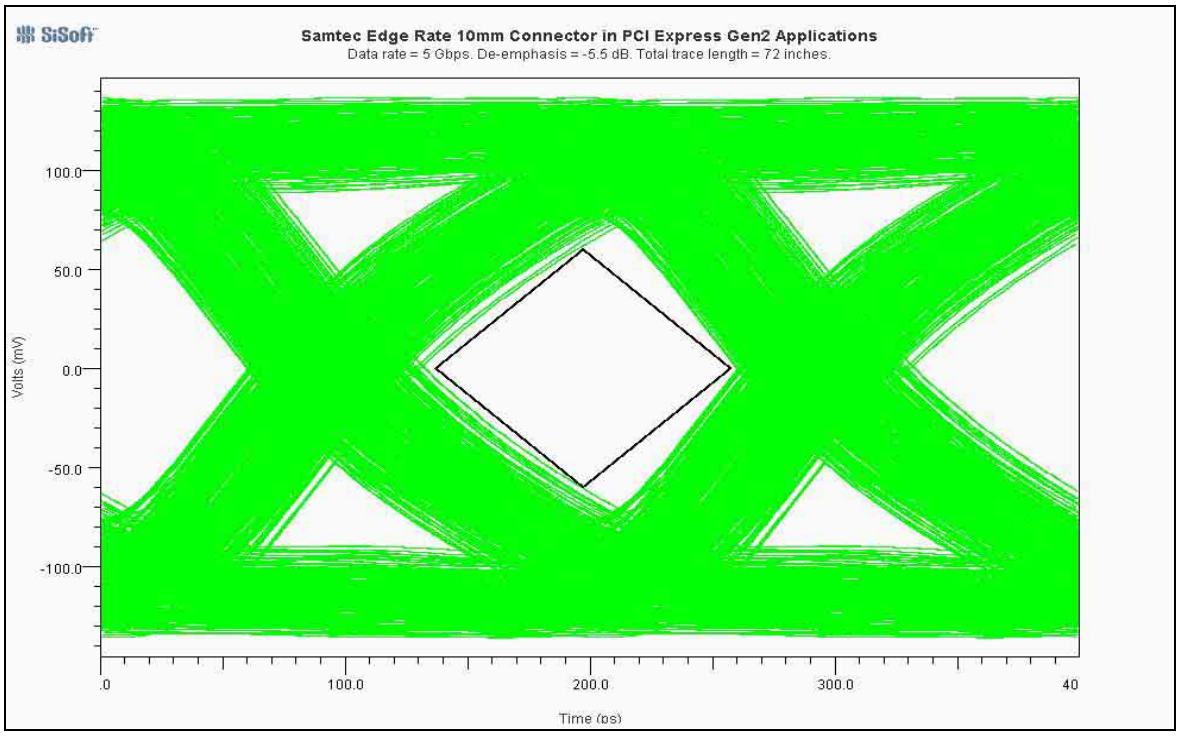

Figure 10 – Receiver eye measurement, probed at far end termination.
Normal power driver setting with -5.5 dB de-emphasis.
Total trace length = 72 inches

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

PCI Express with Edge Rate Connector Final Inch Circuit	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	**≥120 $mV_{DIFFp-p}$**	**≥120 ps**	-
10.0" total trace	249 mV	144 ps	Pass
20.0" total trace	245 mV	143 ps	Pass
30.0" total trace	243 mV	143 ps	Pass
40.0" total trace	228 mV	143 ps	Pass
50.0" total trace	210 mV	143 ps	Pass
60.0" total trace	173 mV	143 ps	Pass
70.0" total trace	136 mV	140 ps	Pass
75.0" total trace	121 mV	133 ps	Pass
76.0" total trace	116 mV	133 ps	Fail

Table 7 - PCI Express, Connector Far-end Measurements, Normal Driver with -6.5dB de-emphasis.

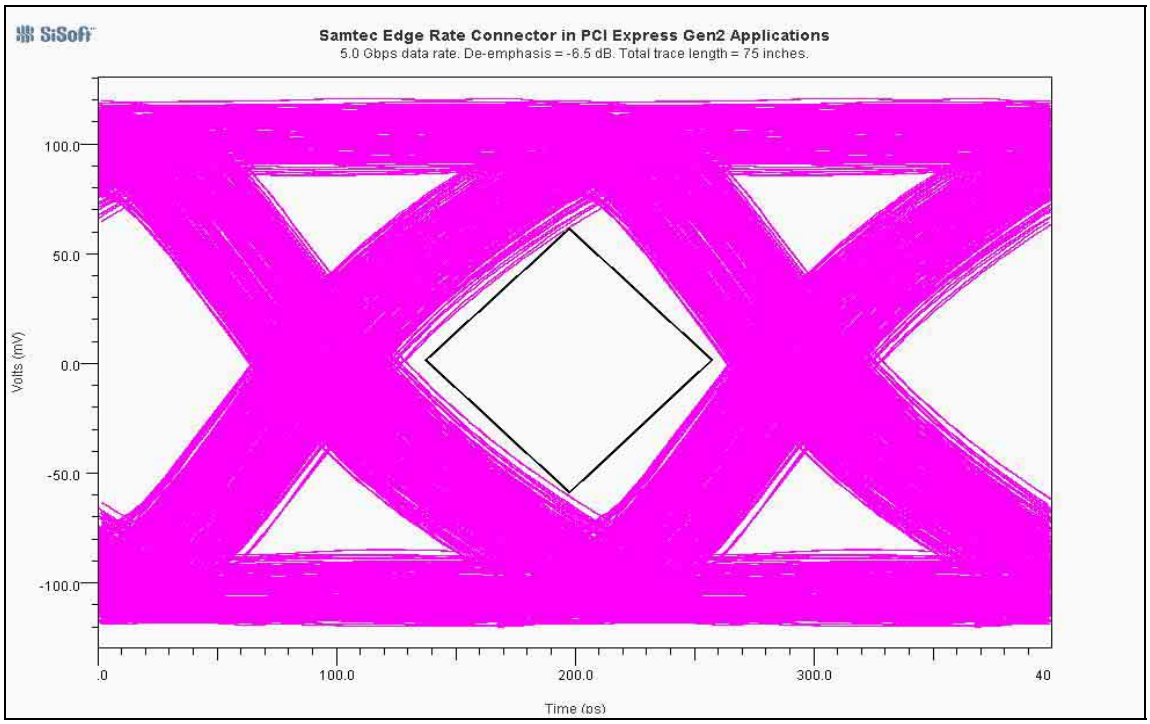

Figure 11 – Receiver eye measurement, probed at far end termination.
Standard driver setting with -6.5 dB de-emphasis.
Total trace length = 75 inches.

Series: ERM8/ERF8, 10mm Stack Height
Standard: PCI Express, Generation 2

Conclusions

When used with Samtec's Final Inch® differential routing, breakout, and trace width solution, a single Samtec Edge Rate ERM8/ERF8 Series 10mm connector in a motherboard to daughter card configuration can be used to transfer PCI Express lanes with total trace lengths up to:

- 39 inches in low power driver mode.
- 59 inches when using a normal driver with -3 dB to -4 dB de-emphasis.
- 72 inches when using a normal driver with -5.5 dB de-emphasis.
- 75 inches when using a normal driver with -6.5 dB de-emphasis.

Recommendations

Designers should be aware that using smaller trace widths, laminates with higher loss tangent, and sub optimal routing solutions with higher pair-to-pair coupling and additional via stubs will decrease overall performance and the maximum allowable trace length. It is advisable, when designing systems that approach the maximum trace length limits, to perform detailed modeling, simulation, and measurement of the target design including the effects of material properties, traces, vias, and additional components.