Application Note

PCIE Series
Final Inch® Designs in
PCI Express Applications
Generation 1 – 2.5 Gbps

Revision Date: March 24, 2006

Series: PCIE (PCI Express Standard Connector)
Standard: PCI Express, Generation 1 (2.5 Gbps)

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Abstract

PCI Express is primarily intended as a high performance serial interface targeted for use in desktop, mobile, workstation, server, communications platforms, and embedded devices. As with any modern high speed PCB design, the performance of an actual PCI Express interconnect is highly dependent on the implementation. This paper describes a measurement method applied to proven Samtec Final Inch® designs and this industry standard to help engineers deploy systems of two PCB cards mated through Samtec's family of high speed electrical connectors. To demonstrate the feasibility of using Samtec PCIE Series PCI Express connectors with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through SPICE simulation and presented in spreadsheet format. Also, trace lengths on the motherboard side of the PCIe connector will be gradually increased to show the limits of compliance.

In order to ensure interoperability between PCI Express transmitter and receiver devices, we will stress a typical interconnect design by stimulating their SPICE model components and devices with stressed data patterns. This paper will cover techniques to stress the system with reduced driver amplitude as well as jitter and noise injection.

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Introduction

Samtec has developed a full line of connector products that are designed to support serial speeds greater than 2.5 Gbps, the "Baud rate" of each PCI Express Generation 1 data lane. Working with Teraspeed Consulting, they have developed a complete breakout and routing solution for each member of Samtec's line of high speed connectors, called Final Inch®. To demonstrate the feasibility of using Samtec PCIE Series connectors in PCI Express applications with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through SPICE simulation and presented in a user-friendly spreadsheet format. Trace lengths will be varied to show the limits of compliance.

Analysis will consist of stimulating a typical trace-connector-trace circuit path with a worst case signal and then observing the corresponding eye closure related to reflections due to impedance discontinuities, loss, and stubs. Next, utility software will be used to extract, analyze, and format SPICE-measured voltage amplitudes and differential signal crossing times. Mask violations (see Figure 4) will be recorded in pass/fail format.

Definitions

Interconnect Budget – The amount of loss and jitter that is allowed in the interconnect and still meet the target specification.

Loss – The differential voltage swing attenuation from transmitter to receiver on the trace. The trace is subject to resistive, dielectric, and skin effect loss. Loss increases as trace length and and/or signal frequency increases. Vias and connectors also exhibit losses which must be included in the interconnect budget. Total loss allowed in the interconnect is 13.2 dB.

Jitter – The variation in the time between differential crossings from the ideal crossing time. Jitter includes both data dependent and random contributions on the interconnect. Total jitter allowed is 0.3UI, or 120 ps when UI = 400 ps.

PRBS – Pseudo Random Bit Sequence.

Tj – Total jitter, which is the convolution of the probability density functions for all the jitter sources, Random jitter (Rj) and Deterministic jitter (Dj). The UI allocation is given as the allowable Tj. The PCI Express specification does not specify allocation of Rj and Dj.

UI – Unit Interval. The time interval required for transmission of one data symbol. For a binary lane operating at 2.5 Gbps, the UI is 400 ps.

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V_{DIFF} – Differential voltage, defined as the difference of the positive conductor voltage and the negative conductor voltage (V_{D+} - V_{D-}).

$V_{DIFFp-p}$ – Differential peak-to-peak voltage, defined by the following equations:

$$V_{DIFFp-p} = (2 * max \mid V_{D+} - V_{D-} \mid) \text{ (Applies to a symmetric differential swing)}$$

$$V_{DIFFp-p} = (max \mid V_{D+} - V_{D-} \mid \{ V_{D+} > V_{D-} \} + max \mid V_{D+} - V_{D-} \mid \{ V_{D+} < V_{D-} \})$$
$$\text{(Applies to a asymmetric differential swing)}$$

The PCI Express Specification

PCI Express links are based on recent advances in point-to-point interconnect technology. A PCI Express link is comprised of a dual-simplex communications channel between two components physically consisting of two low-voltage, differential signal pairs. The PCI Express Base Specification defines one half of a link (one transmitter and receiver) an electrical sub-block. The design model used for this paper is of three electrical sub-blocks operating in tandem, the victim surrounded by two aggressors, with all bit streams heading in the same direction.

The PCI Express 1.0 Base Specification is available though the PCI Sig organization (http://www.pcisig.com) by becoming a member. Detailed specifications for an electrical sub-block can be found starting in Section 4.3 of the PCI Express 1.0 Base Specification and will be referred to throughout the rest of this paper. Detailed electrical signal specifications start in Sub-section 4.3.2. Measurement techniques specified in this section have been rigidly adhered to including the requirement for finding the median within the jitter for use in jitter measurements. See Note 8 of Table 4-6 in the PCI Express 1.0 Base Specification for more details.

Setup and Measurement

Input Stimulus Setup

A PRBS 2^7-1 pattern was used for victim stimulus pair and a repeating 1010… pattern used for the aggressor pairs, one on each side of the victim pair. A stimulus generator is built into the SiSoft SiAuditor design analysis tool along with the capability to add jitter to the driver stimulus. This was used to add enough jitter to just meet worst case PCI Express transmit jitter specifications. The slow-slow corner driver behavioral model was used to come as close as possible to the minimum differential $V_{DIFFp-p}$ output and slew rate specification.

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The Test Circuit Model

The test circuit modeled is shown in Figure 1. It consists of the following:

- One set of Teraspeed behavioral models for PCI Express drivers.
- One set of six AC coupling capacitors, value = 100 nF.
- 1 Samtec PCIE Series Final Inch® design, comprised of the connector model for Samtec P/N PCIE-64-02-F-D-TH attached to a standard edge card, and lossy differential trace models on both sides of the connector. Breakouts are included in the connector model as well as short sections of trace. These breakout trace lengths were compensated for in the lengths simulated and reported.
- One set of Teraspeed behavioral models for PCI Express receivers with on-die termination.
- 50 Ohm termination resistors to Ground (as required per Note 7 in Section 4.3.4 of the PCI Express Base Specification, Rev 1.0a.
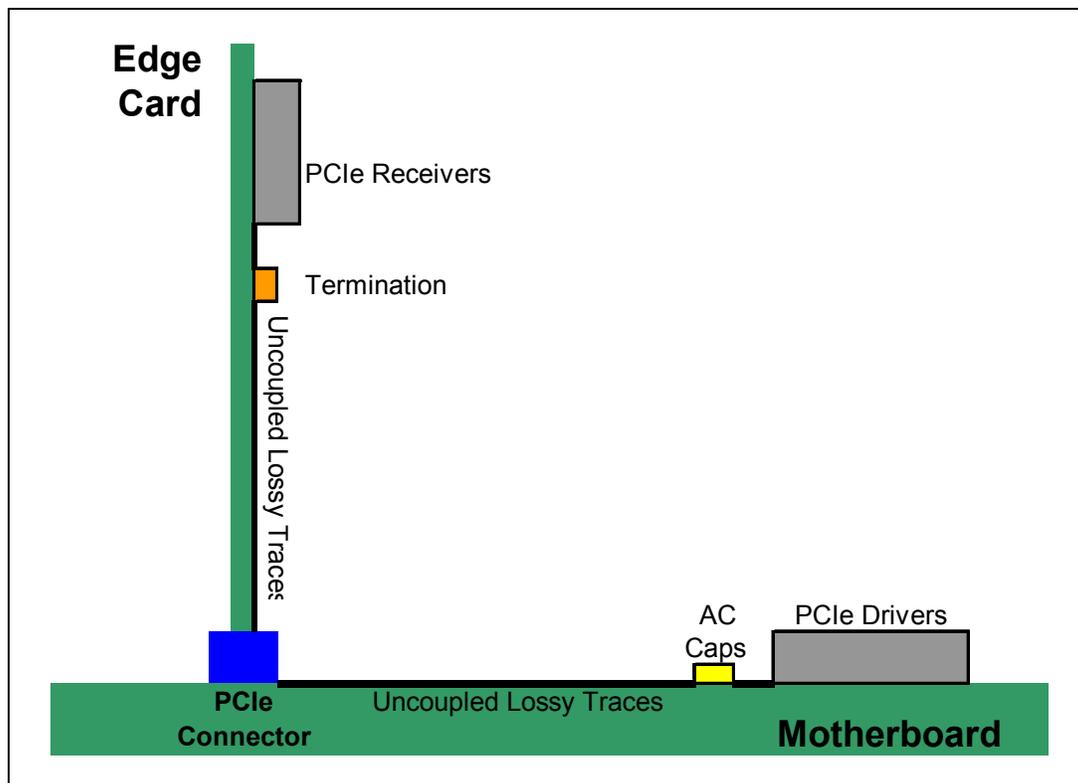

Figure 1— PCI Express Test Circuit (change p/n)

Series: PCIE (PCI Express Standard Connector)
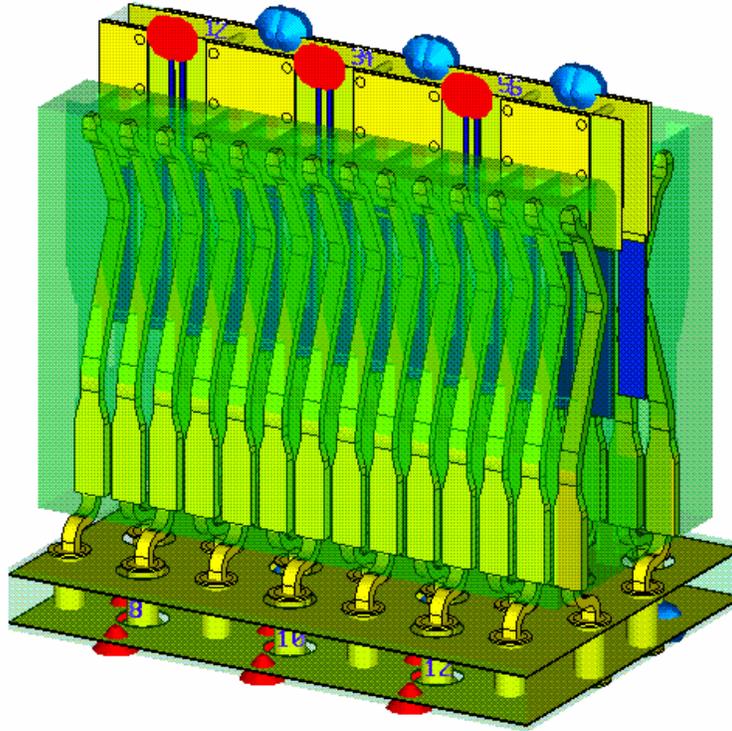**Standard:** PCI Express, Generation 1 (2.5 Gbps)

Figure 2 – X-Ray image of PCIE Series through hole connector section with edge card installed
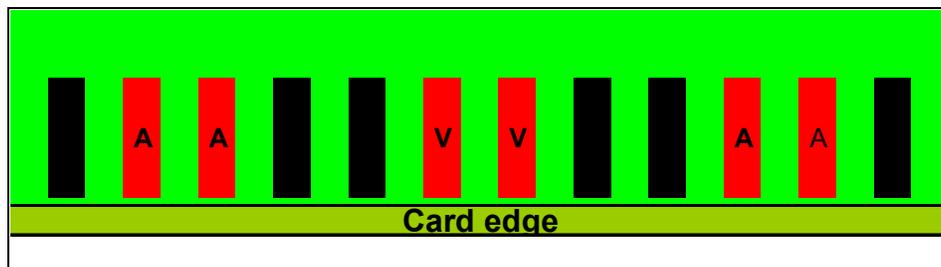

Figure 3 – PCIE Series edge card connector pad pattern; V = Victim, A = Aggressor

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Procedure

Interconnect Budget

The interconnect budget can be best illustrated by the mask shown in Figure 4. In order to pass the PCI Express constraints for loss and jitter, the simulated eye waveform must not touch any location within the grey areas shown. Calculated interconnect budget values are shown in Table 1.
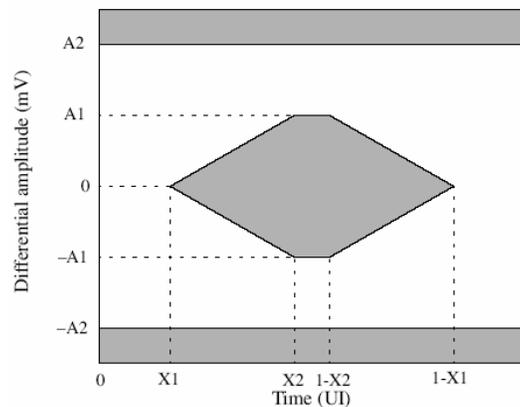

Figure 4 - Example eye mask template

	Maximum Loss, A1 to –A1 (See example mask template) ($V_{DIFFp-p}$)	Minimum Eye Width, X1 to 1-X1 (See example mask template) (UI_{p-p})
Driver at Package Pin	0.800	0.7
Receiver at Package Pin	0.175	0.4
Interconnect budget:	13.2 dB loss[1]	0.3 UI (120ps when UI = 400 ps)

Table 1 - PCI Express interconnect budget max loss and min eye width calculated values

[1]The worst case operational loss budget at 1.25 GHz Nyquist frequency is calculated by taking the minimum driver output voltage ($V_{TX-DIFFp-p}$ = 800 mV) divided by the minimum input voltage to the receiver ($V_{RX-DIFFp-p}$ = 175 mV). 175/800 = .219, which after conversion results in a maximum loss budget of 13.2 dB.

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Transmitter Compliance Measurements

Setup for Tj for UI Measurements

Before the PCI Express circuit model can be simulated and measured, we must first set up the driver stimulus to provide minimum TX eye width (maximum jitter) and minimum amplitude. As mentioned in the previous section, the driver stimulus' jitter can be adjusted until it just reaches the maximum total jitter allowed under the compliance load shown in Figure 4-25 of Section 4.3.3.2 in the PCI Express Base Specification and re-created in Figure 3 below. The AC coupling capacitor C_{TX} can be set anywhere between 75pF and 200pF. We set C_{TX} to 100nF for all simulations because it is a popular value in the industry. Table 2 shows the resulting output measurements. The eye pattern generated in the PCI Express driver compliance test simulation can be found in Appendix A, Picture 1, of this paper.
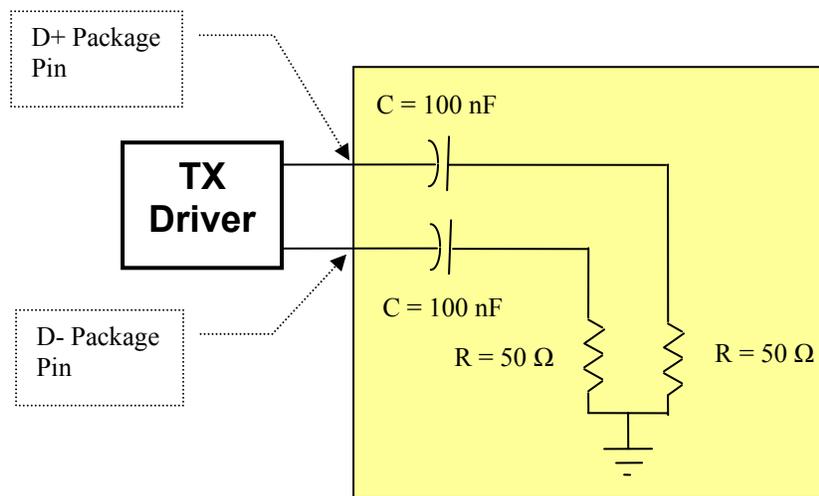

Figure 5 - PCI Express Compliance Test/Measurement load

	Vdiff$_{p-p}$		Total Jitter
	Transition Bit	**De-emphasized Bit**	
Specification	>800 mV	>505 mV	<120 ps
Measured	800 mV[1]	506 mV	120 ps

Table 2 – PCI Express TX Silicon + Package Measurements at Package Pin

[1]The PCI Express Base Specification defines X2 to 1-X2 = 0. The minimum TX height measurements were taken at mid bit.

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Full Circuit Compliance Measurements

Differential Voltage and Eye Width Measurements at Receiver End

PCIE Thru-hole Connector Final Inch Circuit	Max Jitter at UI = 400 ps	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Pass/Fail
Specification	≤240 ps	≥160 ps	≥175 mV$_{DIFFp-p}$	-
10.0" total trace	121 ps	383 ps	323 mV	Pass
12.0" total trace	134 ps	367 ps	233 mV	Pass
12.5" total trace	142 ps	360 ps	218 mV	Pass
13.0" total trace	147 ps	356 ps	199 mV	Pass
13.5" total trace	152 ps	351 ps	187 mV	Pass
13.9" total trace	157 ps	342 ps	177 mV	Pass
14.0" total trace	158 ps	341 ps	174 mV	Fail

Table 3 – PCIE Series Far-end Measurements, 11 mm stack height connector (correct p/n in chart)

[1]The PCI Express Base Specification defines X2 to 1-X2 = 0. The minimum RX height measurements were taken at mid bit.

[2]The total trace length specified is the sum of the two differential trace lengths shown in the PCIE Series schematic, as shown in Figure 1. The edge card trace was fixed in length at 5.3 inches in all simulations.

The eye pattern generated in the PCI Express circuit simulation with 13.9 inches total trace length can be found in Appendix A, Picture 2, of this paper.

Conclusions

A single Samtec PCIE Series through hole connector in a board-to-edge card configuration can be used in PCI Express systems with total trace lengths not to exceed 13.9 inches when used with Samtec's Final Inch® routing, breakout, and trace width solutions. Because loss is the dominant contributor to system degradation, designers should be aware that using smaller trace widths, laminates with higher loss tangent, and sub optimal routing solutions with higher pair-to-pair coupling and additional via stubs will decrease overall performance and the maximum allowable trace length. It is advisable, when designing systems that approach the maximum trace length limits, to perform detailed modeling, simulation, and measurement of the target design including the effects of material properties, traces, vias, and additional components.

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Appendix A – Waveform images
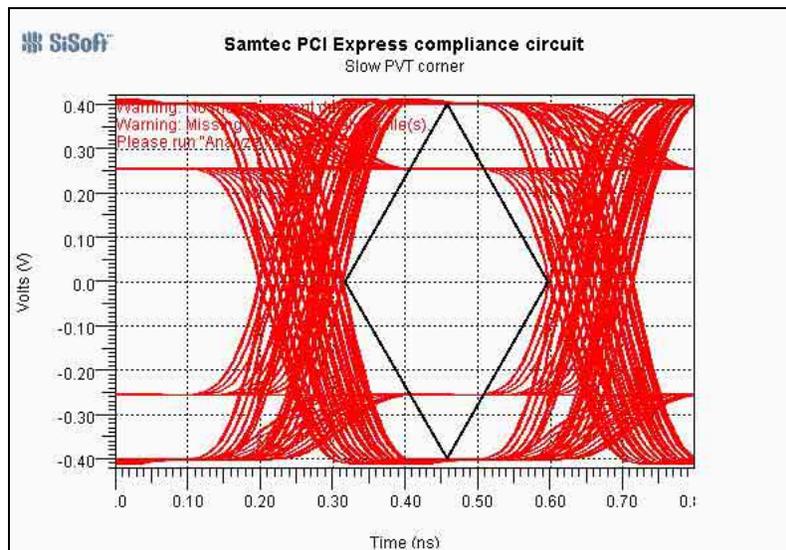
Picture 1 – Worst case stimulus eye waveform, probed at Teraspeed driver behavioral model nodes connected to PCIE Series compliance test/measurement load
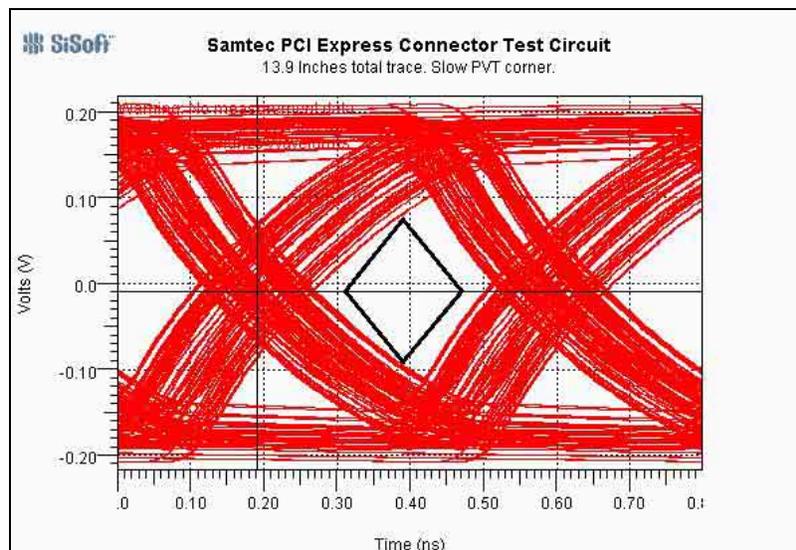
Picture 2 – PCIE Series test circuit eye waveform, probed at terminator pins, 13.9 inches total trace length