



Application Note

PCIE-TH Series Final Inch® Designs in PCI Express Applications Generation 2 – 5.0 Gbps

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Developed in conjunction with
Teraspeed Consulting Group LLC

Series: PCIE-TH (thru-hole)

Standard: PCI Express, Generation 2

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Abstract

PCI Express (PCIe) is primarily intended as a high performance serial interface targeted for use in desktop, mobile, workstation, server, communications platforms, and embedded devices. As with any modern high speed PCB design, the performance of an actual PCI Express interconnect is highly dependent on the implementation. This paper describes a measurement method applied to proven Samtec Final Inch® designs and this industry standard to help engineers deploy systems of two PCB cards mated through Samtec's family of high speed electrical connectors. To demonstrate the feasibility of using Samtec PCI Express connectors with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in spreadsheet format. Also, trace lengths on the motherboard side of the PCIe connector will be gradually increased to show the limits of compliance.

In order to ensure interoperability between PCI Express Generation 2 transmitter and receiver devices, we will stress a typical interconnect design by stimulating their Spice model components and devices with worst case data patterns as described in Section 4.3.6.2.4 of PCI Express Base Specification, Rev 2.0. This paper will cover techniques to stress the system with reduced driver amplitude as well as max transmit jitter and noise injection.

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Introduction

Samtec has developed a full line of connector products that are designed to support serial speeds greater than 5.0 Gbps, the “Baud rate” of each PCI Express Generation 2 data lane. Working with Teraspeed Consulting, they have developed a complete breakout and routing solution for each member of Samtec’s line of high speed connectors, called Final Inch®. To demonstrate the feasibility of using Samtec PCIe connectors in PCI Express applications with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in a user-friendly spreadsheet format. Trace lengths will be varied to show the limits of compliance.

Analysis will consist of stimulating a typical trace-connector-trace circuit path with a worst case signal and then observing the corresponding eye closure related to reflections due to impedance discontinuities, loss, and stubs. Next, utility software will be used to extract, analyze, and format Spice-measured voltage amplitudes and differential signal crossing times. Mask violations (see Figure 2) will be recorded in pass/fail format.

Definitions

Interconnect Budget – The amount of loss and jitter that is allowed in the interconnect and still meet the target specification.

Loss – The differential voltage swing attenuation from transmitter to receiver on the trace. The trace is subject to resistive, dielectric, and skin effect loss. Loss increases as trace length and and/or signal frequency increases. Vias and connectors also exhibit losses which must be included in the interconnect budget. Total loss allowed in the interconnect is 13.2 dB.

Jitter – The variation in the time between differential crossings from the ideal crossing time. Jitter includes both data dependent and random contributions on the interconnect. Total jitter allowed is $0.4UI$, or 80 ps when $UI = 200$ ps.

PRBS – Pseudo Random Bit Sequence.

T_j – Total jitter, which is the convolution of the probability density functions for all the jitter sources, Random jitter (R_j) and Deterministic jitter (D_j). The UI allocation is given as the allowable T_j. The PCI Express specification does not specify allocation of R_j and D_j.

UI – Unit Interval. The time interval required for transmission of one data symbol. For a binary lane operating at 5.0 Gbps, the UI is 200 ps.

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V_{DIFF} – Differential voltage, defined as the difference of the positive conductor voltage and the negative conductor voltage ($V_{D+} - V_{D-}$).

$V_{DIFFp-p}$ – Differential peak-to-peak voltage, defined by the following equations:

$$V_{DIFFp-p} = (2 * \max | V_{D+} - V_{D-} |) \text{ (Applies to a symmetric differential swing)}$$

$$V_{DIFFp-p} = (\max | V_{D+} - V_{D-} | \{ V_{D+} > V_{D-} \} + \max | V_{D+} - V_{D-} | \{ V_{D+} < V_{D-} \})$$

(Applies to an asymmetric differential swing)

The PCI Express Specification

PCI Express links are based on recent advances in point-to-point interconnect technology. A PCI Express link is comprised of a dual-simplex communications channel between two components physically consisting of two low-voltage, differential signal pairs. The PCI Express Base Specification defines one half of a link (one transmitter and receiver) as an electrical sub-block. The design model used for this paper is of three electrical sub-blocks operating in tandem, the victim surrounded by multiple aggressors, with all bit streams heading in the same direction.

Detailed specifications for an electrical sub-block can be found in the PCI Express 2.0 Base Specification and will be referred to throughout the rest of this paper¹. Measurement techniques specified in this section have been rigidly adhered to including the requirement for finding the median within the jitter for use in jitter measurements.

¹ The PCI Express Base 2.0 specification is available for purchase through the PCI Sig organization (http://www.pcisig.com/specifications/ordering_information).

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Setup and Measurement

Input Stimulus Setup

A PRBS 2^7-1 pattern was used for victim stimulus pair and a repeating 1010... pattern used for the aggressor pairs surrounding the victim pair. Teraspeed has developed its own stimulus conversion tool that has the capability to selectively de-emphasize and/or add jitter to the HSPICE stimulus output, such as a vector file. This was used to add enough jitter and de-emphasis to just meet worst case PCI Express Generation 2 transmit jitter specifications.

The Test Circuit Model

The test circuit modeled is shown in Figure 1. It consists of the following:

- One set of Teraspeed behavioral driver models with programmable edge rate, amplitude, and de-emphasis.
- One set of six AC coupling capacitors, value = 100 nF
- 1 PCI Express Final Inch™ design, comprised of the PCIe connector model surrounded by the Samtec's BOR models, lossy trace models and SMA connector models on both sides of the connector.
- 50 Ohm termination resistors to Ground (as required per Section 4.3.4 of the PCI Express Base Specification, Rev 2.0).

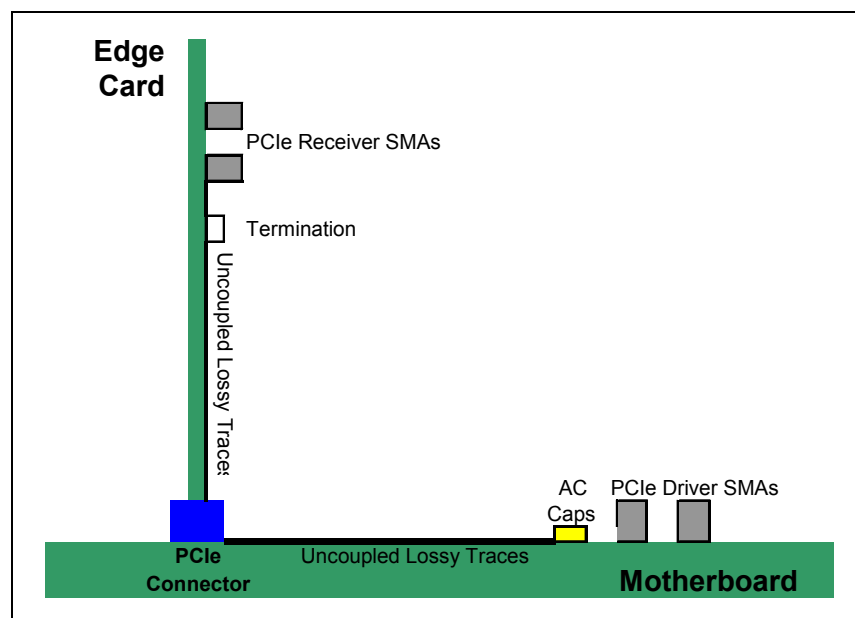


Figure 1 - PCI Express Test Circuit

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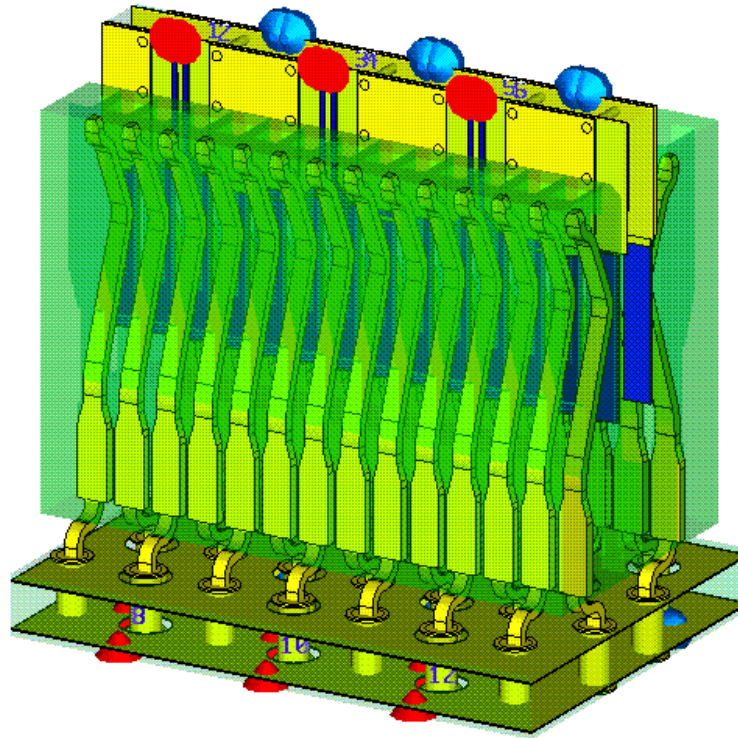


Figure 2a – X-Ray image of PCIe thru-hole connector section with edge card installed

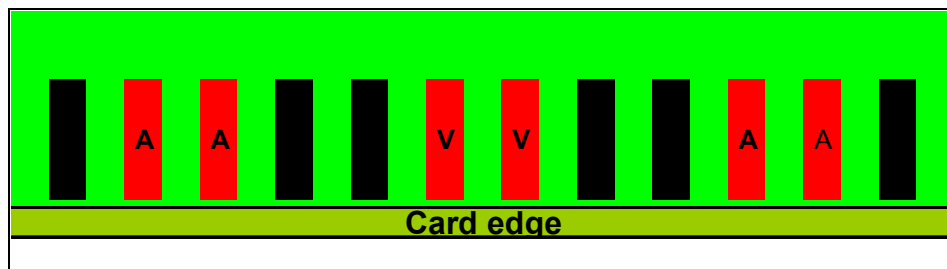


Figure 2b – PCIe edge card connector pad pattern. V = Victim, A = Aggressor

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Procedure

Interconnect Budget

The interconnect budget can be best illustrated by the mask shown in Figure 3. In order to pass the PCI Express constraints for loss and jitter, the simulated eye waveform must not touch any location within the grey areas shown. Calculated interconnect budget values are shown in Table 1.

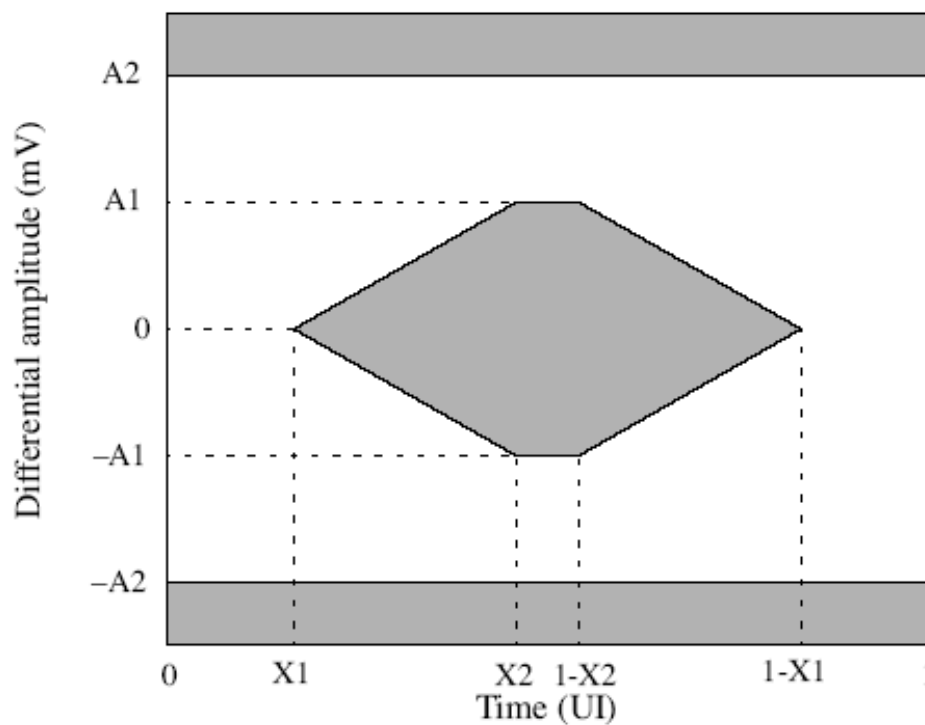


Figure 3 - Example eye mask template

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	Low Power Differential Maximum Loss, A1 to -A1 (See example mask template) ($V_{DIFFp-p}$)	Normal Power Differential Maximum Loss, A1 to -A1 (See example mask template) ($V_{DIFFp-p}$)	Minimum Eye Width, X1 to 1-X1 (See example mask template) (UI_{p-p})
Driver at Package Pin	0.400	0.800	0.75
Receiver at Package Pin	0.120	0.120	0.60 ²
Interconnect budget:	10.5 dB loss	16.5 dB loss ¹	0.15 UI (30ps when UI = 200 ps)

Table 1 - PCI Express Gen 2 interconnect budgets: max loss and min eye width calculated values

¹The worst case operational loss budget at 2.5 GHz Nyquist frequency is calculated by taking the minimum driver output voltage ($V_{TX-DIFFp-p} = 800$ mV) divided by the minimum input voltage to the receiver ($V_{RX-DIFFp-p} = 175$ mV). $175/800 = .219$, which after conversion results in a maximum loss budget of 13.2 dB.

²Minimum width pulse at Rx after accounting for worst Tj at 10^{-12} BER. See Table 4-12 in the PCI Express Base Specification, Revision 2.0.

Transmitter Compliance Measurements

Setup for Tj for UI Measurements

Before the PCI Express circuit model can be simulated and measured, we must first set up the driver stimulus to provide minimum TX eye width (maximum jitter) and minimum amplitude for both low power and regular power driver models. As mentioned in the previous section, the driver stimulus' jitter can be adjusted until it just reaches the maximum total jitter allowed under the compliance load shown in the figure below. The AC coupling capacitor C_{TX} can be set anywhere between 75pF and 200pF. We set C_{TX} to 100nF for all simulations because it is a popular value in the industry. Table 2 shows the resulting output measurements. The eye pattern generated in the PCI Express driver compliance test simulation can be found in [Appendix A](#), Picture 1, of this paper.

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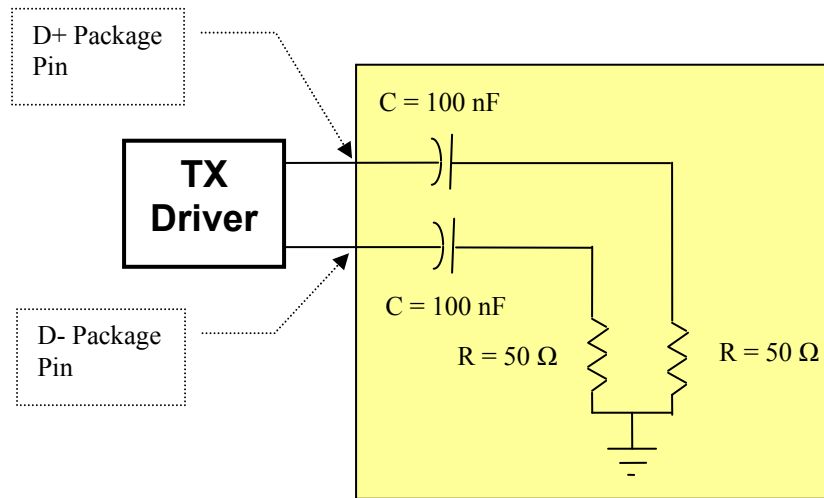


Figure 4 - PCI Express Compliance Test/Measurement load

De-emphasis		Vdiff _{p-p}		Total Jitter	Edge Rate
		Transition Bit	De-emphasized Bit	≤0.25 UI, measured at crossings	≥0.15 UI, measured 20% to 80%
0dB (Low Power)	Specification	≥400 mV	None	≤50 ps	≥30ps
	Measured	401 mV ¹	-	46 ps	34ps
-3 dB	Specification	≥800 mV	≥566 mV	≤50 ps	≥30ps
	Measured	800 mV ¹	566 mV	49 ps	30ps
-4 dB	Specification	≥800 mV	≤505 mV	≤50 ps	≥30ps
	Measured	800 mV ¹	505 mV	49 ps	30ps
-5.5 dB	Specification	≥800 mV	≥425 mV	≤50 ps	≥30ps
	Measured	800 mV ¹	425 mV	49 ps	30ps
-6.5 dB	Specification	≥800 mV	≤378 mV	≤50 ps	≥30ps
	Measured	800 mV ¹	378 mV	49 ps	30 ps

Table 2 - PCI Express TX Silicon + Package Measurements at Package Pin

¹The PCI Express Base Specification defines X2 to 1-X2 = 0. The minimum TX height measurements were taken at mid bit.

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Measurements at the Receiver

Notes:

- 1.) The total trace length specified is the sum of the mother board and daughter card differential traces as shown in Figure 1. Both trace lengths are equal in each simulation.
- 2.) For each of the following tables, the eye patterns generated in the PCI Express circuit simulation with the maximum allowable total trace length in each of the following table can be found in [Appendix A](#) of this paper.

PCIE-TH Connector with Final Inch Design	Min RX Differential Voltage, A1 to -A1 ¹ (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	≥120 mV _{DIFFp-p}	≥120 ps	-
5.0" total trace	296 mV	151 ps	Pass
10.0" total trace	250 mV	148 ps	Pass
15.0" total trace	207 mV	143 ps	Pass
20.0" total trace	171 mV	138 ps	Pass
25.0" total trace	143 mV	129 ps	Pass
27.0" total trace	135 mV	125 ps	Pass
29.0" total trace	121 mV	120 ps	Pass
30.0" total trace	117 mV	118 mV	Fail

Table 3 - PCI Express Connector Far-end Measurements, Low Power Driver.

PCIE-TH Connector with Final Inch Design	Min RX Differential Voltage, A1 to -A1 ¹ (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	≥120 mV _{DIFFp-p}	≥120 ps	-
10.0" total trace	384 mV	151 ps	Pass
20.0" total trace	321 mV	151 ps	Pass
30.0" total trace	237 mV	139 ps	Pass
40.0" total trace	168 mV	123 ps	Pass
41.0" total trace	162 mV	122 ps	Pass
42.0" total trace	157 mV	120 ps	Pass
43.0" total trace	149 mV	119 ps	Fail

Table 4 - PCI Express Connector Far-end Measurements, Normal Driver with -3dB de-emphasis.

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PCIE-TH Connector with Final Inch Design	Min RX Differential Voltage, A1 to -A1 ¹ (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	≥120 mV _{DIFFp-p}	≥120 ps	-
10.0" total trace	344 mV	149 ps	Pass
20.0" total trace	320 mV	149 ps	Pass
30.0" total trace	244 mV	144 ps	Pass
40.0" total trace	181 mV	133 ps	Pass
45.0" total trace	154 mV	126 ps	Pass
47.0" total trace	142 mV	122 ps	Pass
48.0" total trace	136 mV	121 ps	Pass
49.0" total trace	132 mV	119 ps	Fail

Table 5 - PCI Express Connector Far-end Measurements, Normal Driver with -4dB de-emphasis.

PCIE-TH Connector with Final Inch Design	Min RX Differential Voltage, A1 to -A1 ¹ (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	≥120 mV _{DIFFp-p}	≥120 ps	-
10.0" total trace	292 mV	146 ps	Pass
20.0" total trace	282 mV	146 ps	Pass
30.0" total trace	259 mV	146 ps	Pass
40.0" total trace	198 mV	143 ps	Pass
50.0" total trace	147 mV	134 ps	Pass
55.0" total trace	125 mV	126 ps	Pass
56.0" total trace	122 mV	124 ps	Pass
57.0" total trace	117 mV	121 ps	Fail

Table 6 - PCI Express Connector Far-end Measurements, Normal Driver with -5.5dB de-emphasis.

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PCIe-TH Connector with Final Inch Design	Min RX Differential Voltage, A1 to -A1 ¹ (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	≥120 mV_{DIFFp-p}	≥120 ps	-
10.0" total trace	263 mV	144 ps	Pass
20.0" total trace	261 mV	144 ps	Pass
30.0" total trace	243 mV	144 ps	Pass
40.0" total trace	204 mV	142 ps	Pass
50.0" total trace	158 mV	138 ps	Pass
55.0" total trace	137 mV	136 ps	Pass
57.0" total trace	130 mV	133 ps	Pass
59.0" total trace	121 mV	129 ps	Pass
60.0" total trace	119 mV	128 ps	Fail

Table 7 - PCI Express Connector Far-end Measurements, Normal Driver with -6.5dB de-emphasis.

Conclusions

When used with Samtec’s Final Inch® differential routing, breakout, and trace width solution, a single Samtec PCIe connector in a motherboard to daughter card configuration can be used to transfer PCI Express lanes with total trace lengths up to:

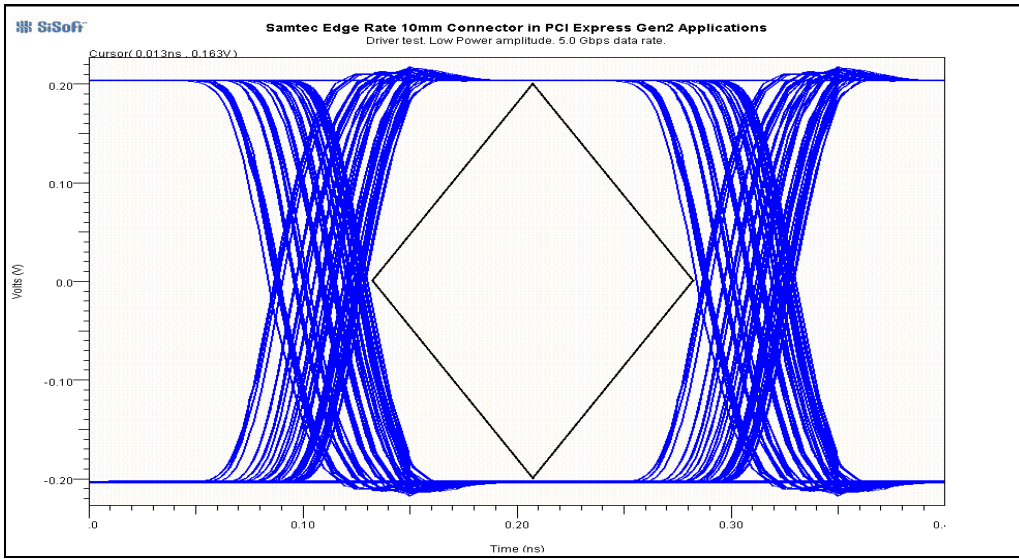
- 29 inches in low power driver mode.
- 42 inches when using a normal driver with -3 dB de-emphasis.
- 48 inches when using a normal driver with -4 dB de-emphasis.
- 56 inches when using a normal driver with -5.5 dB de-emphasis.
- 59 inches when using a normal driver with -6.5 dB de-emphasis.

Recommendations

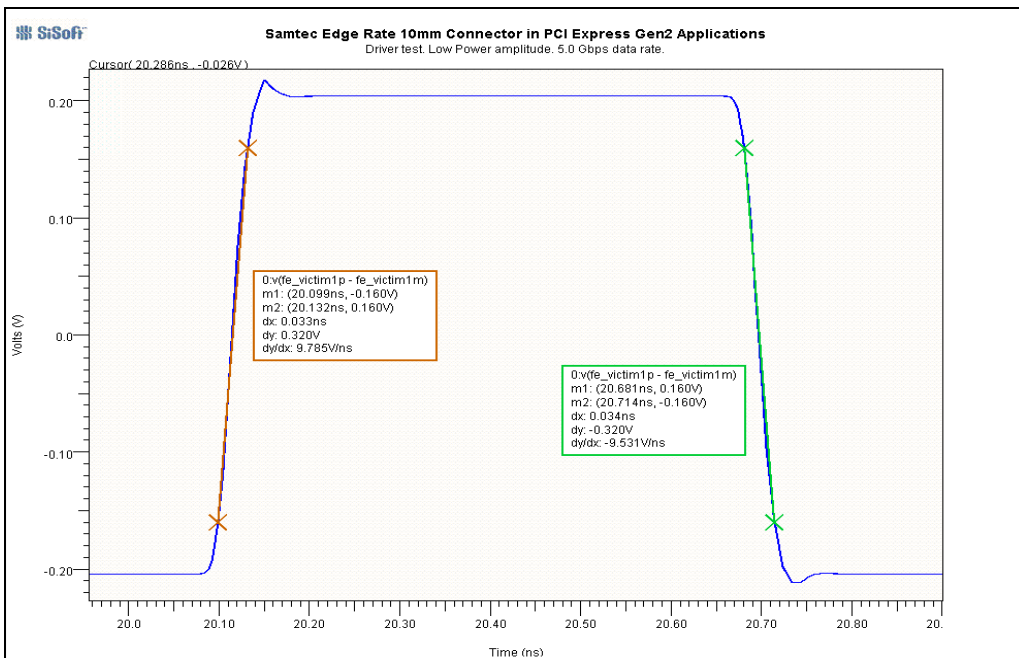
Designers should be aware that using smaller trace widths, laminates with higher loss tangent, and sub optimal routing solutions with higher pair-to-pair coupling and additional via stubs will decrease overall performance and the maximum allowable trace length. It is advisable, when designing systems that approach the maximum trace length limits, to perform detailed modeling, simulation, and measurement of the target design including the effects of material properties, traces, vias, and additional components.

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Appendix A – Waveform images

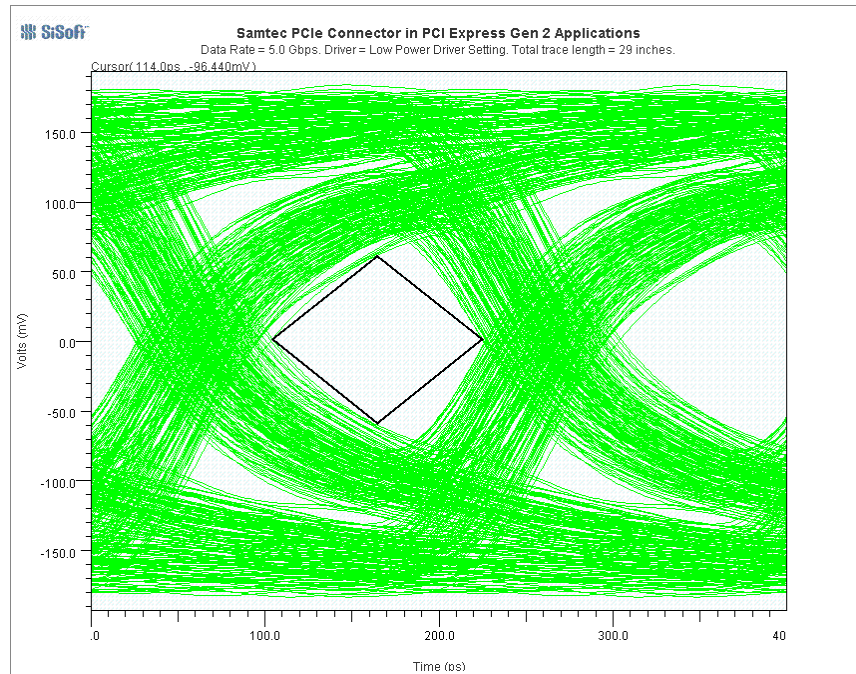


Picture A1 – Example of worst case stimulus eye waveform, probed at Teraspeed driver behavioral model nodes connected to PCIe compliance test/measurement load. Low power setting.

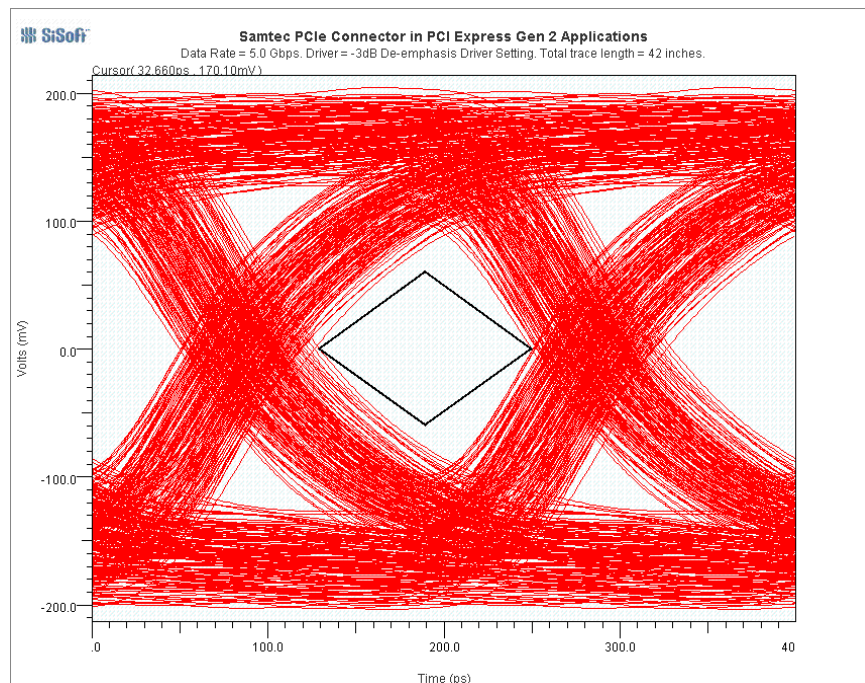


Picture A2 – Example of worst case stimulus measurement, probed at Teraspeed driver behavioral model nodes connected to PCIe compliance test/measurement load. Low power setting.

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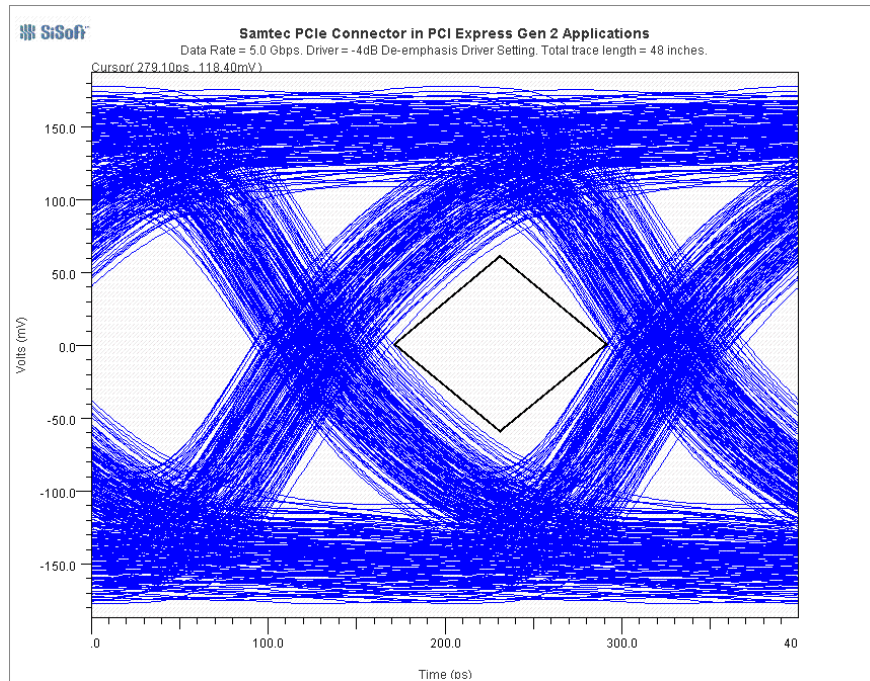


Picture A3 – Receiver eye measurement, probed at far end termination. Low power driver setting with 0 dB de-emphasis. Total trace length = 29 inches.

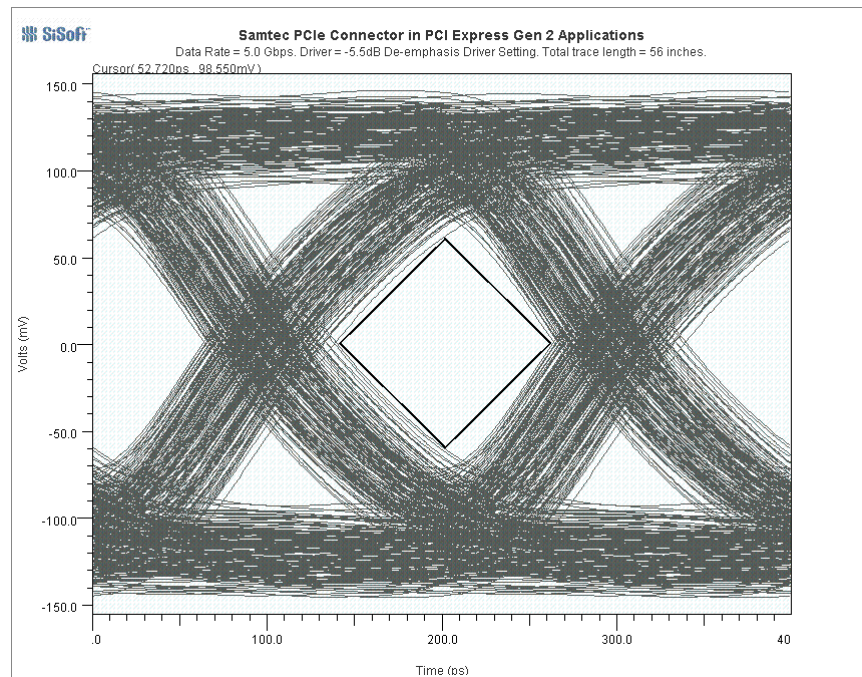


Picture A4 – Receiver eye measurement, probed at far end termination. Normal power driver setting with -3 dB de-emphasis. Total trace length = 42 inches.

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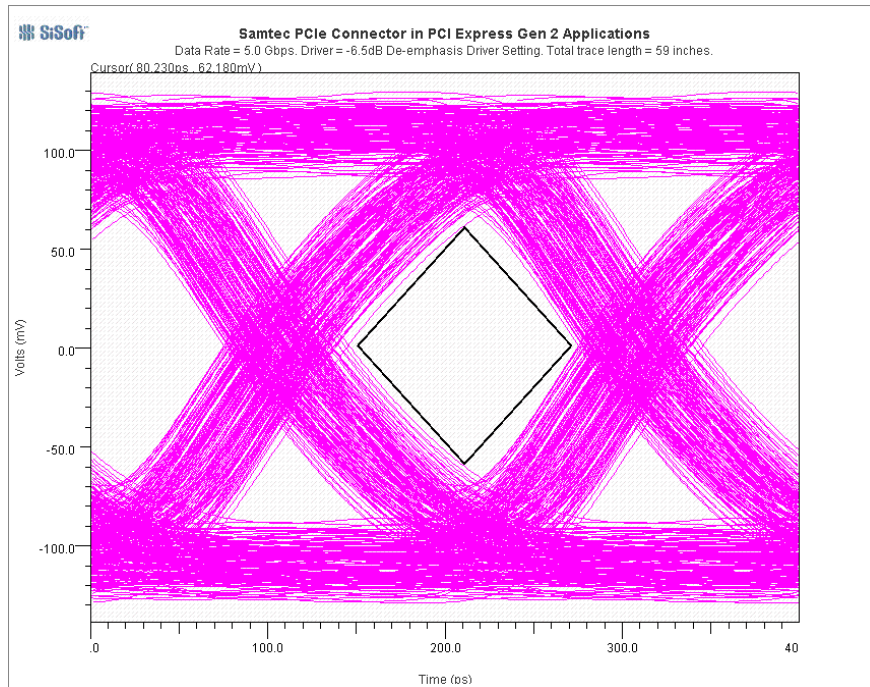


Picture A5 – Receiver eye measurement, probed at far end termination. Normal power driver setting with -4 dB de-emphasis. Total trace length = 48 inches.



Picture A6 – Receiver eye measurement, probed at far end termination. Normal power driver setting with -5.5 dB de-emphasis. Total trace length = 56 inches

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Picture A7 – Receiver eye measurement, probed at far end termination. Standard driver setting with -6.5 dB de-emphasis. Total trace length = 59 inches.