Application Note

QPairs® QTE-DP/QSE-DP 16mm Stack Height Final Inch™ Designs In PCI Express Applications Generation 2 – 5.0 Gbps

Revision Date: February 13, 2009

Developed in conjunction with
Teraspeed Consulting Group LLC

Series: QxE-DP, 16mm Stack Height
Standard: PCI Express, Generation 2

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Abstract

The PCI Express is primarily intended as a high performance serial interface targeted for use in desktop, mobile, workstation, server, communications platforms, and embedded devices. As with any modern high speed PCB design, the performance of an actual PCI Express interconnect is highly dependent on the implementation. This paper describes a measurement method applied to proven Samtec Final Inch® designs and this industry standard to help engineers deploy systems of two PCB cards mated through Samtec's family of high speed electrical connectors. To demonstrate the feasibility of using the Samtec QTE-DP/QSE-DP 16mm stack height connector with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in spreadsheet format. Also, trace lengths on the motherboard side of the QTE-DP/QSE-DP 16mm stack height connector will be gradually increased to show the limits of compliance.

In order to ensure interoperability between PCI Express transmitter and receiver devices, we will stress a typical interconnect design by stimulating their Spice model components and devices with worst case data patterns as described in Section 4.3.6.2.4 of PCI Express Base Specification, Rev 2.0. This paper will cover techniques to stress the system with reduced driver amplitude as well as max transmit jitter and noise injection.

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Introduction

Samtec has developed a full line of connector products that are designed to support serial speeds greater than 5.0 Gbps, the "Baud rate" of each PCI Express Generation 2 data lane. Working with Teraspeed Consulting, they have developed a complete breakout and routing solution for each member of Samtec's line of high speed connectors, called Final Inch®. To demonstrate the feasibility of using Samtec QxE-DP connectors in PCI Express applications with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in a user-friendly spreadsheet format. Trace lengths will be varied to show the limits of compliance.

Analysis will consist of stimulating a typical trace-connector-trace circuit path with a worst case signal and then observing the corresponding eye closure related to reflections due to impedance discontinuities, loss, and stubs. Next, utility software will be used to extract, analyze, and format Spice-measured voltage amplitudes and differential signal crossing times. Mask violations (see Figure 2) will be recorded in pass/fail format.

Definitions

Interconnect Budget – The amount of loss and jitter that is allowed in the interconnect and still meet the target specification.

Loss – The differential voltage swing attenuation from transmitter to receiver on the trace. The trace is subject to resistive, dielectric, and skin effect loss. Loss increases as trace length and and/or signal frequency increases. Vias and connectors also exhibit losses which must be included in the interconnect budget. Total loss allowed in the interconnect is 13.2 dB.

Jitter – The variation in the time between differential crossings from the ideal crossing time. Jitter includes both data dependent and random contributions on the interconnect. Total jitter allowed is 0.4UI, or 80 ps when UI = 200 ps.

PRBS – Pseudo Random Bit Sequence.

Tj – Total jitter, which is the convolution of the probability density functions for all the jitter sources, Random jitter (Rj) and Deterministic jitter (Dj). The UI allocation is given as the allowable Tj. The PCI Express specification does not specify allocation of Rj and Dj.

UI – Unit Interval. The time interval required for transmission of one data symbol. For a binary lane operating at 5.0 Gbps, the UI is 200 ps.

V_{DIFF} – Differential voltage, defined as the difference of the positive conductor voltage and the negative conductor voltage (V_{D+} - V_{D-}).

$V_{DIFFp-p}$ – Differential peak-to-peak voltage, defined by the following equations:

$$V_{DIFFp-p} = (2*\max | V_{D+} - V_{D-} |)$$ (Applies to a symmetric differential swing)

$$V_{DIFFp-p} = (\max | V_{D+} - V_{D-} | \{ V_{D+} > V_{D-} \} + \max | V_{D+} - V_{D-} | \{ V_{D+} < V_{D-} \})$$
(Applies to a asymmetric differential swing)

The PCI Express Specification

PCI Express links are based on recent advances in point-to-point interconnect technology. A PCI Express link is comprised of a dual-simplex communications channel between two components physically consisting of two low-voltage, differential signal pairs. The PCI Express Base Specification defines one half of a link (one transmitter and receiver) an electrical sub-block. The design model used for this paper is of three electrical sub-blocks operating in tandem, the victim surrounded by multiple aggressors, with all bit streams heading in the same direction.

Detailed specifications for an electrical sub-block can be found in the PCI Express 2.0 Base Specification and will be referred to throughout the rest of this paper[1]. Measurement techniques specified in this section have been rigidly adhered to including the requirement for finding the median within the jitter for use in jitter measurements.

[1] The PCI Express Base 2.0 specification is available for purchase though the PCI Sig organization (http://www.pcisig.com/specifications/ordering_information).

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Setup and Measurement

Input Stimulus Setup

A PRBS 2^7-1 pattern was used for victim stimulus pair and a repeating 1010… pattern used for the aggressor pairs surrounding the victim pair. Teraspeed has developed its own stimulus conversion tool that has the capability to selectively de-emphasize and/or add jitter to the HSICE stimulus output, such as a vector file. This was used to add enough jitter and de-emphasis to just meet worst case PCI Express Generation 2 transmit jitter specifications.

The Test Circuit Model

The test circuit modeled is shown in Figure 1. It consists of the following:

- One set of Teraspeed behavioral driver models with programmable edge rate, amplitude, and de-empgasis.
- One set of six AC coupling capacitors, value = 100 nF
- 1 QxE-DP Final Inch™ design, comprised of the QTE-DP/QSE-DP connector model surrounded by the Samtec's BOR models, lossy trace models (7.5mil; stripline; FR4) and SMA connector models on both sides of the connector.
- 50 Ohm termination resistors to Ground (as required per Note 7 in Section 4.3.4 of the PCI Express Base Specification, Rev 1.0a.

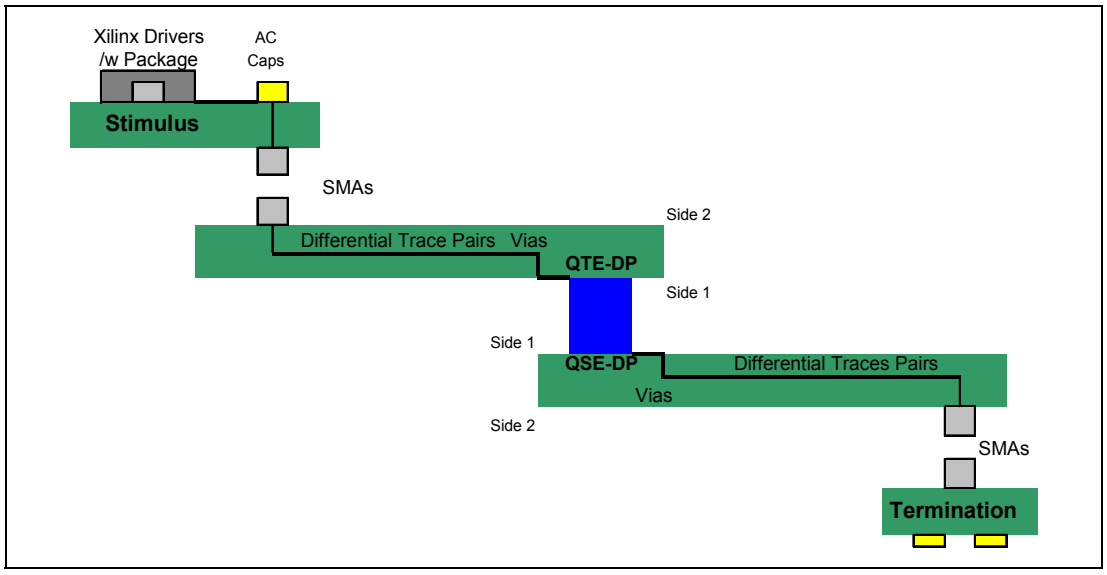

Figure 1 - PCI Express Test Circuit

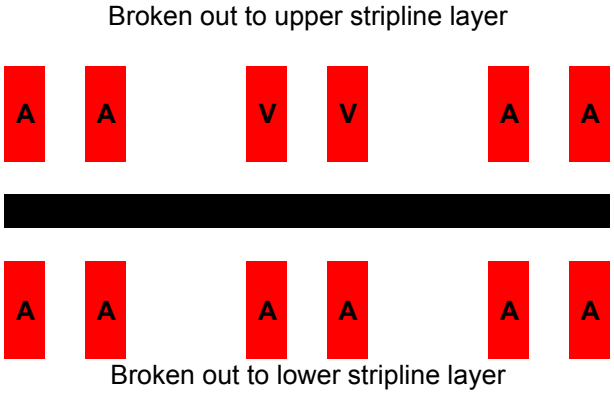

Figure 2 – QxE-DP connector test cases pad patterns for HSPICE simulations. V = Victim, A = Aggressor. Black = grounded connections.

Procedure

Interconnect Budget

The interconnect budget can be best illustrated by the mask shown in Figure 3. In order to pass the PCI Express constraints for loss and jitter, the simulated eye waveform must not touch any location within the grey areas shown. Calculated interconnect budget values are shown in Table 1.

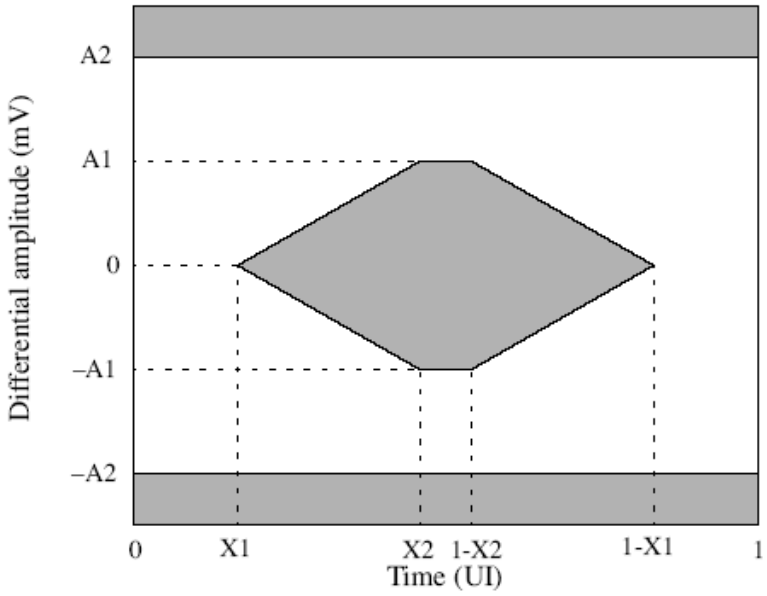

Figure 3 - Example eye mask template

	Low Power Differential Maximum Loss, A1 to –A1 (See example mask template) ($V_{DIFFp-p}$)	Normal Power Differential Maximum Loss, A1 to –A1 (See example mask template) ($V_{DIFFp-p}$)	Minimum Eye Width, X1 to 1-X1 (See example mask template) (UI_{p-p})
Driver at Package Pin	0.400	0.800	0.75
Receiver at Package Pin	0.120	0.120	0.60[2]
Interconnect budget:	10.5 dB loss	16.5 dB loss[1]	0.15 UI (30ps when UI = 200 ps)

Table 1 - PCI Express Gen 2 interconnect budgets: max loss and min eye width calculated values

[1]The worst case operational loss budget at 2.5 GHz Nyquist frequency is calculated by taking the minimum driver output voltage ($V_{TX-DIFFp-p}$ = 800 mV) divided by the minimum input voltage to the receiver ($V_{RX-DIFFp-p}$ = 175 mV). 175/800 = .219, which after conversion results in a maximum loss budget of 13.2 dB.

[2]Minimum width pulse at Rx after accounting for worst Tj at 10^{-12} BER. See Table 4-12 in the PCI Express Base Specification, Revision 2.0.

Transmitter Compliance Measurements

Setup for Tj for UI Measurements

Before the PCI Express circuit model can be simulated and measured, we must first set up the driver stimulus to provide minimum TX eye width (maximum jitter) and minimum amplitude for both low power and regular power driver models. As mentioned in the previous section, the driver stimulus' jitter can be adjusted until it just reaches the maximum total jitter allowed under the compliance load shown in the figure below. The AC coupling capacitor C_{TX} can be set anywhere between 75pF and 200pF. We set C_{TX} to 100nF for all simulations because it is a popular value in the industry. Table 2 shows the resulting output measurements. The eye pattern generated in the PCI Express driver compliance test simulation can be found in Appendix A, Picture 1, of this paper.

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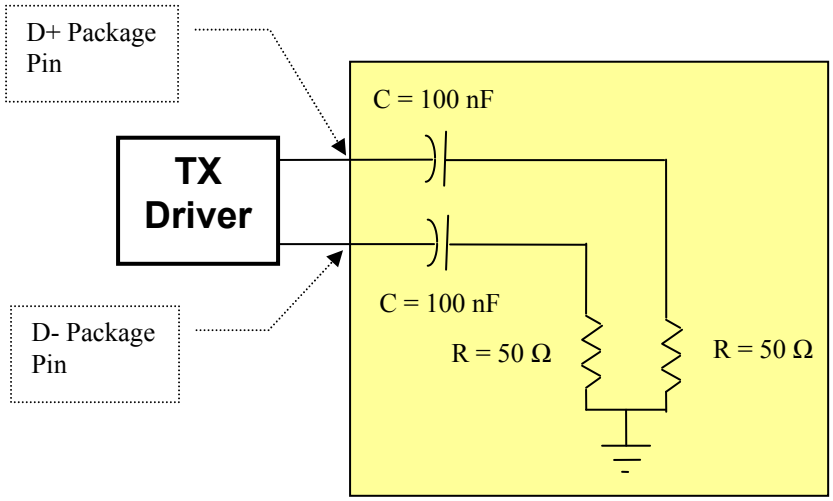

Figure 4 - PCI Express Compliance Test/Measurement load

De-emphasis		$Vdiff_{p-p}$		Total Jitter	Edge Rate
		Transition Bit	De-emphasized Bit	≤0.25 UI, measured at crossings	≥0.15 UI, measured 20% to 80%
0dB (Low Power)	Specification	≥400 mV	None	≤50 ps	≥30 ps
	Measured	401 mV[1]	-	46 ps	34 ps
-3 dB	Specification	≥800 mV	≥566 mV	≤50 ps	≥30 ps
	Measured	800 mV[1]	566 mV	49 ps	30 ps
-4 dB	Specification	≥800 mV	≤505 mV	≤50 ps	≥30 ps
	Measured	800 mV[1]	505 mV	49 ps	30 ps
-5.5 dB	Specification	≥800 mV	≥425 mV	≤50 ps	≥30 ps
	Measured	800 mV[1]	425 mV	49 ps	30 ps
-6.5 dB	Specification	≥800 mV	≤378 mV	≤50 ps	≥30 ps
	Measured	800 mV[1]	378 mV	49 ps	30ps

Table 2- PCI Express TX Silicon + Package Measurements at Package Pin

[1]The PCI Express Base Specification defines X2 to 1-X2 = 0. The minimum TX height measurements were taken at mid bit.

Measurements at the Receiver

Notes:

1.) The total trace length specified is the sum of the mother board and daughter card differential traces as shown in Figure 1. Both trace lengths are equal in each simulation.

2.) For each of the following tables, the eye patterns generated in the PCI Express circuit simulation with the maximum allowable total trace length in each of the following table can be found in Appendix A of this paper.

PCI Express with QxE-DP 16mm Connector Final Inch Circuit	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	**≥120 $mV_{DIFFp-p}$**	**≥120 ps**	-
5.0" total trace	291 mV	143 ps	Pass
10.0" total trace	232 mV	139 ps	Pass
15.0" total trace	182 mV	131 ps	Pass
20.0" total trace	142 mV	122 ps	Pass
21.0"total trace	137 mV	120 ps	Fail
22.0" total trace	128 mV	117 ps	Fail

Table 3 - PCI Express Connector Far-end Measurements, Low Power Driver.

PCI Express with QxE-DP 16mm Connector Final Inch Circuit	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	**≥120 $mV_{DIFFp-p}$**	**≥120 ps**	-
10.0" total trace	389 mV	144 ps	Pass
20.0" total trace	281 mV	140 ps	Pass
30.0" total trace	192 mV	125 ps	Pass
31.0" total trace	180 mV	123 ps	Pass
32.0" total trace	177 mV	121 ps	Pass
33.0" total trace	167 mV	119 ps	Fail

Table 4 - PCI Express Connector Far-end Measurements, Normal Driver with -3dB de-emphasis.

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PCI Express with QxE-DP 16mm Connector Final Inch Circuit	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	**≥120 $mV_{DIFFp-p}$**	**≥120 ps**	-
10.0" total trace	355 mV	142 ps	Pass
20.0" total trace	289 mV	140 ps	Pass
30.0" total trace	204 mV	132 ps	Pass
32.0" total trace	190 mV	129 ps	Pass
34.0" total trace	177 mV	126 ps	Pass
36.0" total trace	162 mV	123 ps	Pass
37.0" total trace	156 mV	121 ps	Pass
38.0" total trace	149 mV	119 ps	Fail

Table 5 - PCI Express Connector Far-end Measurements, Normal Driver with -4dB de-emphasis.

PCI Express with QxE=DP 16mm Connector Final Inch Circuit	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	**≥120 $mV_{DIFFp-p}$**	**≥120 ps**	-
10.0" total trace	305 mV	139 ps	Pass
20.0" total trace	278 mV	137 ps	Pass
30.0" total trace	219 mV	135 ps	Pass
40.0" total trace	161 mV	130 ps	Pass
42.0" total trace	149 mV	126 ps	Pass
44.0" total trace	137 mV	123 ps	Pass
45.0" total trace	133 mV	122 ps	Pass
46.0" total trace	128 mV	120 ps	Pass
47.0" total trace	123 mV	117 ps	Fail

Table 6 - PCI Express Connector Far-end Measurements, Normal Driver with -5.5dB de-emphasis.

Series: QxE-DP, 16mm Stack Height
Standard: PCI Express, Generation 2

PCI Express with QxE-DP 16mm Connector Final Inch Circuit	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Pass/Fail
Specification	≥120 $mV_{DIFFp-p}$	≥120 ps	-
10.0" total trace	277 mV	137 ps	Pass
20.0" total trace	257 mV	136 ps	Pass
30.0" total trace	225 mV	134 ps	Pass
40.0" total trace	172 mV	131 ps	Pass
50.0" total trace	122 mV	124 ps	Pass
51.0" total trace	117 mV	122 ps	Fail

Table 7 - PCI Express Connector Far-end Measurements, Normal Driver with -6.5dB de-emphasis.

Conclusions

When used with Samtec's Final Inch® differential routing, breakout, and trace width solution, a single Samtec QxE-DP 16mm connector set in a board to board configuration can be used to transfer PCI Express lanes with total trace lengths up to:

- 21 inches in low power driver mode.
- 32 inches when using a normal driver with -3 dB.de-emphasis.
- 37 inches when using a normal driver with -4 dB de-emphasis.
- 46 inches when using a normal driver with -5.5 dB de-emphasis.
- 50 inches when using a normal driver with -6.5 dB de-emphasis.

Recommendations

Designers should be aware that using smaller trace widths, laminates with higher loss tangent, and sub optimal routing solutions with higher pair-to-pair coupling and additional via stubs will decrease overall performance and the maximum allowable trace length. It is advisable, when designing systems that approach the maximum trace length limits, to perform detailed modeling, simulation, and measurement of the target design including the effects of material properties, traces, vias, and additional components

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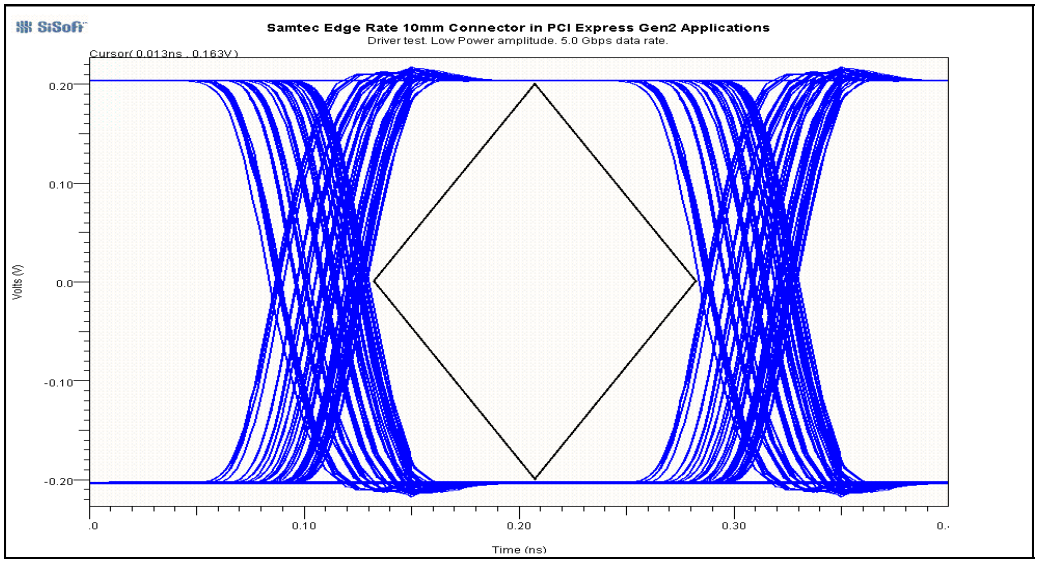
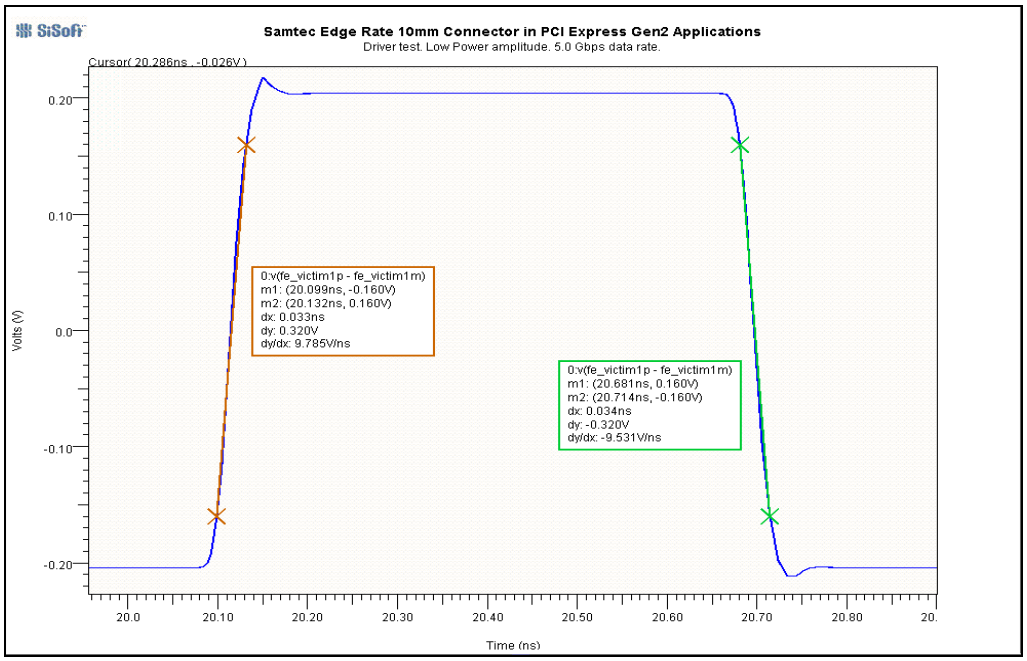
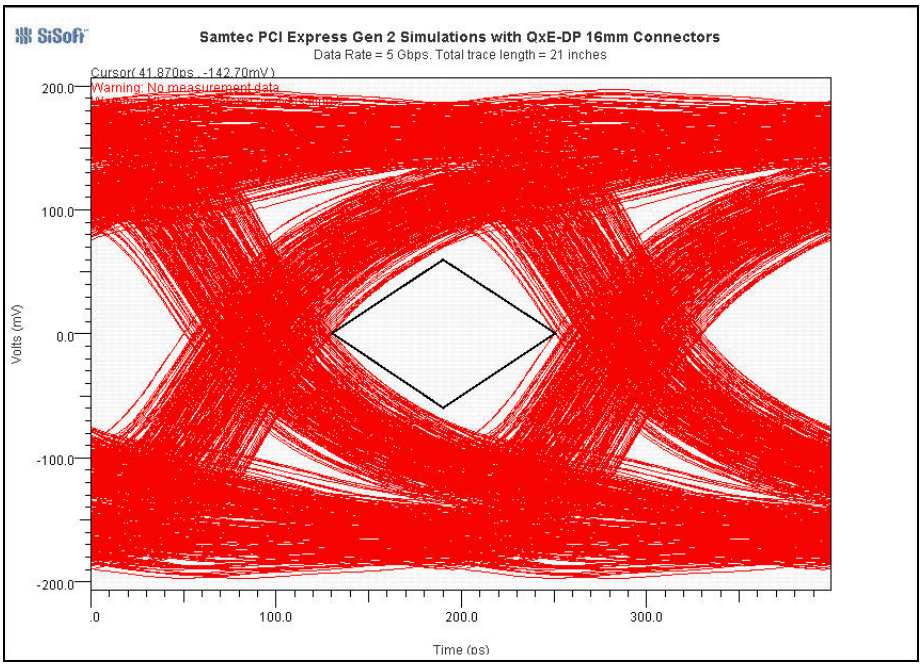
Appendix A – Waveform images



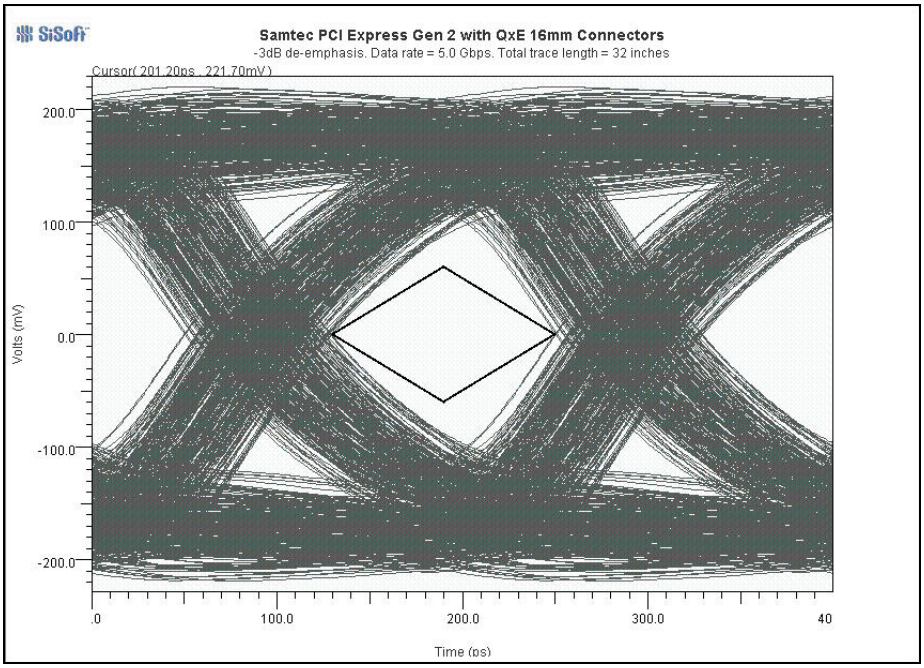
Picture 1 – Example of worst case stimulus eye waveform, probed at Teraspeed driver behavioral model nodes connected to PCIe compliance test/measurement load. Low power setting.



Picture 2 – Example of worst case stimulus edge rate measurement, probed at Teraspeed driver behavioral model nodes connected to PCIe compliance test/measurement load. Low power setting.



Picture 3 – Receiver eye measurement, probed at far end termination. Low power driver setting with 0 dB de-emphasis. Total trace length = 21 inches.



Picture 4 – Receiver eye measurement, probed at far end termination. Normal power driver setting with -3 dB de-emphasis. Total trace length = 32 inches.

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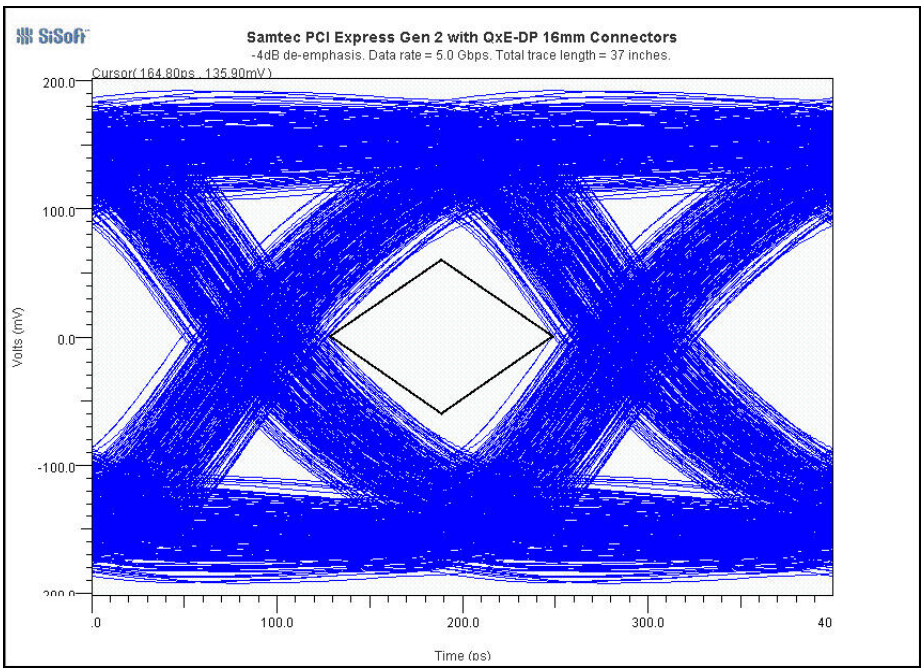
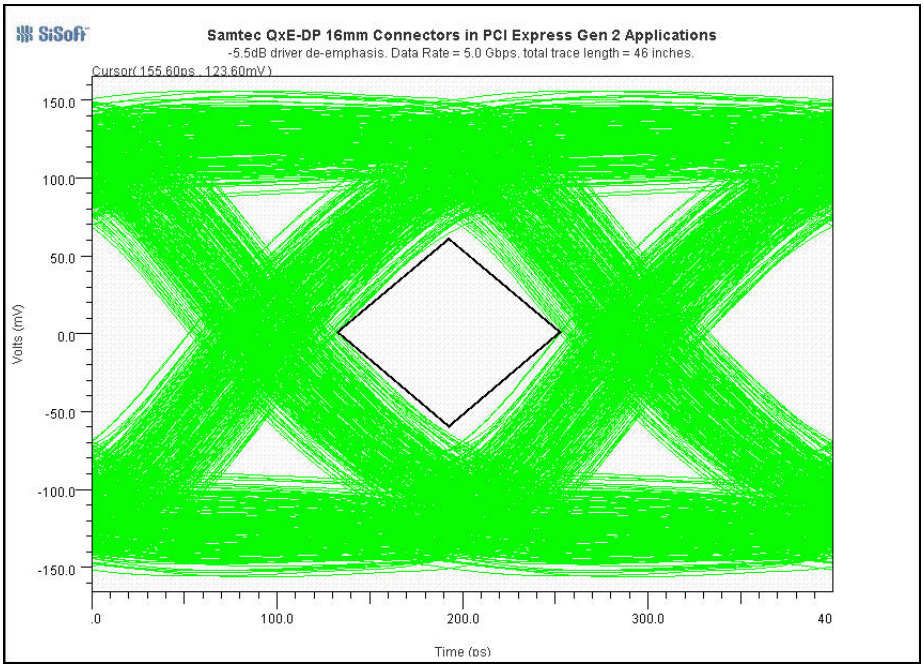


Picture 5 – Receiver eye measurement, probed at far end termination. Normal power driver setting with -4 dB de-emphasis. Total trace length = 37 inches.



Picture 6 – Receiver eye measurement, probed at far end termination. Normal power driver setting with -5.5 dB de-emphasis. Total trace length = 46 inches

Picture 7 – Receiver eye measurement, probed at far end termination. Standard driver setting with -6.5 dB de-emphasis. Total trace length = 50 inches.