Application Note

DP Array™ DPAM/DPAF Final Inch® Designs in Serial ATA Generation 1 Applications 10mm Stack Height

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Developed in conjunction with
Teraspeed Consulting Group LLC

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Abstract

The Serialized AT Attachment Interface (Serial ATA or SATA) is primarily intended as a low voltage, point-to-point, serialized replacement to legacy ATA, the parallel interface used for years to connect hard drives to CPU mother boards. Cable lengths are comparable to parallel ATA (<1 m at 1.5 Gbits/sec bit rate). As with any modern high speed PCB design, the performance of an actual Serial ATA interconnect is highly dependent on the implementation. This paper describes a measurement method applied to proven Samtec Final Inch® designs and this industry standard to help engineers deploy systems of two PCB cards mated through Samtec's family of high speed electrical connectors. To demonstrate the feasibility of using Samtec DP Array™ DPAM/DPAF Series connectors with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in spreadsheet format. Also, trace lengths on each side of the DPAM/DPAF Series connector will be gradually increased to show the limits of compliance.

In order to ensure interoperability between Serial ATA transmitter and receiver devices, we will show that our Final Inch® test fixture meets all success criteria documented in **Table 4 – Signal integrity requirements and test procedures** in the Serial ATA specification, Revision 1.0a, 7-January-2003. These requirements are intended for testing of cable designs, so to stay true to the SATA specifications intent, the requirements will be met for the entire signal path from the near-end SMA connectors to the far-end SMA connectors (see fixture illustration, Figure 1). Trace lengths will be varied to show the limits of compliance.

Introduction

Samtec has developed a full line of connector products that are designed to support serial speeds up to and greater than 1.5 Gbps, the "Baud rate" of each Generation 1 Serial ATA data lane. Working with Teraspeed Consulting, they have developed a complete breakout and routing solution for each member of Samtec's line of high speed connectors, called Final Inch®. To demonstrate the feasibility of using Samtec DP Array™ DPAM/DPAF Series connectors in Serial ATA applications with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in a user-friendly spreadsheet format. Trace lengths will be varied to show the limits of compliance.

Analysis will consist of stimulating a typical trace-connector-trace circuit path with a worst case signal and then observing the corresponding eye closure related to reflections due to impedance discontinuities, loss, and stubs. Next, utility software will be used to extract, analyze, and format Spice-measured voltage amplitudes and differential signal crossing times. Mask violations will be recorded in pass/fail format.

Definitions

Crosstalk - Disturbance caused by the electric or magnetic fields of one telecommunication signal affecting a signal in an adjacent circuit. The phenomenon that causes crosstalk is called electromagnetic interference (EMI). It can occur in microcircuits within computers and audio equipment as well as within network circuits. The term is also applied to optical signals that interfere with each other.

DJ - Deterministic Jitter (peak to peak). All jitter sources that do not have tails on their probability distribution function (i.e. values outside the bounds have probability zero). Four kinds of deterministic jitter are identified: duty cycle distortion, data dependent (ISI), sinusoidal, and uncorrelated (to the data) bounded. DJ is characterized by its bounded, peak-to-peak value.

Interconnect Budget – The amount of loss and jitter that is allowed in the interconnect and still meet the target specification.

Loss – The differential voltage swing attenuation from transmitter to receiver on the trace. The trace is subject to resistive, dielectric, and skin effect loss. Loss increases as trace length and and/or signal frequency increases. Vias and connectors also exhibit losses which must be included in the interconnect budget.

Insertion Loss - The loss resulting from the insertion of a device in a transmission line, expressed as the reciprocal of the ratio of the signal power delivered to that part of the line following the device to the signal power delivered to that same part before insertion. Insertion loss is usually expressed in dB.

Jitter – The variation in the time between differential crossings from the ideal crossing time. Jitter includes both data dependent and random contributions on the interconnect.

PRBS – Pseudo Random Bit Sequence.

RJ - Random Jitter (peak to peak). Assumed to be Gaussian and equal to 14 times the 1σ rms value given the 10^{-12} BER requirement.

TJ – Total jitter, which is the convolution of the probability density functions for all the jitter sources, Random jitter (RJ) and Deterministic jitter (DJ). The UI allocation is given as the allowable TJ.

UI – Unit Interval. The time interval required for transmission of one data symbol. For a binary lane operating at 3.125 Gbps, the UI is 320 ps.

$\mathbf{V_{DIFF}}$ – Differential voltage, defined as the difference of the positive conductor voltage and the negative conductor voltage (V_{D+} - V_{D-}).

The Serial ATA Specification

Serial ATA links are based on recent advances in point-to-point interconnect technology. A Serial ATA lane is comprised of a dual-simplex communications channel between two components physically consisting of two low-voltage, differential signal pairs. One lane is used to convey self-clocking data and control, each at a nominal rate of ~1.5 GB/s.

The Serial ATA specification, errata, and design guidelines can be downloaded free of charge at the organization's web site, http://www.serialata.org/ . Detailed physical layer electrical specifications for the Serial ATA can be found starting in Section 6.6.2 for the specification. Relevant timing and voltage constraints from this section of the specification will be referred to in the section on validating the DPAM/DPAF Series DP Array™ Final Inch® Test Fixture when used as a complete system.

DP Array™ Final Inch® Test Fixture Validation When Used As a Substitute for the SATA Cable

Readers may be interested in how the DPAM/DPAF Series DP Array™ test fixture fares when it is used in place of the Serial ATA cable. The Serial ATA specification makes this fairly easy to ascertain, as cable signal integrity requirements can be found in Table 4 of Section 6.3.6**,** Serial ATA cable**.** The following table summarizes the requirements to be met, and which ones apply to Spice simulation and measurement.

Parameter	Requirement	Relevant to fixture Spice Model?
Mated connector impedance	100 ohm +/- 15% @ Trise=70ps (20%-80%)	Yes
Cable absolute impedance	100 ohm +/- 10% @ Trise=70ps (20%-80%)	Yes
Cable pair matching	+/- 5 ohm	No
Common mode impedance	25 to 40 ohms @ Trise=70ps (20-80)	Yes
Insertion loss	6 dB max @ 4.5 Ghz	Yes
Crosstalk: NEXT	-26 dB @ 4.5 Ghz	Yes
Rise time	85 ps maximum	Yes
Inter-symbol Interference	50 ps maximum	Yes
Intra-Pair Skew	10 ps max	No

Table 1 - Serial ATA Signal Integrity Requirements

Setup and Measurement

The DPAM/DPAF Series Test Circuit Model

The DPAM/DPAF Series test circuit modeled is shown in Figure 1. It consists of the following:

- DPAM/DPAF Series DP Array™ mated connector model for part numbers DPAM-23-10-H-8-1 and DPAF-23-01-H-8-1
- BOR models for DPAM side and DPAF side, short via stubs
- Trace models, variable lengths

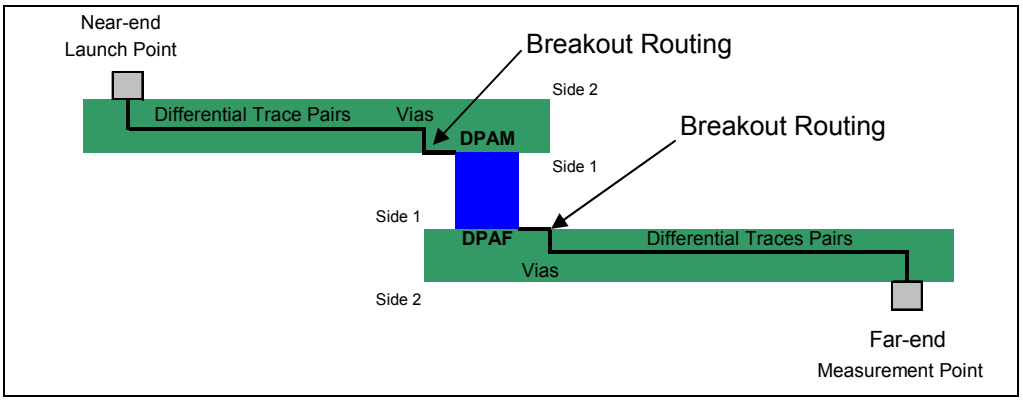


Figure 1 DPAM/DPAF Series DP Array™ Final Inch® Test Fixture

Test Procedure

Insertion Loss

We deliberately did the insertion loss simulations first to determine the maximum total test fixture trace length we could reliably use for the rest of the procedure. For this measurement, we connected the differential pair input to a 1Volt a.c. stimulus, linearly

swept from 10 MHz to 4.5 GHz. The far-end of the test fixture was terminated differentially at the measurement point, value=100 Ohms. The extra differential pairs on either side of the circuit under test were terminated at both end points, 50 Ohms to Ground. Results for various total trace lengths are shown in Figure 2. Both near-end and far-end trace lengths were kept equal for each measurement.

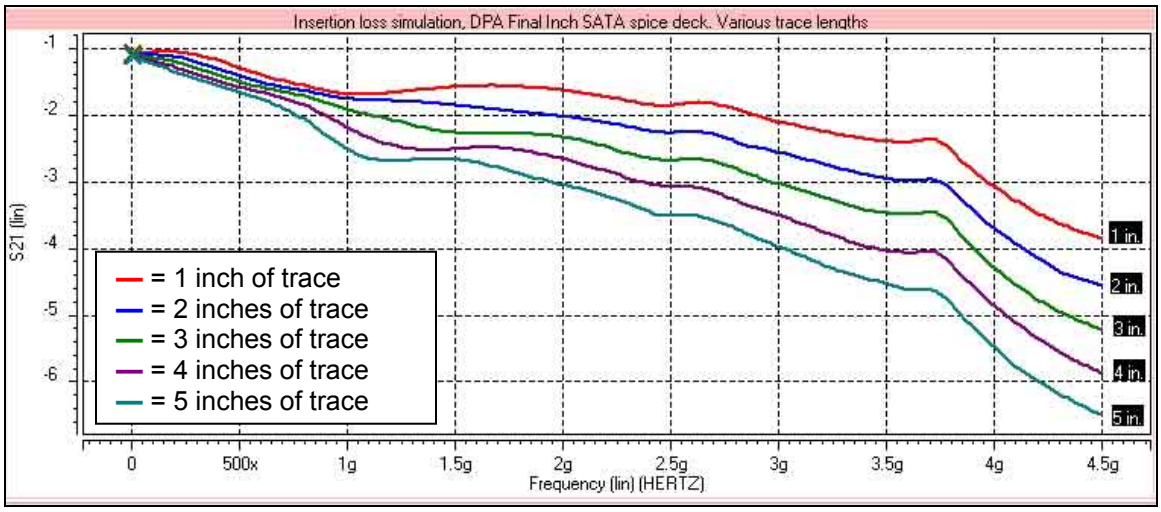


Figure 2 – Serial ATA circuit insertion loss

The Serial ATA test circuit meets the insertion loss specification if total trace lengths are kept at or below 4 inches. We will use 4 inches total trace length in the rest of the test procedure.

Readers may be curious to know how much of this loss is from the connector/BOR and how much can be contributed to the traces. Figure 3 shows the insertion loss with our 4 inches of trace, with (blue) and without (red) the connector and breakout regions present. At 4.5 Ghz the connector and breakout add 3.35 dB of insertion loss.

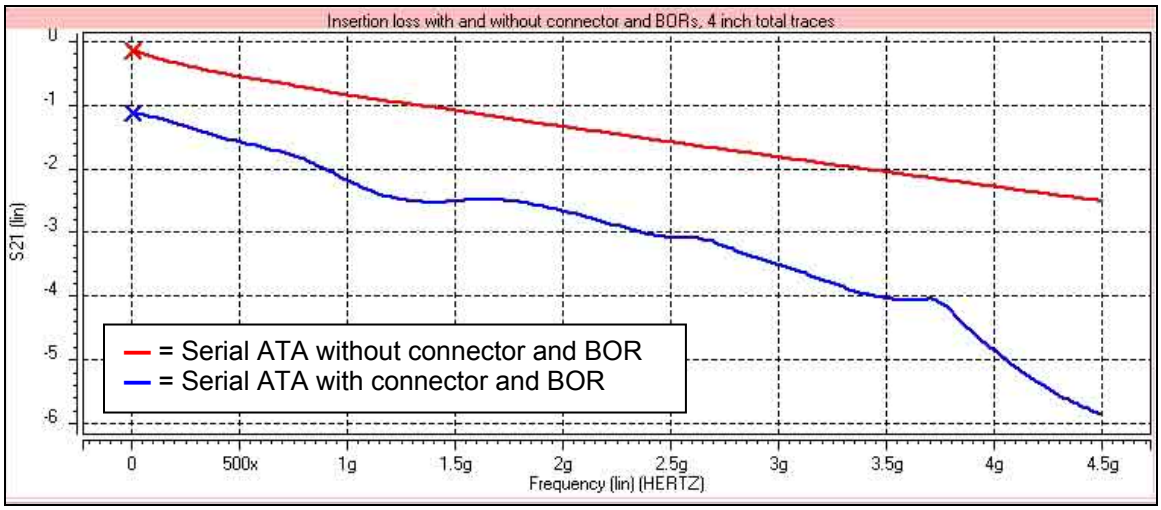


Figure 3 - Insertion loss comparison of 4 inch trace with and without connector and breakout

Crosstalk: NEXT

To test near-end crosstalk, all of the test fixtures' differential pairs were configured in an aggressor-victim-passive setup. Figure 4 shows the location of the victim pair on the connector.

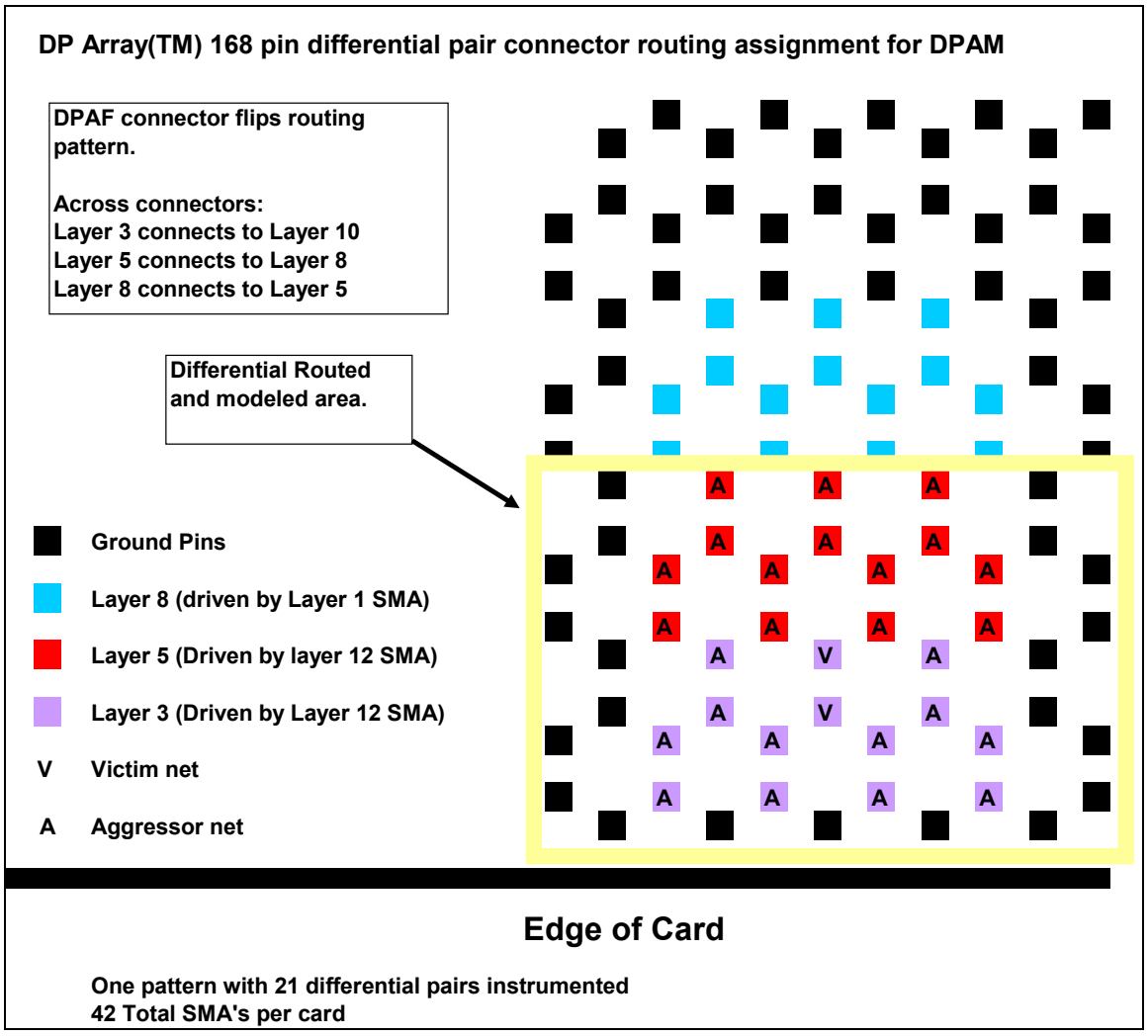


Figure 4 - DPAM/DPAF Series differential connector pin pattern

Results for 4 inches total trace length are shown in Figure 5.

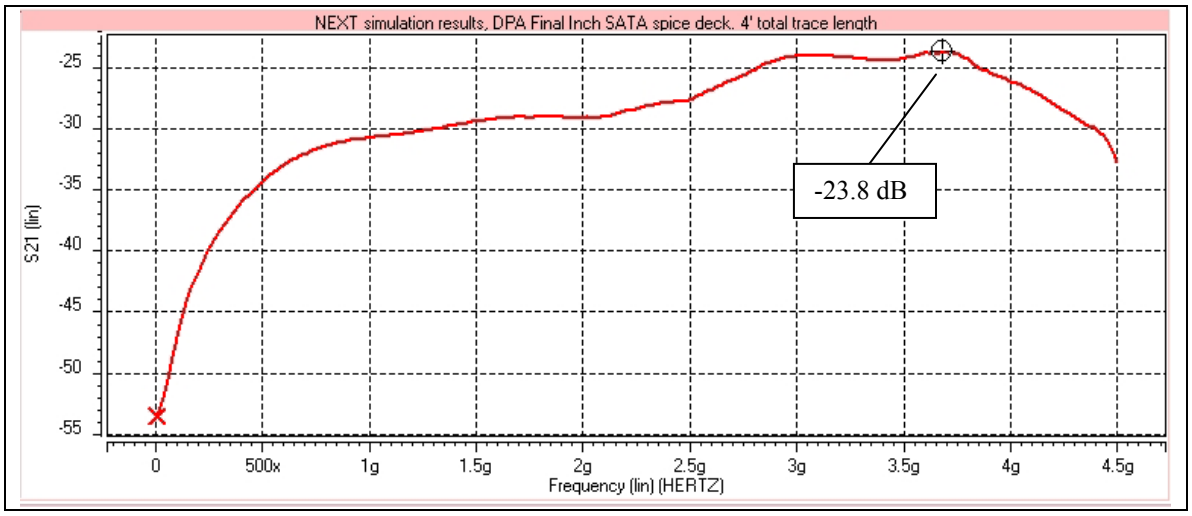


Figure 5 – DPAM/DPAF Series 10mm circuit NEXT simulation results, 4 inches total trace length

The DPAM/DPAF Series 10mm stack Serial ATA test circuit does not meet the near-end crosstalk requirement of -26 dB.

Mated Connector Impedance

The following figure shows the TDR response for the DPAM/DPAF Series 10mm stack connector set when used in the Final Inch® circuit. Note that 50 Ohm T-element traces were used on each side of the connectors with delays set to 250 ps.

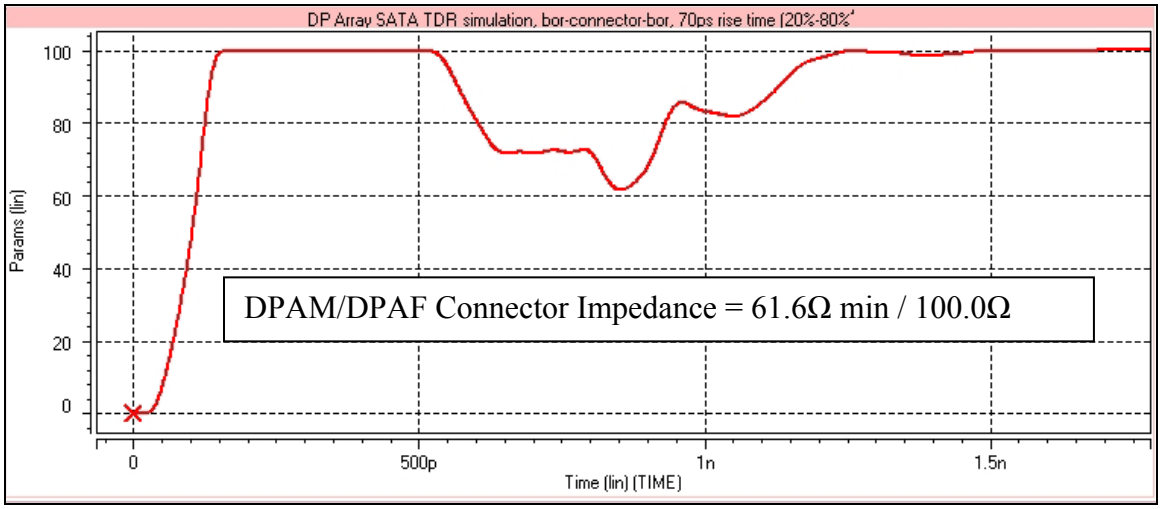


Figure 6 – DPAM/DPAF Series 10mm Connector TDR results

The DPAM/DPAF Series connector set does not meet the impedance criteria of 100 ohms +/-15%.

Final Inch® Circuit Absolute Impedance

The results of the full circuit TDR is shown in Figure 7 below.

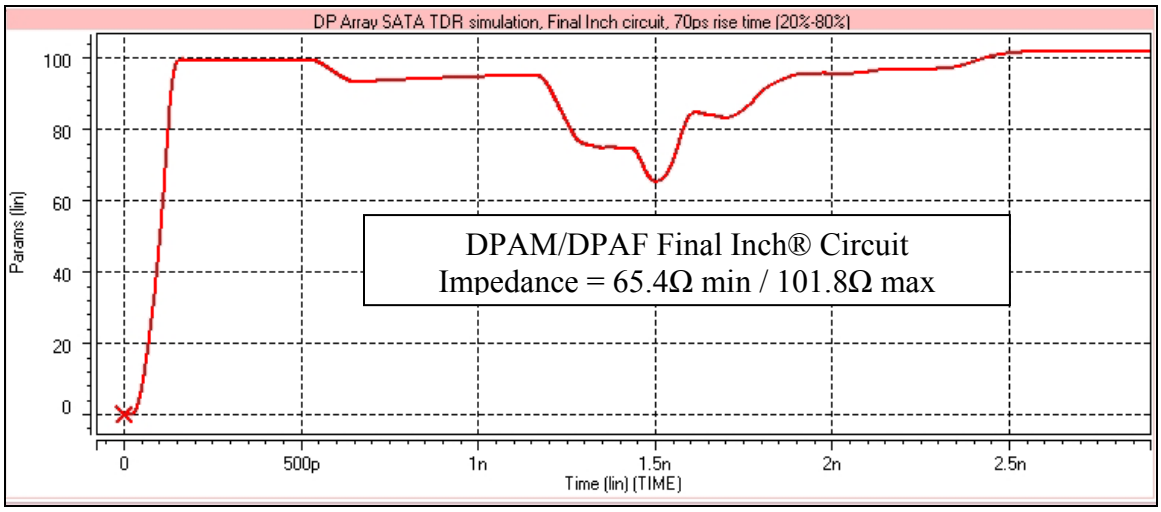


Figure 7 – DPAM/DPAF Series Final Inch® circuit TDR results

The DPAM/DPAF Series Final Inch® circuit does not meet the impedance criteria of 100 ohms +/-10% set forth in the Serial ATA Specification for cable compliance.

Common Mode Impedance

To determine the common mode impedance, we set both TDR pulsers to produce positive going pulses, then measured the even mode impedance of each signal in the differential pair. The common mode impedance is determined by dividing the results by 2.

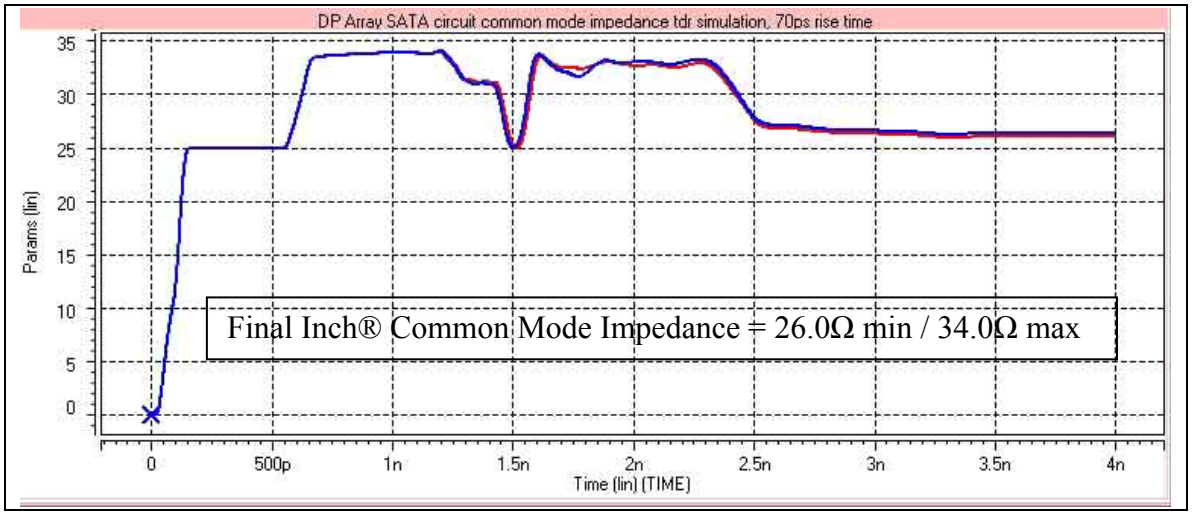


Figure 8 – DPAM/DPAF Final Inch® circuit common mode impedance

The DPAM/DPAF Series Final Inch® circuit meets the specified common mode range of 25 to 40 ohms.

Rise Time

The Serial ATA specification indicates that the far-end rise time requirement is 85 ps maximum. With a synthetic driver set to the minimum allowed 25 ps rising edge rate, the results indicate the Final Inch® circuit with 4 inches total trace length is well within the maximum allowed 85 ps far-end edge rate. The transmitter and receiver edges are shown in Figure 9 below.

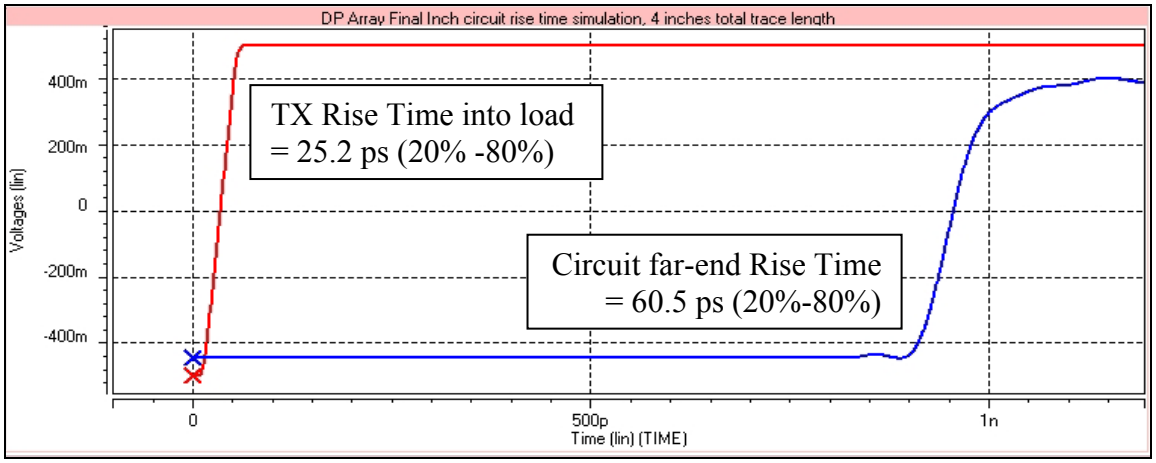


Figure 9 – DPAM/DPAF Series Final Inch® circuit rise time results with 4 inches total trace length. Red = TX driving compliance load. Blue = Final Inch® circuit probed at the far-end termination

Inter-symbol Interference

To test the inter-symbol interference requirement of +/-50 ps maximum, a PRBS 2^7-1 pattern was used for the victim pair stimulus and a repeating 1010… pattern used for the aggressor pairs on each side of the victim pair. Utility software was then used to extract, analyze, and format Spice-measured differential signal crossing times. The resulting eye waveform is shown in Figure 10, along with the measured jitter value.

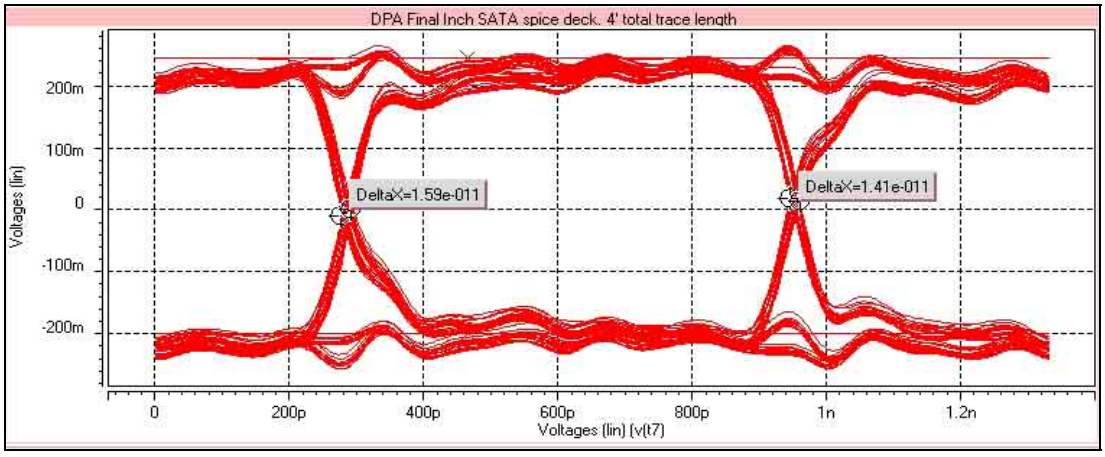


Figure 10 – DPAM/DPAF Series Final Inch® circuit eye

The Serial ATA test circuit easily meets the inter-symbol interference jitter requirement of not more than +/-50 ps

Conclusions

The Samtec DP Array™ DPAM/DPAF Series 10mm stack height connector, set in a Final Inch® TX board/RX board configuration, does not meet the Serial ATA compliance specification for system cables. One should keep in mind that the Serial ATA specification defines the cable to be 26 or 30 AWG. The trace geometry used on the Final Inch PCBs is the equivalent to approximately 42AWG (based on 4 mil wide traces; 1 0z Cu thickness). The equivalent trace width (1 oz thick) for 26 AWG is about 153 mils wide; for 30 AWG it is about 60 mils wide; for 38 AWG, it is about 9.5 mils wide.

Because loss is the dominant contributor to system degradation, designers should be aware that using smaller trace widths, laminates with higher loss tangent, and sub optimal routing solutions with higher pair-to-pair coupling and additional via stubs will decrease overall performance and the maximum allowable trace length. It is advisable, when designing systems that approach the maximum jitter limits, to perform detailed modeling, simulation, and measurement of the target design including the effects of material properties, traces, vias, and additional components.

DPAM/DPAF Series DP Array™ Final Inch® Test Fixture Validation When Used As a Complete System

Setup and Measurement

Input Stimulus Setup

A PRBS 2^7-1 pattern was used for victim stimulus and a repeating 1010… pattern used for the aggressor differential pairs on each side of the victim differential pair. Xilinx supplies a stimulus generator tool kit within their VirtexII Pro™ design kit giving customers complete control over the amount of jitter in the transmitter's data output. Using their stimulus system with their RocketIO™ multi-gigabit serial transceiver model, enough total jitter was added to the driver output to just meet worst case Serial ATA transmit jitter specifications. The slow-slow corner silicon model was used to come as close as possible to the minimum differential V_{DIFF} output specification.

The Test Circuit Model

The test circuit modeled is shown in Figure 11. It consists of the following:

- One set of three of Xilinx Virtex-II Pro™ Serial transceiver models configured as Serial ATA drivers.
- Xilinx FPGA flip-chip package model.
- 1 Samtec DP Array™ DPAM/DPAF Series Final Inch® design comprised of the DPAM-23-10-H-8-1/DPAF-23-01-H-8-1 mated connector model surrounded by the Samtec's BOR models, lossy trace models, and SMA connector models on both sides of the connector.
- One set of six AC coupling capacitors, value = 10 nF.
- 100 Ohm termination resistors.

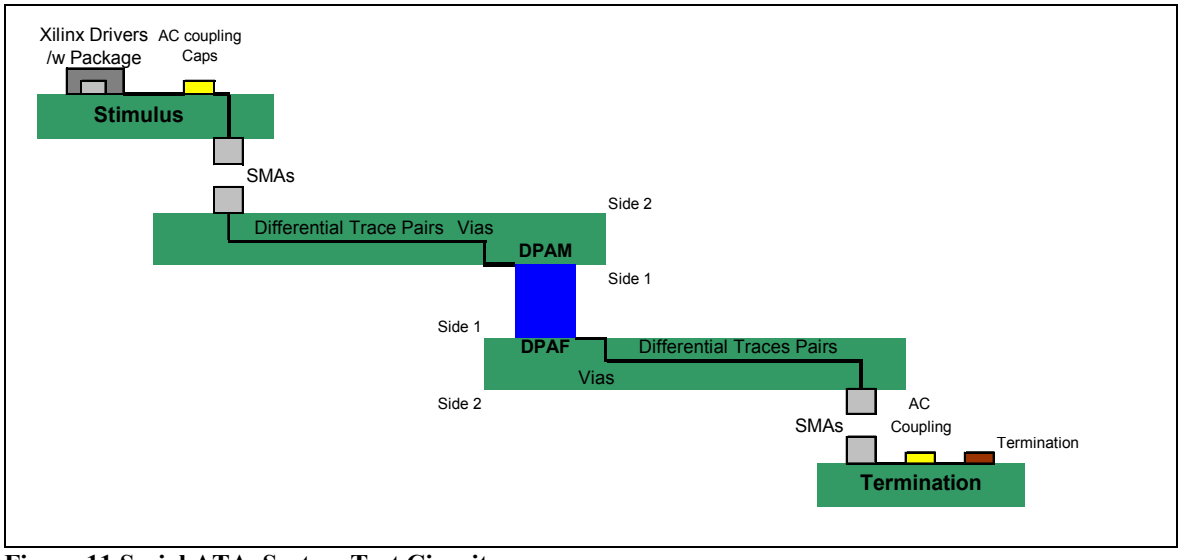


Figure 11 Serial ATA System Test Circuit

Procedure

Interconnect Budget

The interconnect budget can be best illustrated by the mask shown in Figure 12. In order to pass the Serial ATA constraints for loss and jitter, the simulated eye waveform must not touch any location within the grey areas shown. Calculated interconnect budget values are shown in Table 3.

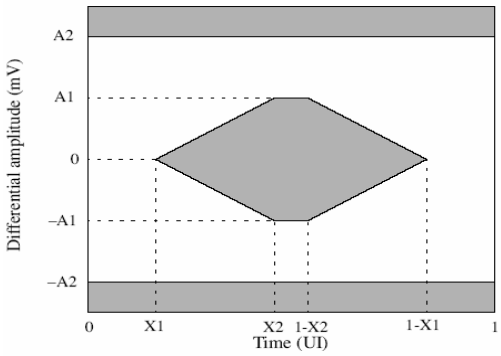


Figure 12 -Example mask template

Symbol	Near-end value	Far-end value	Units
X1	220.0	286.7	psec
X2[1]	0	0	psec
A1	200	162.5	mV Minimum
A2	300	300	mV Maximum

Table 2 - Serial ATA mask template intervals at 1.5 Gbps

[1]X2 is not specified in the Serial ATA specification. The time between X2 and 1-X2 is assumed to be 0 psec.

	Maximum Loss, A1 to –A1 (See example mask template) ($V_{DIFFp-p}$)	Minimum Eye Width, X1 to 1-X1 (See example mask template) (UI_{p-p})
Driver at Package Pin	0.400	0.65
Receiver at Package Pin	0.325	0.45
Interconnect budget:	1.8 dB loss[1]	0.2 UI_{p-p} (133.3ps when UI=666.7 ps)

Table 3 - Serial ATA interconnect budget max loss and min eye width calculated values

[1]The worst case operational loss budget at Nyquist frequency is calculated by taking the minimum input voltage to the receiver ($V_{RX-DIFF}$ = 325 mV) divided by the minimum driver output voltage ($V_{TX-DIFF}$ = 400 mV) 325/400 = .8125, which after conversion results in a maximum loss budget of 1.8 dB.

Transmitter Compliance Measurements

Setup for Tj for UI Measurements

As mentioned in the previous section, the driver stimulus' jitter was adjusted until the transmitter exhibited the maximum total jitter allowed by the Serial ATA specification at the driver package pins under the compliance load shown in Figure 13 below. The Serial ATA specification does not specify the range of capacitor values allowed for the AC coupling capacitors. We set C to 100nF for all simulations because it is a popular value in the industry. Table 4 shows the resulting output measurements.

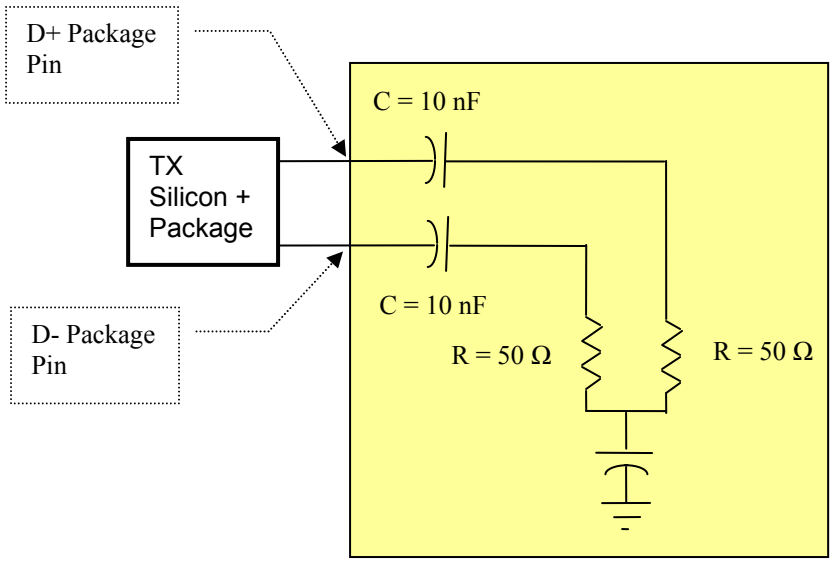


Figure 13 - Serial ATA Compliance Test/Measurement load

	V_{p-p}	Total Jitter
Specification	≥400 mV	≤ 220 ps
Measured	400.0 mV	220 ps

Table 4 - Serial ATA TX Silicon + Package Measurements at Package Pin

The eye pattern generated in the Serial ATA driver compliance test simulation can be found in Appendix A of this paper, picture #1.

Differential Voltage and Eye Width Measurements at Receiver End

The measurement results of the Serial ATA circuit simulations are shown in Table 5.

DPAM/DPAF Connector, 10 mm Stack Height	Max Jitter at UI = 666.7 psec	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Min Rx Differential Voltage, A1 to –A1[1] (See example mask template)	Pass/Fail
Specification	**≤ 286.6 psec**	**≥380 psec**	**≥325mVDIFFp-p**	-
2" total trace[2]	229.2	653.8	346.4	Pass
4" total trace	231.3	652.5	339.8	Pass
6" total trace	228.8	651.8	331.2	Pass
7" total trace	229.5	651.2	329.8	Pass
8" total trace	229.4	650.9	321.8	Fail

Table 5 - Serial ATA Measurements at Receiver End, 10mm stack height

[1]X2 to 1-X2, the mid bit sample time, is unspecified and assumed to be 0 ps.

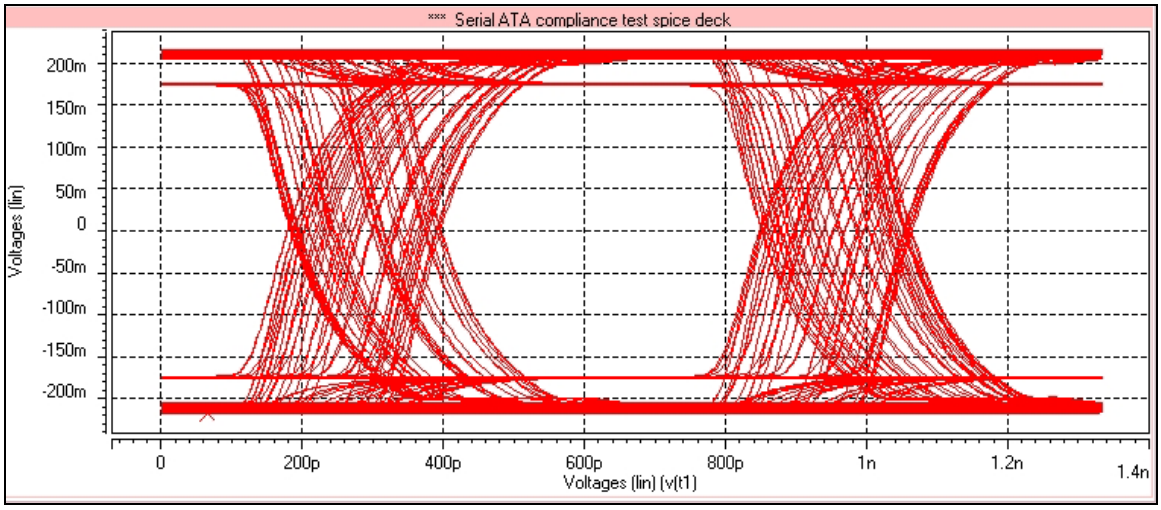
[2]The total trace length specified is the sum of the two differential trace lengths in the DPAM/DPAF Series test fixture model, as shown in Figure 11. These traces are always kept equal in length in each simulation.

The eye pattern generated in the Serial ATA circuit simulation with 7 inches total trace length can be found in Appendix A of this paper, picture #2. Superimposed on top of this eye waveform are the simulation results of the same circuit but without the DPAM/DPAF Series connector and breakout.

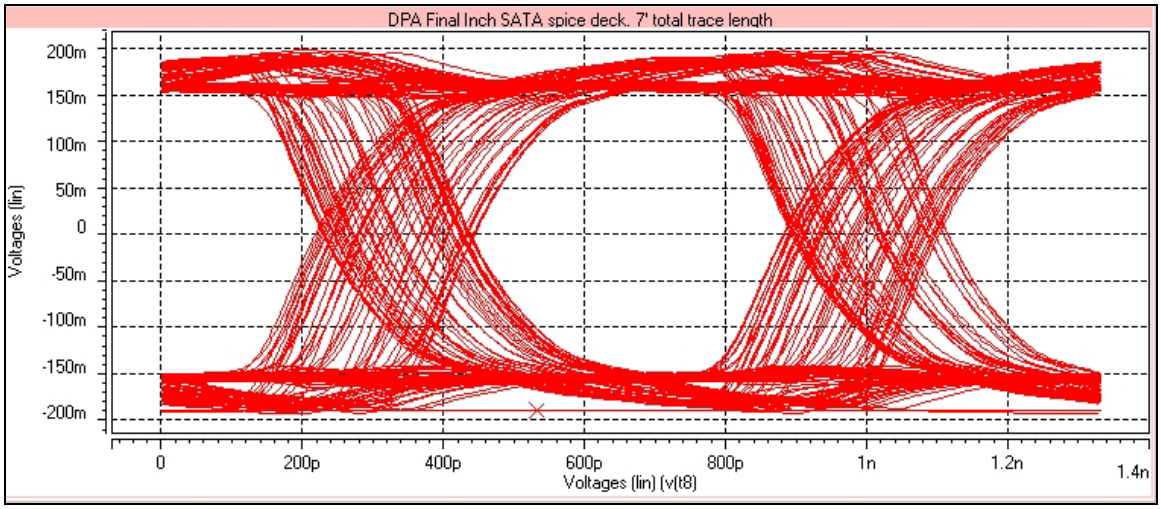
Conclusions

A single Samtec DP Array™ DPAM/DPAF Series 10mm stack height connector set in a board-to-board configuration can be used in Serial ATA systems with total trace lengths not to exceed 7 inches when used with Samtec's Final Inch® routing, breakout, and trace width solutions. Because loss is the dominant contributor to system degradation, designers should be aware that using smaller trace widths, laminates with higher loss tangent, and sub optimal routing solutions with higher pair-to-pair coupling and additional via stubs will decrease overall performance and the maximum allowable trace length. It is advisable, when designing systems that approach the maximum jitter limits, to perform detailed modeling, simulation, and measurement of the target design including the effects of material properties, traces, vias, and additional components.

Appendix A – Waveform images



Picture 1 – Worst case stimulus eye waveform, probed at Xilinx driver package pins and connected to compliance test/measurement load.



Picture 2 – Serial ATA circuit eye waveform, probed at terminator pins, 7 inches total trace length. Red = circuit with DPAM/DPAF connector, Blue = circuit without DPAM/DPAF connector