Application Note

DesignCon 2005

Correlation Report
QPairs® QTE-DP/QSE-DP and
DP Array™ DPAM/DPAF
Final Inch® SPICE Simulations vs.
Lab Measurements with the Xilinx™
RocketIO® Evaluation Board

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Developed in conjunction with
Teraspeed Consulting Group LLC

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Abstract

This paper will document correlation results of lab measurements and simulations of the Xilinx™ RocketIO® evaluation board used with the QPairs® QTE-DP/QSE-DP Final Inch® and DP Array™ DPAM/DPAF Final Inch® Test and Evaluation Board sets. Analysis will consist of first stimulating a typical trace-connector-trace circuit path and then observing the corresponding eye closure related to reflections caused by impedance discontinuities, loss, and stubs. Next, utility software will be used to extract, analyze, and format SPICE-measured voltage amplitudes and differential signal crossing times. These simulation results will then be compared with test measurements taken by Teraspeed.

Definitions

Loss – The differential voltage swing attenuation from transmitter to receiver on the trace. The trace is subject to resistive, dielectric, and skin effect loss. Loss increases as trace length and and/or signal frequency increases. Vias and connectors also exhibit losses which must be included in the interconnect budget.

Insertion Loss - The loss resulting from the insertion of a device in a transmission line, expressed as the reciprocal of the ratio of the signal power delivered to that part of the line following the device to the signal power delivered to that same part before insertion. Insertion loss is usually expressed in dB.

Jitter – The variation in the time between differential crossings from the ideal crossing time. Jitter includes both data dependent and random contributions on the interconnect.

PRBS – Pseudo Random Bit Sequence.

$\mathbf{V_{DIFF}}$ – Differential voltage, defined as the difference of the positive conductor voltage and the negative conductor voltage (V_{D+} - V_{D-}).

Introduction

High-speed serial data links are becoming more popular with engineers than parallel data busses because they are more power and space efficient. There are serial links used for chip-to-chip interfacing, backplane connectivity and system boards, and box-to-box communications. Although it is touted that switching to serial IO will simplify system design, some would argue that it comes with the added burden of more design time, for at a given data transfer rate, the frequencies present in serial links are much higher than those found in parallel busses, and so require both high-speed analog circuits and design techniques. Some of the more popular high speed serial links used today and their respective bit rates are:

Serial ATA	1.5 Gbps (Generation 1)
PCI Express	2.5 Gbps
XAUI	3.125 Gbps

Today's high speed serial links are based on recent advances in point-to-point interconnect technology. A link typically consists of a dual-simplex communications channel between two components, physically consisting of two low-voltage, differential signal pairs. One lane is used to convey self-clocking data and control at a nominal bit rate of 1.5 Gbps and up.

Samtec has developed a full line of high speed connector products that are designed to support these high serial bit rates. Working with Teraspeed Consulting, they have developed a complete breakout and routing solution for each member of their line of high speed connectors called Final Inch®. Design guidelines, test boards, and SPICE models for each test element (SMA, trace, breakout, and connector pair) have also been developed and are available for use by Samtec's customers. There are also many Application Notes available which demonstrate the use of Samtec high speed connectors in some of today's most popular serial data technologies; each showing their limits under stressed driver conditions. The stress simulations completed for these application notes all use the Xilinx™ RocketIO® SPICE kit components as part of the circuit.

As an addendum to the Application Notes just mentioned, this paper documents the comparison of real lab measurements of Final Inch® Test and Evaluation Board sets to SPICE simulations of the same using the Xilinx™ Vertex II Pro test platform and the Xilinx™ RocketIO® SPICE kit as the driver stimulus.

Lab Measurement Setup

Equipment

The components used for Final Inch® eye lab measurements are illustrated in Figure 1. The setup consists of the following components:

- Xilinx Virtex-II Pro™ ML321 Platform, Rev F used for stimulus; data rate set to 3.125 Gbps
- One of the following sets of Final Inch® Test and Evaluation Boards:
  - Samtec Q-Pairs® QTE-DP/QSE-DP Series in a 5mm stack: connector part numbers QTE-014-01-F-D-DP-A and QSE-014-01-F-D-DP-A.
  - Samtec DP Array™ DPAM/DPAF Series in a 10mm stack: connector part numbers DPAM-23-10-H-8-1 and DPAF-23-01-H-8-1.
- One set of 10:1 attenuators to protect the scope inputs.
- 50 Ohm termination resistors.
- Two sets of co-ax.
- Agilent Infinium 86100c oscilloscope with 86117A plug-in.

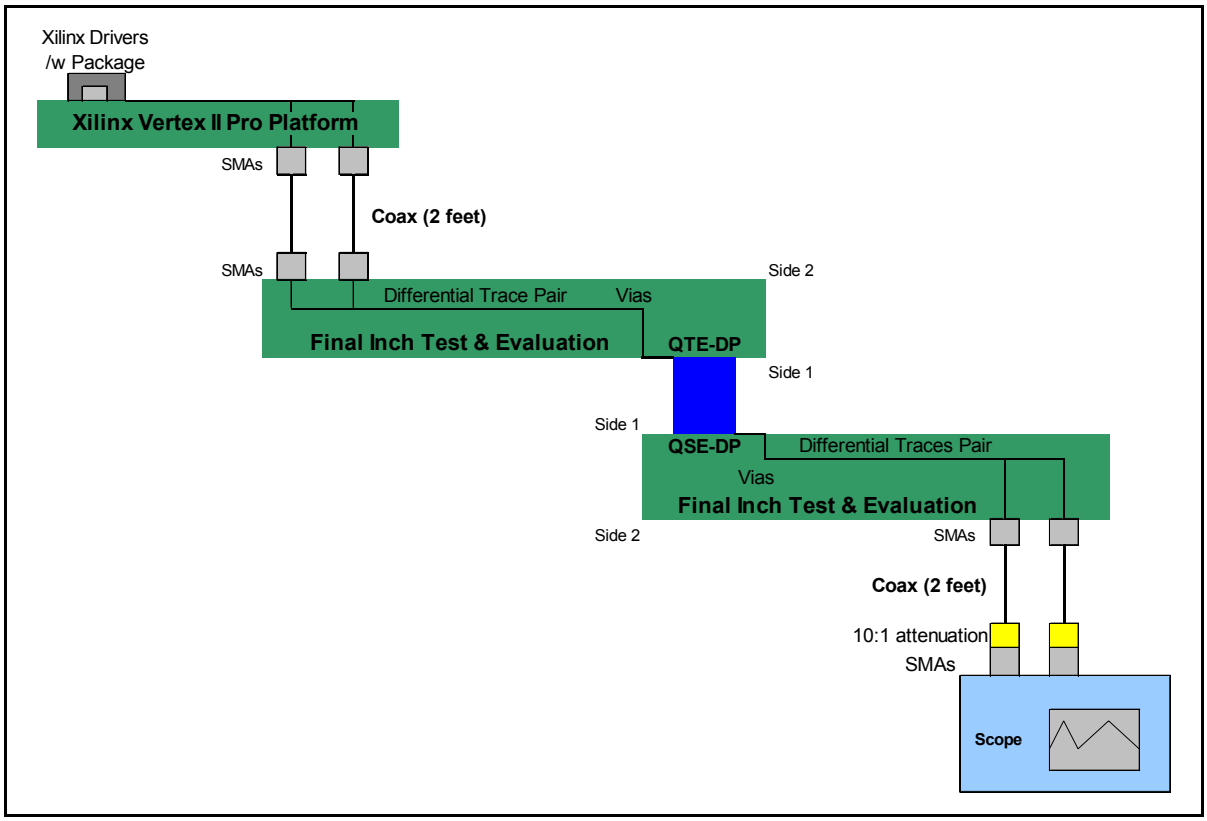

Figure 1 - Lab setup for Final Inch® measurements

Input Stimulus Setup

The Xilinx™ Virtex-II Pro platform is capable of producing a wide variety of bit stream patterns, most of them rather long. It was decided to run the PRBS 2^7-1 pattern, at a data rate of 3.125 Gbps, to keep the SPICE simulation completion times manageable. Unfortunately, the Xilinx test platform can only produce 1 bit pattern at a time, so testing with adjacent aggressors running a different bit pattern was not possible. Therefore, all of the results shown are of an uncoupled differential pair.

Simulation Measurement Setup

Test Circuit Spice Model

The test circuit model is shown in Figure 2. It consists of the following:

- One set of Xilinx™ Virtex-II Pro Serial transceiver spice models configured as differential drivers; data rate set to 3.125 Gbps
- Xilinx FPGA flip-chip package model.
- Lossy trace model (developed by Teraspeed) for Virtex-II Pro™ ML321 Platform
- Co-ax model (developed by Teraspeed).

- 1 Samtec Final Inch® SPICE design kit comprised of mated connector models for either QTE-DP/QSE-DP Series in a 5mm stack or DPAM/DPAF Series in a 10mm stack surrounded by their respective breakout models, lossy trace models, and SMA models on both sides of the connector.
- 50 Ohm termination to Ground.
- The measured traces were scaled by 1/10th to match scope results.

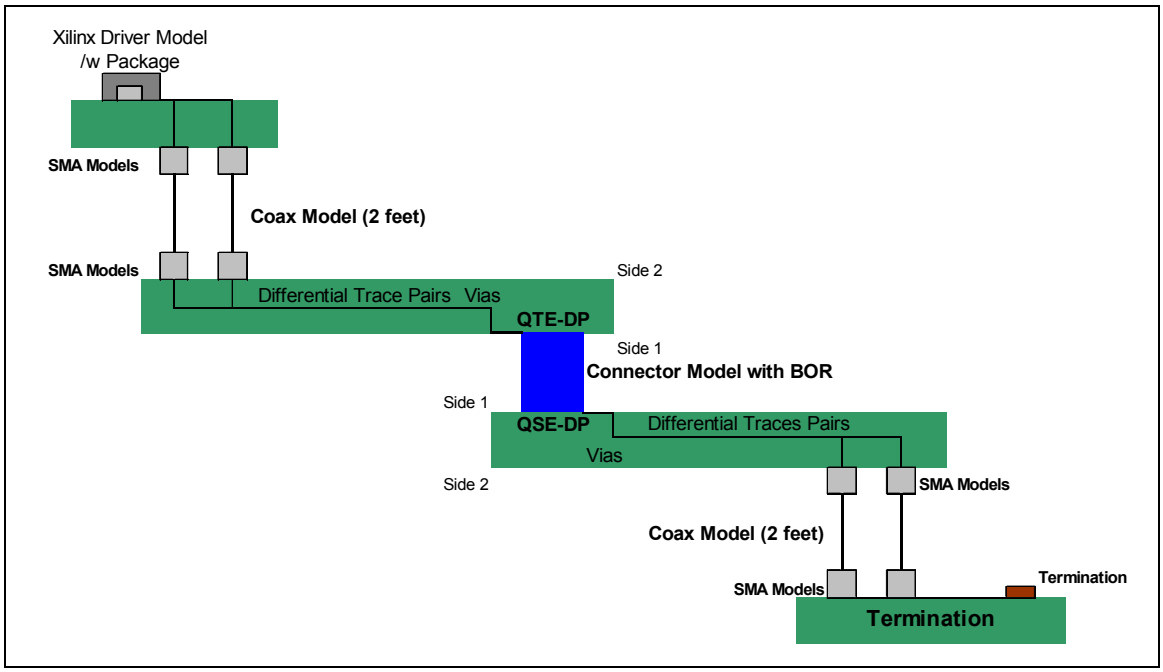

Figure 2 SPICE Circuit for Final Inch® correlation measurements

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SPICE Simulation Stimulus

Xilinx supplies a stimulus generator tool kit within their VirtexII Pro™ SPICE design kit giving customers complete control over the amount of jitter in the driver's data output. Using this stimulus system with their RocketIO™ multi-gigabit serial transceiver model, enough total jitter was added to the driver output to match the lab-measured driver jitter. The nominal silicon model was used in order to come as close as possible to the same differential V_{DIFF} output voltage and drive strength.

When we first compared the Virtex II platform's modeled outputs to our empirical measurements, we found that the model's edge rates were much faster (See Figure 3). This was caused by the bandwidth limiting components on the real platform that were not accounted for in the simulation. To remedy this, we added a filter circuit in the simulation to emulate these unmodeled board components. Figure 4 shows the dramatic improvement in the eye waveform.

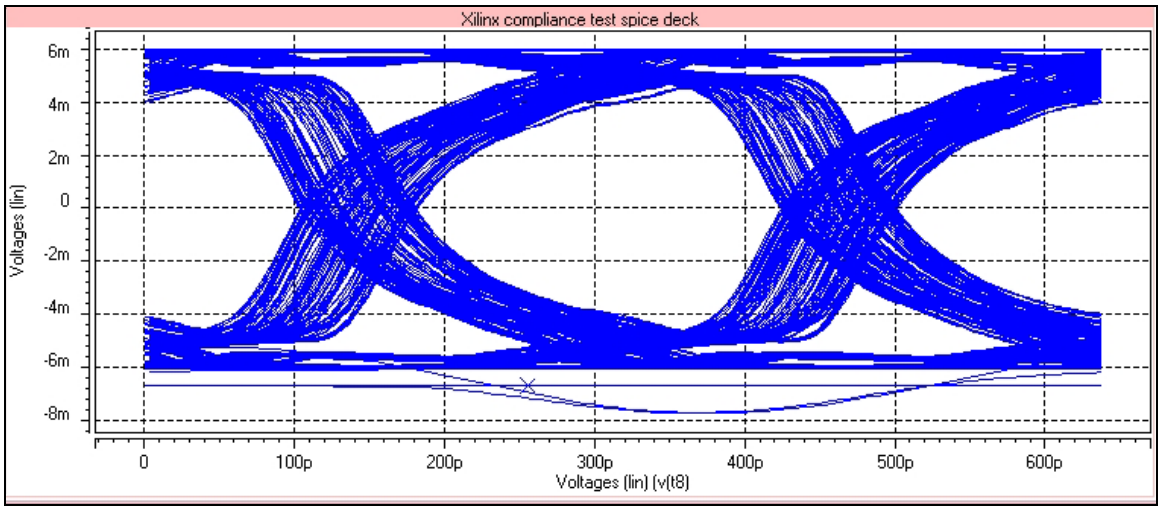

Figure 3 - Xilinx Vertex II platform model eye pattern before adding the low-pass filter (Data Rate = 3.125 Gbps)

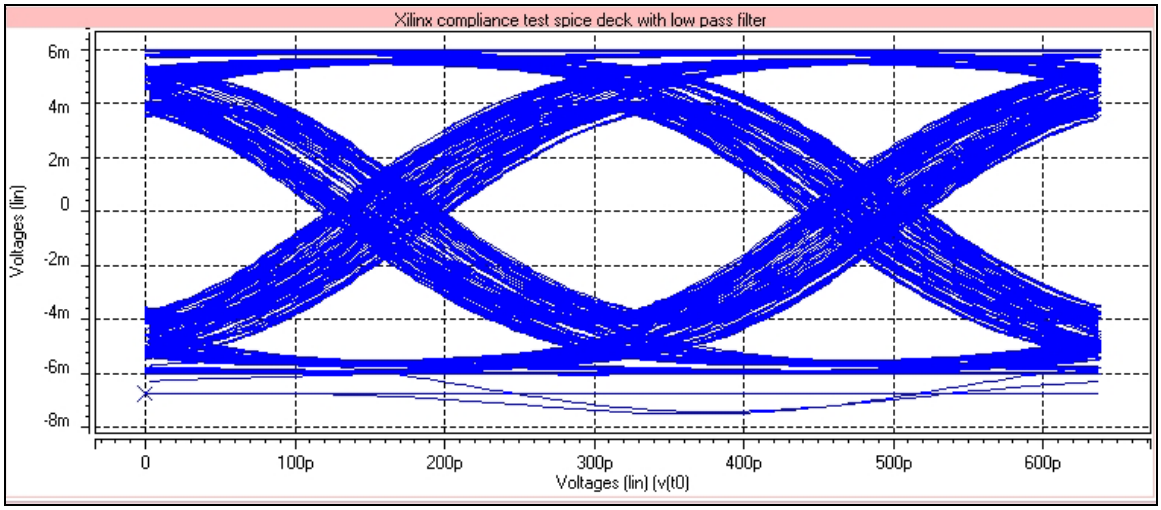

Figure 4 - Xilinx Vertex II platform model eye pattern after adding the low-pass filter (Data Rate = 3.125 Gbps)

Comparison of Xilinx Driver Stimulus

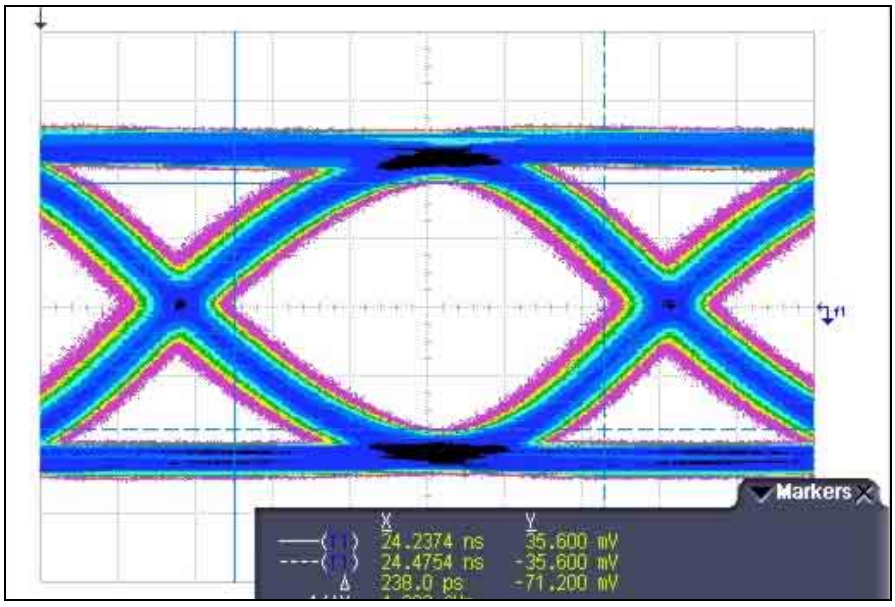

Figure 5 – Scope eye diagram of Vertex II test platform differential channel with 2 feet of co-ax (Data Rate = 3.125 Gbps)

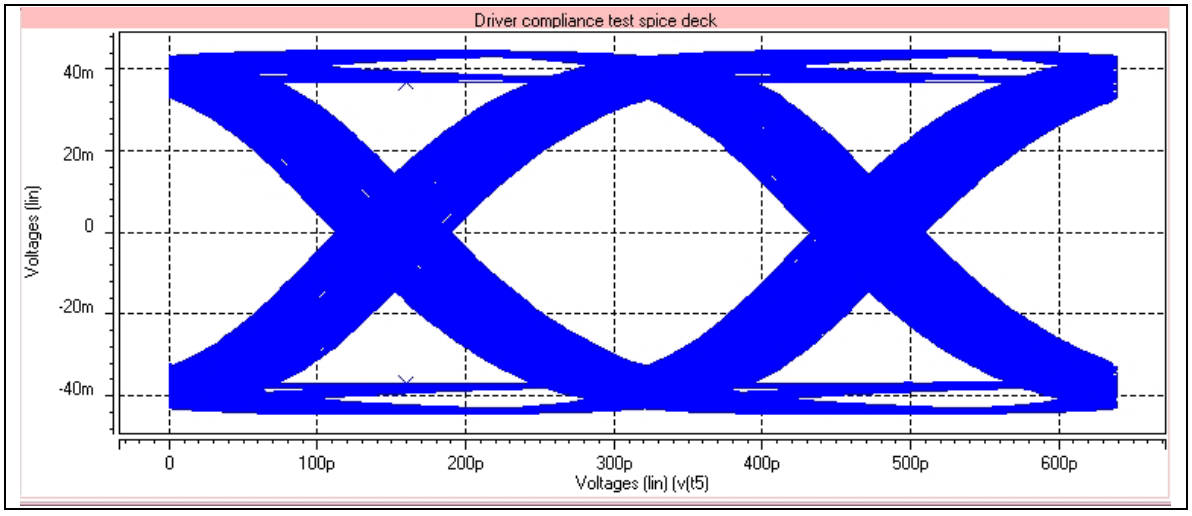

Figure 6 - SPICE eye diagram of Vertex II test platform differential channel with 2 feet of co-ax (Data Rate = 3.125 Gbps)

	V_{DIFF}	$Jitter_{P-P}$
Xilinx Board	694 mV	77.8 ps
Xilinx Spice	692 mV	81.0 ps

Table 1 – Xilinx Driver Correlation, Test board vs. SPICE simulation

QTE-DP/QSE-DP 5mm Board-Board Test Results

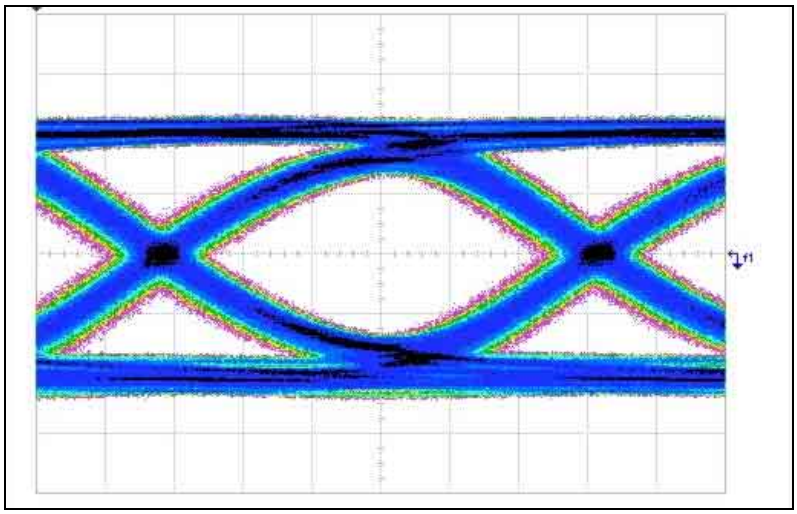

Figure 7 - Scope eye diagram of test stimulus through the QPairs® QTE-DP/QSE-DP Final Inch® Test and Evaluation Board Set (Data Rate = 3.125 Gbps)

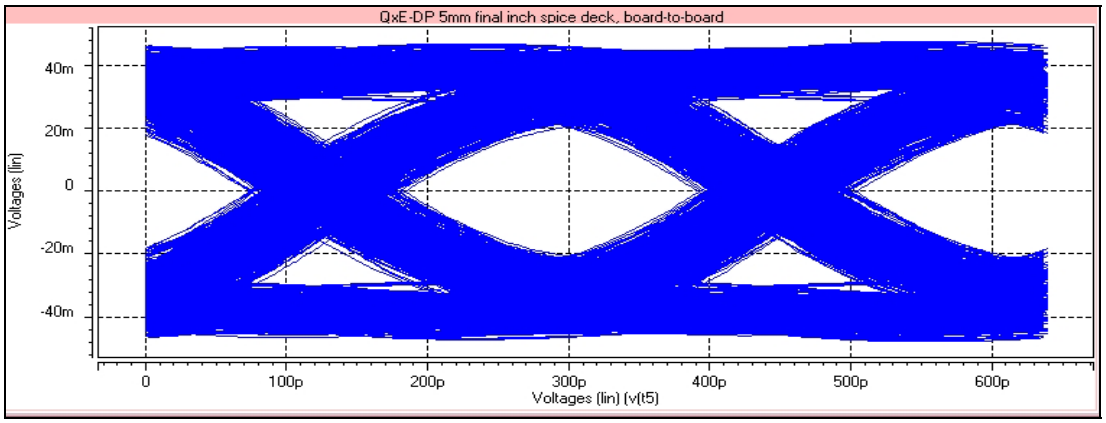

Figure 8 - SPICE eye diagram of test stimulus through the QPairs® QTE-DP/QSE-DP Final Inch® Test and Evaluation Board SPICE model (Data Rate = 3.125 Gbps)

QTE/QSE-DP 5mm Board-Board	**Min Eye Height (mV_{DIFF})**	**Max Eye Jitter ($psec_{P-P}$)**
Lab results	407	107
Spice results	391	109

Table 2 – Comparison, QTE-DP/QSE-DP board lab vs. SPICE simulation

Conclusion

There is strong correlation between measured and simulated results of the QPairs® QTE-DP/QSE-DP Final Inch® boards using the same SPICE models that were used in the Application Notes.

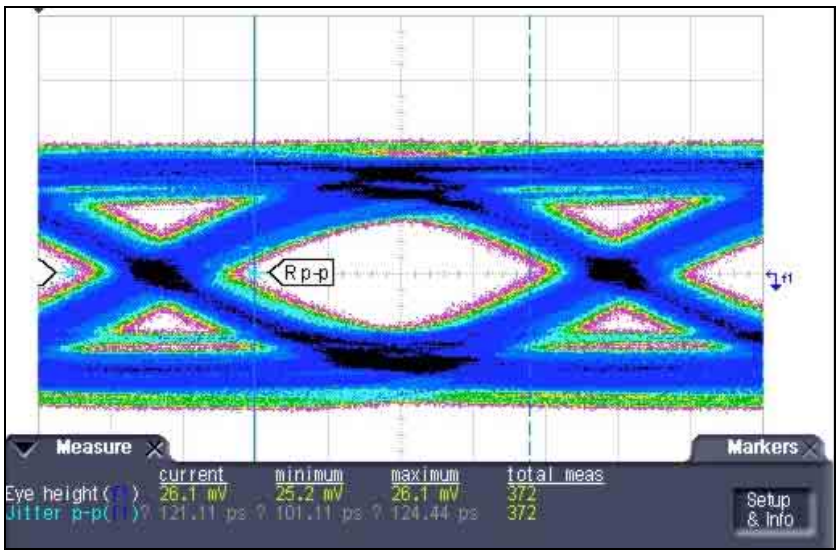

Figure 9 - Scope eye diagram of test stimulus through the QPairs® QTE-DP/QSE-DP Final Inch® Test and Evaluation Board Set with 10 inch HFEM-DP Flex Assembly (Data Rate = 3.125 Gbps)

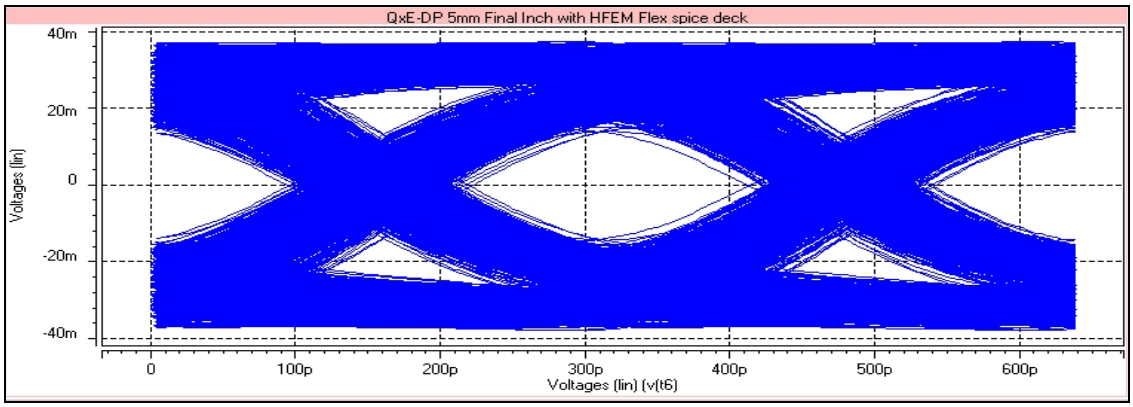

Figure 10 - SPICE eye diagram of test stimulus through the QPairs® QTE-DP/QSE-DP Final Inch® Test and Evaluation Board with 10 inch HFEM-DP Flex Assembly (Data Rate = 3.125 Gbps)

QTE/QSE-DP Board -10" Flex -Board	**Min Eye Height (mV_{DIFF})**	**Max Eye Jitter ($psec_{P-P}$)**
Lab results	252	124
Spice results	276	126

Table 3 - Comparison, QTE-DP/QSE-DP board with Flex, lab vs. SPICE simulation

Conclusion

There is still strong correlation between measured and simulated results after adding 10 inches of Flex between the two QTE-DP/QSE-DP Final Inch® boards.

DP Array™ 10 mm Board-Board Test Results

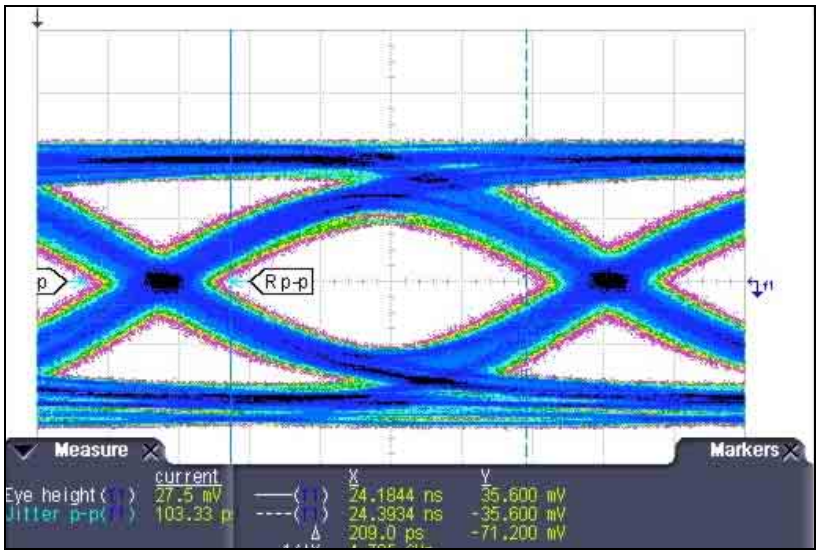

Figure 11 - Scope eye diagram of test stimulus through the DP Array™ 10 mm Final Inch® Test and Evaluation Board Set (Data Rate = 3.125 Gbps)

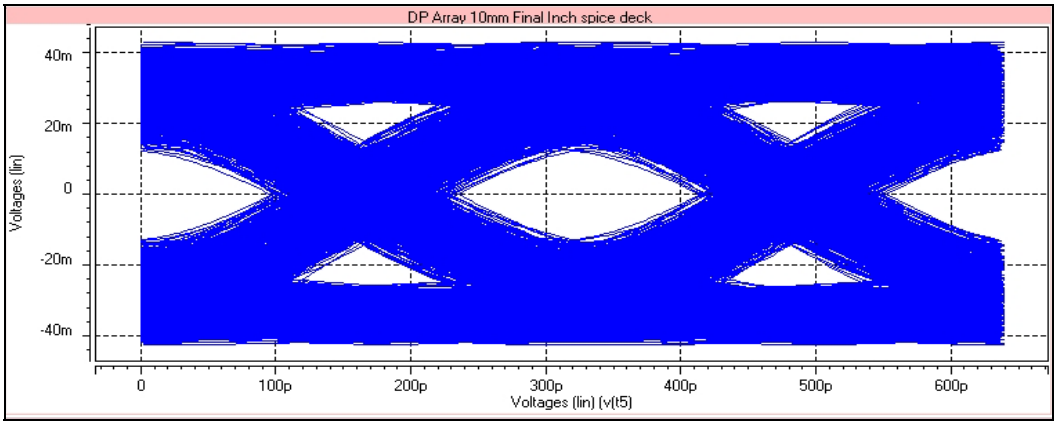

Figure 12 - SPICE eye diagram of test stimulus through the DP Array™ 10 mm Final Inch® Test and Evaluation Board SPICE model (Data Rate = 3.125 Gbps)

DP Array 10mm Final Inch® Board - Board	**Min Eye Height (mV_{DIFF})**	**Max Eye Jitter ($psec_{P-P}$)**
Lab results	272	103
Spice results	251	138

Table 4 – Correlation, DP Array™ 10 mm Final Inch® lab vs. SPICE simulation

Conclusion

DP Array™ SPICE models are conservative with respect to real measurements.

Final Conclusions

The overall results show that SPICE models developed by Samtec and Teraspeed show good correlation to real measured data.

Samtec has an extensive collection of Application Notes based on some of today's most popular serial transmission technologies. All SPICE simulations utilize the exact same SPICE models used to complete this paper. Following is a list of Application Notes available at the time of publication, and a complete, up-to-date list can be found on our website on our Application Notes page.

QPairs® QTH-DP/QSH-DP Series - 5mm stack

- PCI Express
- Serial ATA
- XAUI

QPairs® QTE-DP/QSE-DP Series - 5mm stack

- PCI Express
- Serial ATA
- XAUI

QPairs® QTE-DP/QSE-DP Series - 16mm stack

- PCI Express

Q2™ QMS-DP/QFS-DP Series - 11mm stack

- PCI Express
- Serial ATA
- XAUI

SamArray® YFW/YFS Series - 10mm stack

- Rapid IO

SE Array™ SEAM/SEAF Series - 7mm stack

- Rapid IO

DP Array™ DPAM/DPAF Series - 10mm stack

- RapidIO
- PCI Express
- Serial ATA
- XAUI