DDR4 Design And Verification In Hyperlynx LINESIM/Boardsim

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Outline

- **Objective/Goal**
- DDR4 vs. DDR3 from the SI/PI Perspective
- Stackup Design Consideration & SSO Effects
- Design Considerations:
  - Impedance, ODT and Manufacturing Variations
  - Length Matching Requirements
  - Crosstalk Effects &Timing
- Analysis Tools Comparison
- Summary

Objective/Goal

- Design & verify DDR4 interface across all operational conditions and possible manufacturing variations that meets both vendor requirements (driver and receiver) and the JEDEC standard.

- The ultimate goal in designing a DDR4 interface is that the signals meet their required eye masks and timing while crosstalk and Simultaneous Switching Output (SSO) effects are taken into consideration.

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DDR4 vs. DDR3 from the Si/PI Perspective

Features/Options	DDR3	DDR4	Comments
Voltage (core, /IO)	1.5V	1.2V	Reduces memory power demand
Vref Inputs	2 – DQs & CMD/ADDR	1 –CMD/ADDR	VREFDQ now internal
Data Rate - Mb/s	800, 1066, 1333 1600, 1866, 2133	1600, 1866, 2133 2400, 2666, 3200	Migration to higher-speed I/O
tCK – DLL enabled	300MHz to 800MHz	667MHz to 1.6GHz (625MHz minimum)	Higher data rates
DQ Driver (ALT)	40Ω	48Ω	Optimized for Point-to-Point (PtP)
DQ Bus	SSTL15	POD12	Mitigate I/O noise and power
Rtt Values	120, 60, 40, 30, 20Ω	240, 120, 80, 60, 48, 40, 34Ω	Support higher data rates
ODT Control	ODT signaling required	ODT signaling not required	Ease of ODT control, allows non- ODT routing on PtP applications
VREFDQ Calibration	none	supported	Optimize internal VREFDQ
Data Bus Inversion (DBI)	none	supported	Mitigate I/O noise and power
Data Bus Write CRC	none	supported	Error detection of data traffic
C/A Parity	none	supported	Error detection of CMD/ADDR bus

Courtesy of Micron

DDR4 vs. DDR3 from the SI/PI Perspective

- DDR4 Pins added
  - VDDQ (2)
  - VPP
  - Bank Group (2)
  - DBI_n
  - ACT_n
  - PAR
  - Alert_n
  - TEN
- DDR3 Pins eliminated
  - VREFDQ
  - Bank Address (1 of 3)
  - VDD (1), VSS (3), VSSQ (1)

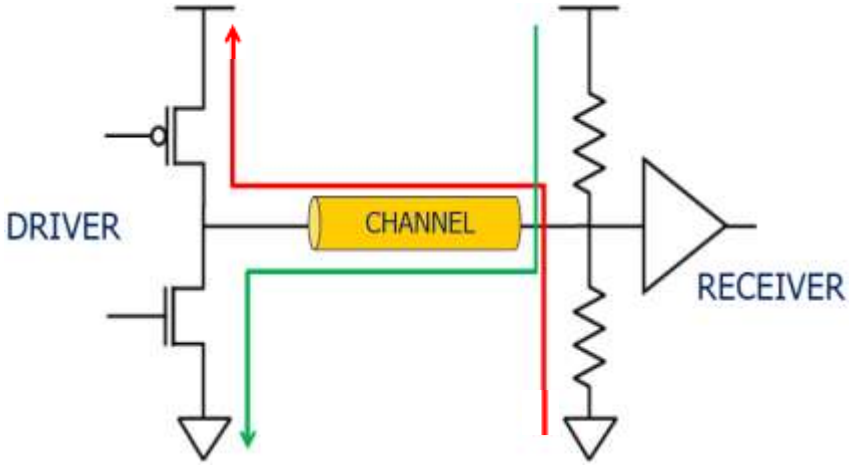
	x8	
	DDR3	DDR4
VSS	12	9
VDD	9	8
VPP	0	1
VSSQ	5	4
VDDQ	4	6
VREFCA	1	1
VREFDQ	1	0
Bank Group	0	2
Bank Address	3	2
Address	16	16
DQ	8	8
DQS/DQS#	2	2
CK/CK#	2	2
CKE	1	1
CS	1	1
ODT	1	1
ACT	0	1
RAS	1	1
CAS	1	1
WE	1	1
DM/TDQS/DBI	2	2
ZQ	1	1
Reset	1	1
TEN	0	1
PAR	0	1
Alert	0	1
Total	73	75
New for DDR4		

Micron

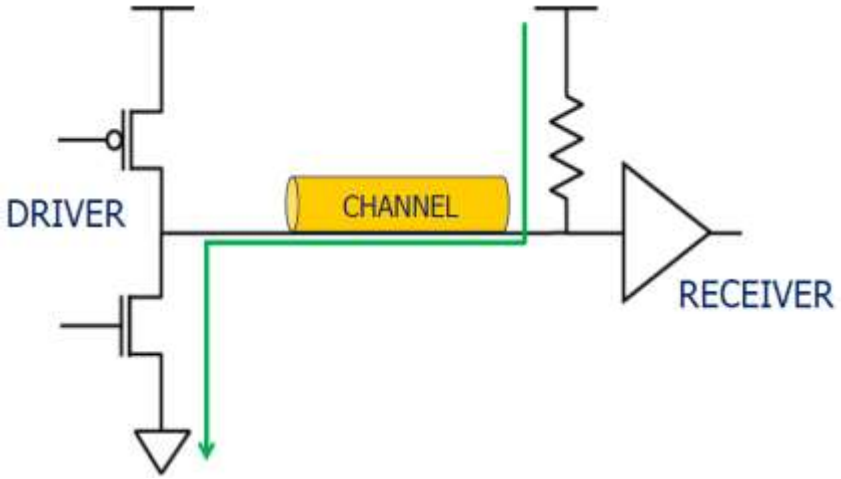
DDR4 vs. DDR3 from the SI/PI Perspective

- output Driver and Termination

DDR3 – Push-Pull
(HSTL)



DDR4 – Pseudo Open Drain
(POD)



- POD drivers have a strong pull-down strength but a weaker pullup strength.
- Reduced overall power demand compared to using strong pullup
- Proven GDDR scheme

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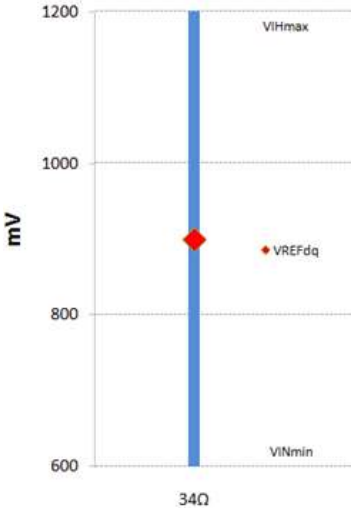
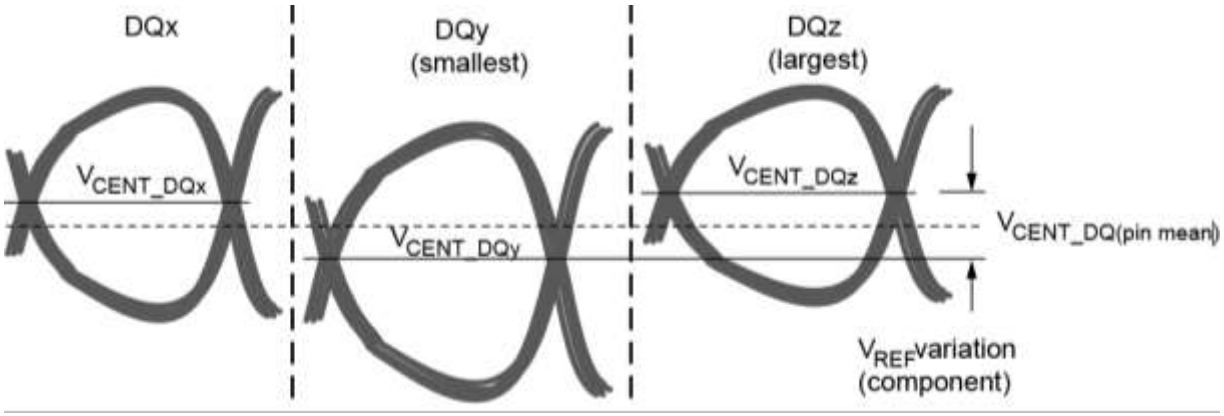
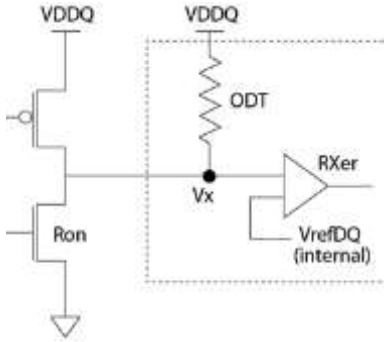
DDR4 vs. DDR3 from the SI/PI Perspective

- VREFDQ Calibration – VCENT_DQ(mean)
- VREFDQ is determined by the controller's calibration process using training
  - Calibrating VREFDQ determines optimum VREFDQ setting for each DQ - VCENT_DQ(mean)
    - The level halfway between the lowest DQ setting and the highest DQ setting







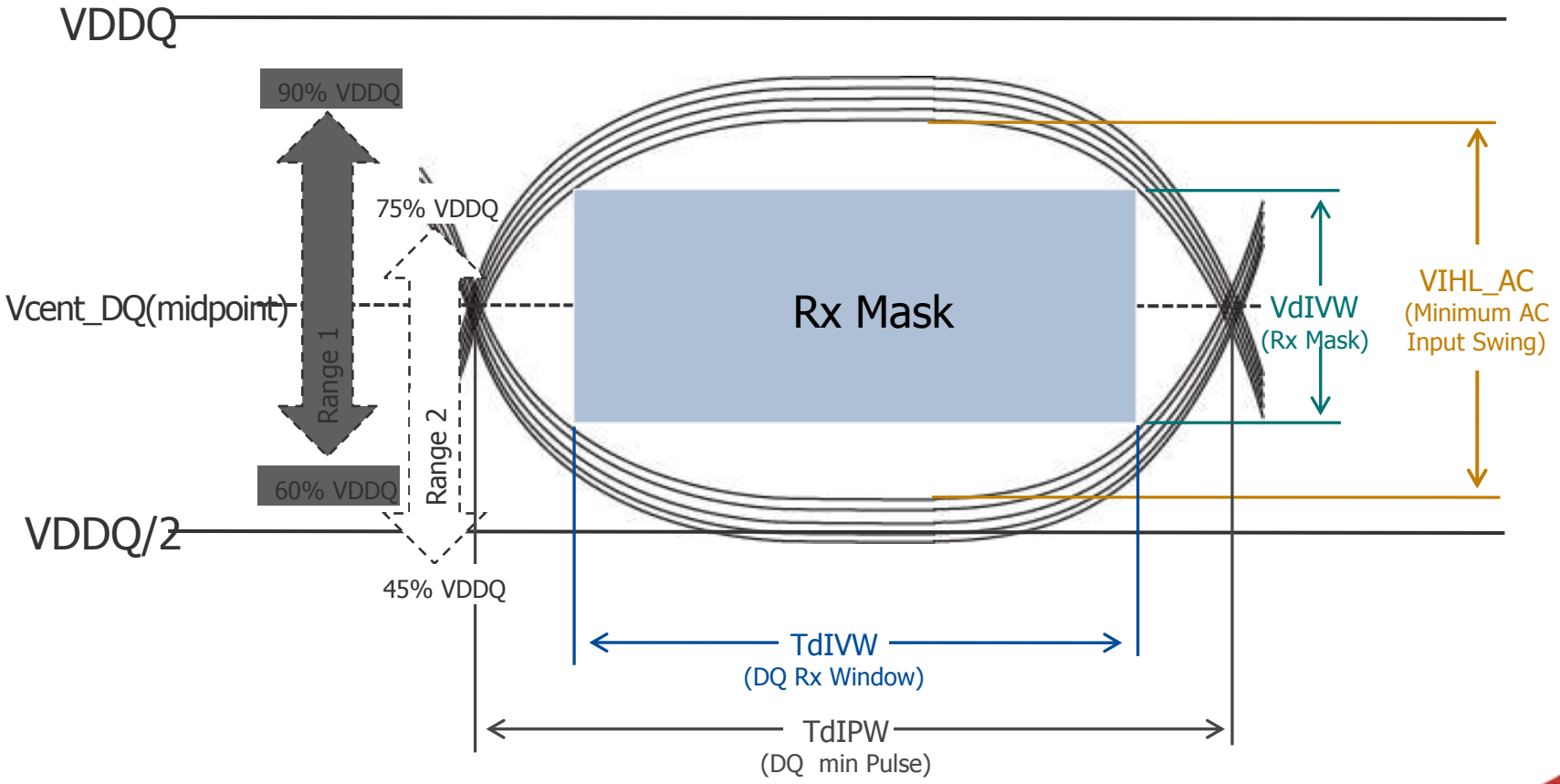
- Hyperlynx DDR4 timing wizard supports analysis for various VREFDQ

DDR4 vs. DDR3 from the SI/PI Perspective

- DDR4 Rx Mask and Data-Eye
- The Data bus timing has changed from the classical setup/hold relationship to DDR4's data-eye mask
  - The controller must satisfy the data receiver mask requirements
  - Data timing specifications are applicable when referenced to calibrated VREFDQ: Vcent_DQ(midpoint)
  - The calibrated Rx mask takes the place of classical set-up and hold
- Each DRAM is individually calibrated by the controller to meet the Rx Mask requirements

DDR4 vs. DDR3 from the Si/PI Perspective

- DDR4 Receiver Data Mask vs Data-Eye



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Stackup Design Considerations

- Power & Ground Planes Placement
- Minimize inductive path
- Data Lines Signal Group Placements
- Need to place adjacent to ground plane
- Address, Command & Control Signals Placement
- When possible place adjacent to good reference plane (i.e. ground or power)

Layer #	Recommended Layer Assignment	
1	Signal 1	
2	GND_1	
3	Signal 2	Address CMD & CNTL
4	PWR_1	VDD =1.2V for Memory Interface
5	Signal 3	Address CMD, CNTL & CLK
6	GND_3	
7	Signal 4	DQ & DQS
8	GND_4	
9	Signal 5	DQ & DQS
10	GND_4	
11	Signal 6	Discrete signals
12	Signal 7	Discrete signals
13	GND_5	
14	Signal 8	DQ & DQS
15	GND_6	
16	Signal 9	DQ & DQS
17	GND_7	
18	Signal 10	Address CMD, CNTL & CLK
19	PWR_2	VDD =1.2V for Memory Interface
20	Signal 11	Address CMD & CNTL
21	GND_8	
22	Signal 12	

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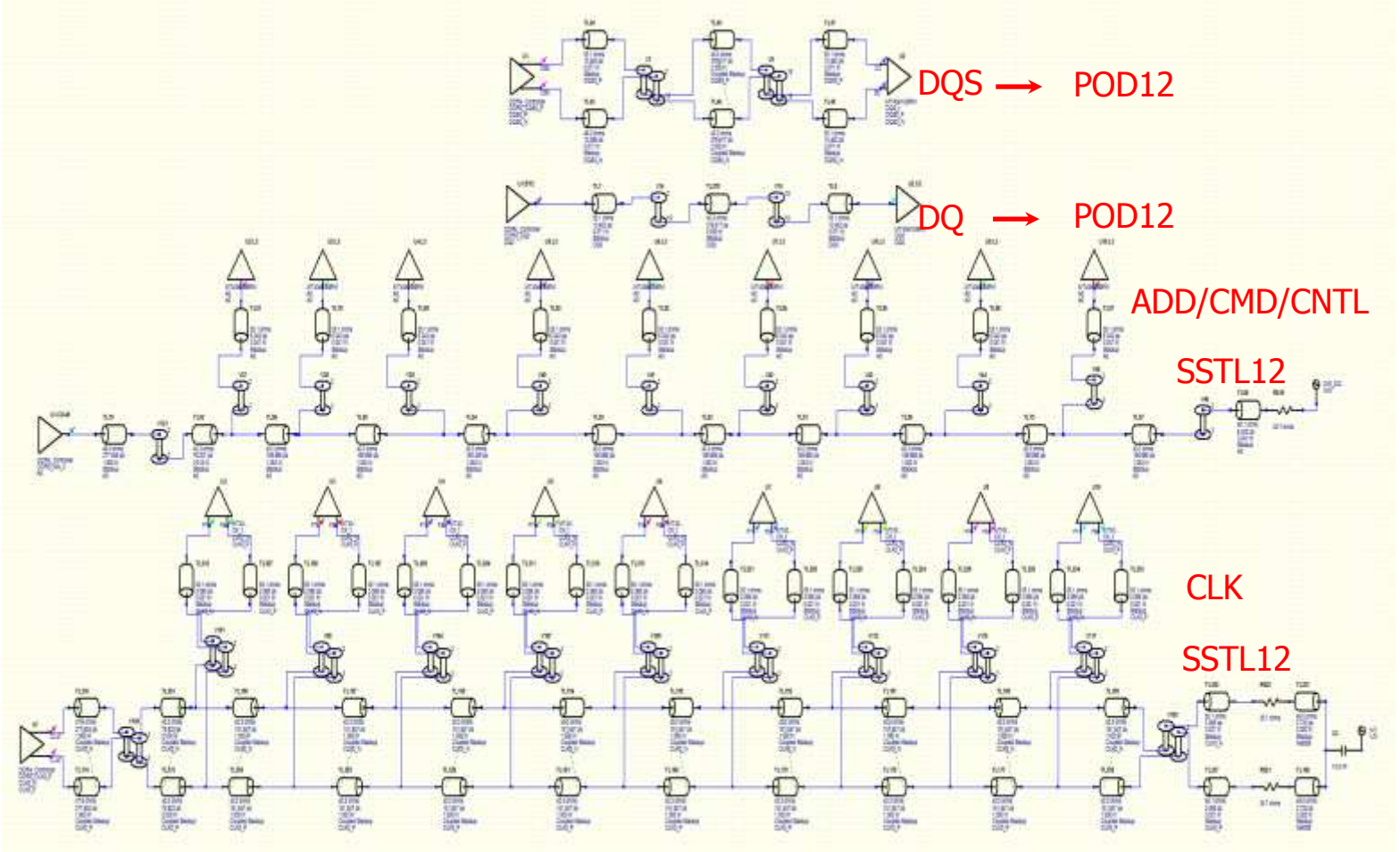
DDR4 Signal Groups & operating Frequency

	Signal Groups	Nets	DDR4 @ 2133 MT/s
1	Clocks Group	CLK_N CLK_P	1066.5 MHz
2	Data Group	DQS_N/P[7:0] DQ[72:0] DM[7:0]/DBI[7:0]/TDQS[7:0]	1066.5 MHz
3	CTL Group with 1T Timing	CS[1:0] CKE[1:0] ODT[1:0]	533.25 MHz
4	ADD/CMD Group with 1T Timing	A[16:0] BA[1:0] BG[1:0] ACT_N PAR_N	533.25 MHz
4	ADD/CMD Group with 2T Timing	A[16:0] BA[1:0] BG[1:0] ACT_N PAR_N	266.625 MHz

Design Considerations

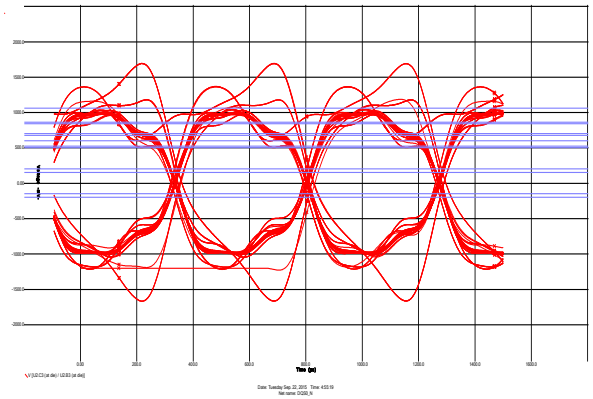
Impedance, ODT, & manufacturing variations

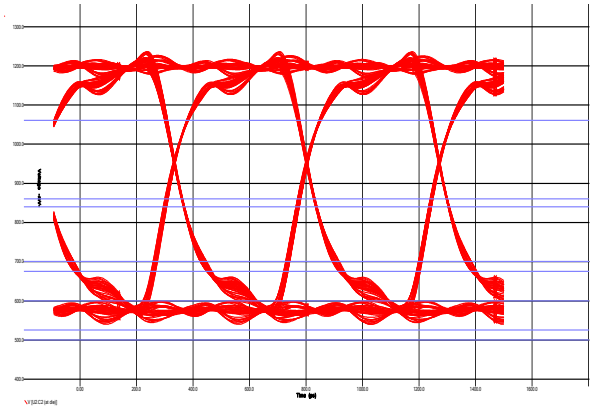


Design Considerations

Impedance, ODT, & manufacturing variations

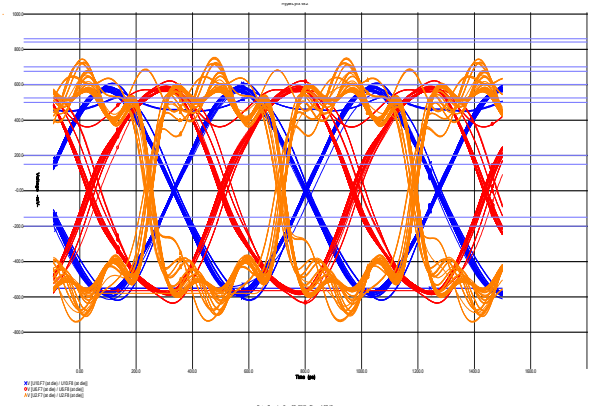
DQS

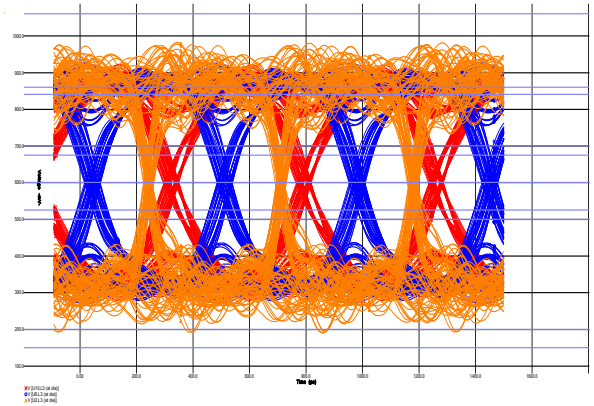




DQ

CLK @ 1ST, 5TH, & 9TH CHIP





ADD/CMD/CNTL @ 1ST, 5TH, & 9TH CHIP

Optimized Data/Strobe/ADD/CNTL and Clock signals quality after all permutations.

High confidence in signal quality was achieved prior to moving forward.

Typical DDR4 Signal Groups Length Matching Guidelines

	Groups	Group Matching Description	Length Matching (mils)
1	Clock Group: CLK_N & CLK_P	 CLK_N to CLK_P	 ± 10
2	Data Groups: DQ[72:0]/DM[7:0]/DBI[7:0]/T DQS[7:0] & DQS[7:0]	DQ to DQ within byte lane DQ to DQS_N/P DQS_N to DQS_P	± 50 ± 50 ± 10
3	CTL Group: CS[1:0] CKE[1:0] ODT[1:0]	Maximum trace segment routing to each memory chip CTL to CTL CTL signals to CLK_N/P to each memory chip	NA* ± 20 ± 20
4	ADD/CMD Group: A[16:0] BA[1:0] BG[1:0] ACT_N PAR_N	 Maximum trace segment routing to each memory chip Maintain equal length between trace segment to each memory chip within Add/CMD to Add/CMD Add/CMD signals to CLK_N/P to each memory chip	 NA* ± 20 ± 20 ± 20

- All a Data lines within a byte lane must be length matched to their associated strobes within that byte lane
- To be determined through eye diagram analysis and validated through timing analysis
- *To be determined by topology

Typical DDR4 Signal Groups Crosstalk Routing Guidelines

	Signal Groups	Coupling Description	Coupling Distances (in terms of line width)
1	Clocks Group	CLK from other signals	2W
2	Data Group	DQ to DQ within same byte lane DQ to DQS within same byte lane DQ to other byte lanes DQS to other signal groups	1.5W 1.5W 1.5W 4W-5W
3	CTL Group with 1T Timing	CTL to CTL CTL to other signal groups	2.5W 4W-5W
4	ADD/CMD Group with 1T Timing	ADD/CMD to ADD/CMD ADD/CMD to other signal groups	2.5W 4W-5W

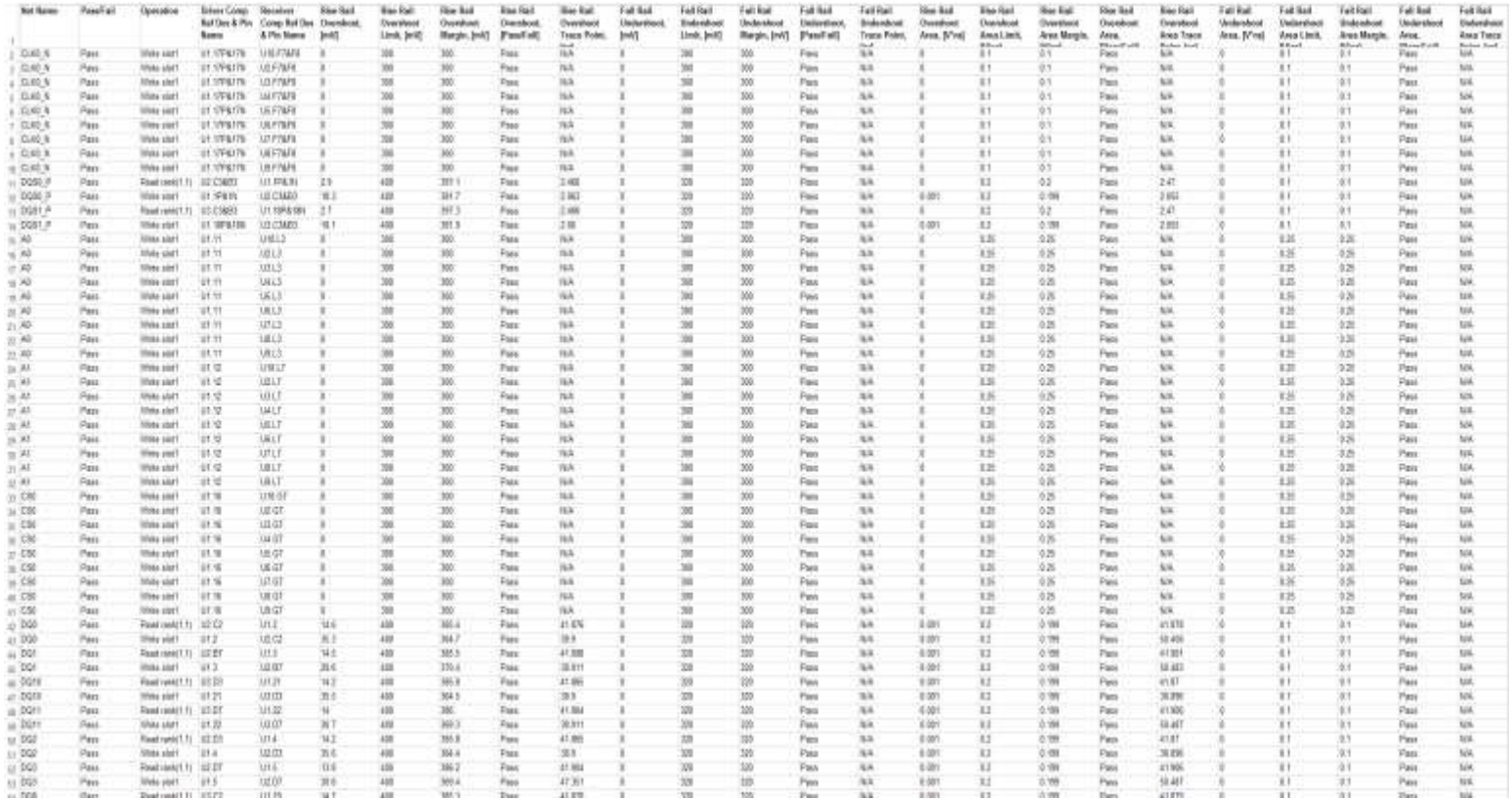
- Designed for a 40 ohm system with minimum trace width of 5 mils for the ADD group and 7.9 mils for the DQ group
- To be determined through eye diagram analysis and validated through **timing analysis**

Don’t route the entire DDR4 bus then simulate

Hyperlynx DDR4 Sample Signal Groups Timing Reports

Per The length matching guidelines & crosstalk rules

Typical-Corner Case JEDEC Timing Spreadsheet from simulations

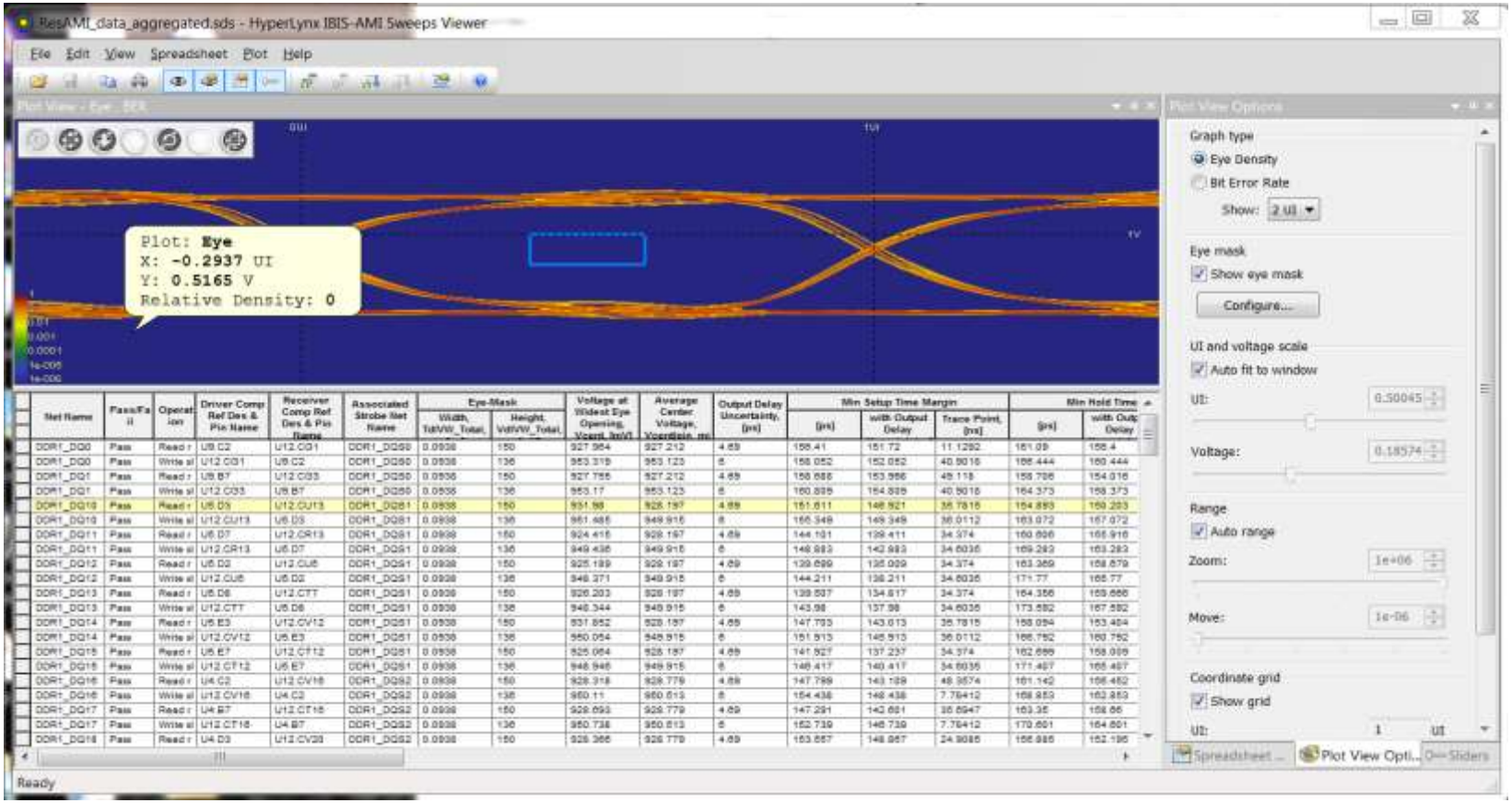


DQ to DQ within same byte lane = 1.5W
DQ to DQS within same byte lane = 1.5W
DQ to other byte lanes = 1.5W
DQS to other signal groups = 4W-5W

ADD/CMD to ADD/CMD = 2.5W
CTL to CTL = 2.5W
ADD/CMD/CTL to other signal groups = 4W -5W
CLK from other signals = 2W

Hyperlynx DDR4 Sample Signal Groups Timing Reports
for Data Byte Lanes

Received Data Signals Timing Spreadsheet and Eye Mask listed per Bit



The timing wizard allows you to assess your signal quality across many possible variation (i.e. design and manufacturing variations) with multiple timing reports

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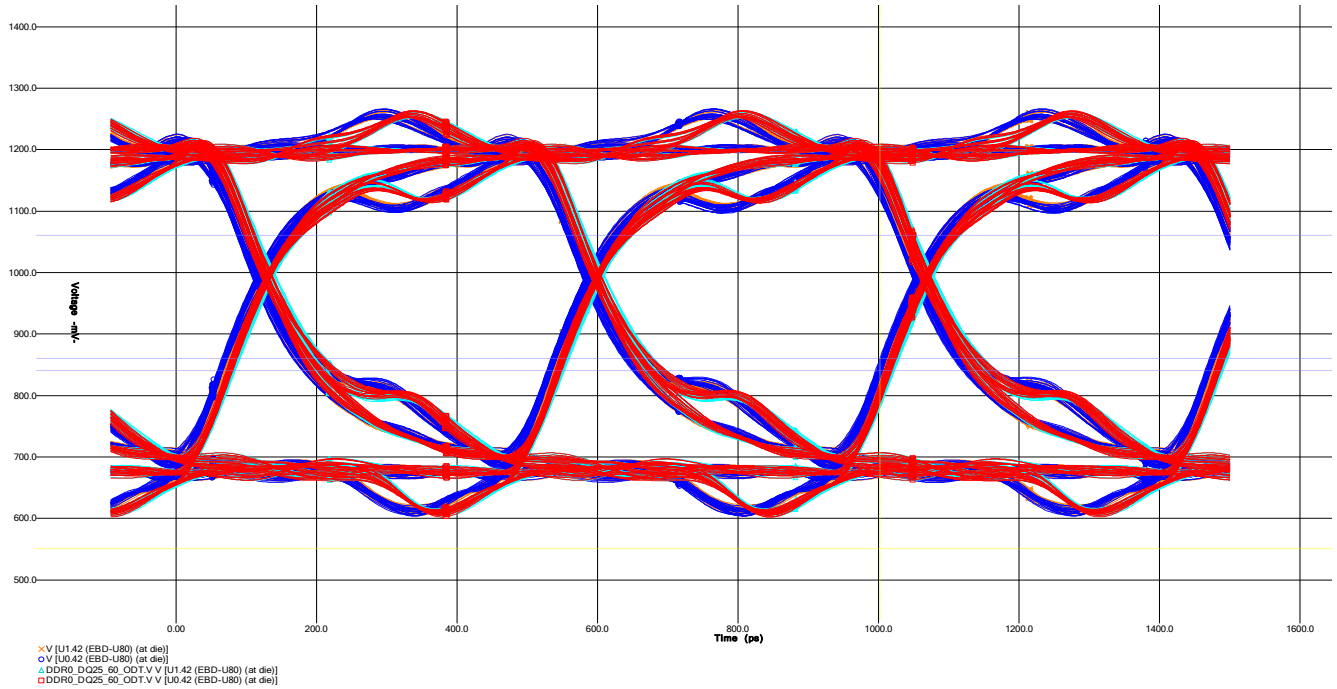
Analysis Tools Comparison (Data Signal)

Hyperlynx Boardsim results vs 2½ D field solver s-parameter extracted results overlaid



1021 ports

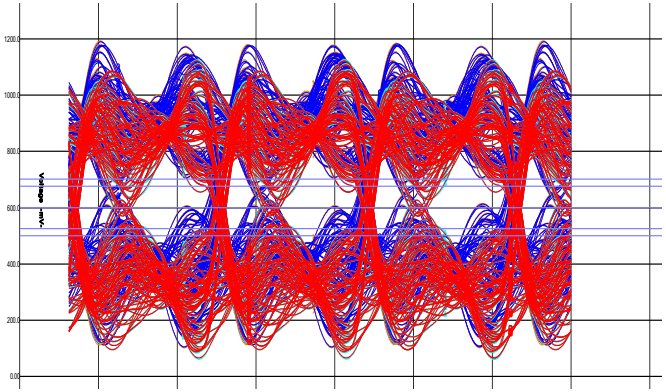
Royal Blue & **Orange** Waveforms = 2 ½-D Field Solver Results
Red & **Light Blue** Waveforms = Hyperlynx Boardsim Results

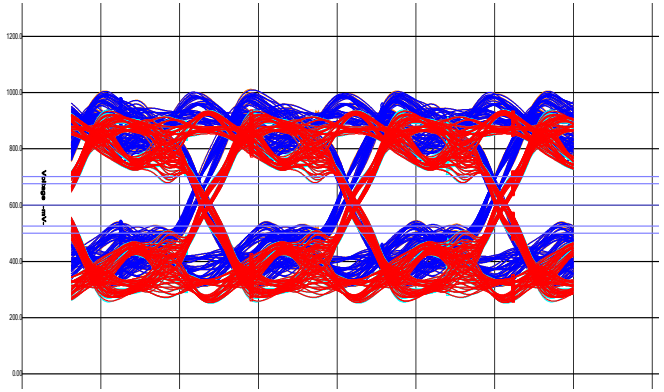
High confidence can be extrapolated from the Hyperlynx Boardsim simulations when the signals are ground referenced.

Analysis Tools Comparison (ADD Signal)

Hyperlynx Boardsim results vs 2½ D field solver s-parameter extracted results overlaid

1ST Chip

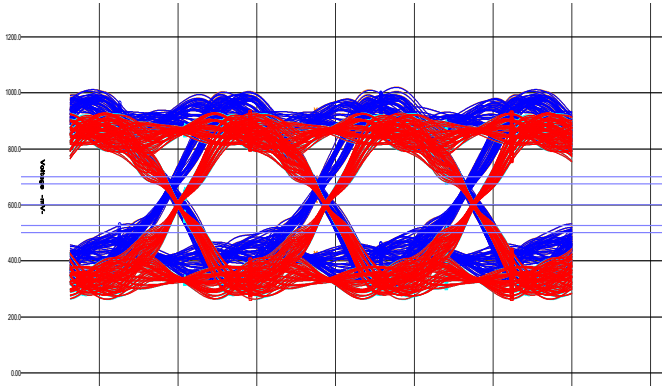




5TH Chip

Royal Blue & **Orange** Waveforms = 2½ D Field Solver Results

Red & **Light Blue** Waveforms = Hyperlynx Boardsim Results



9TH Chip

Again reasonably high confidence can be extrapolated from the Hyperlynx Boardsim simulations when the signals are power referenced.

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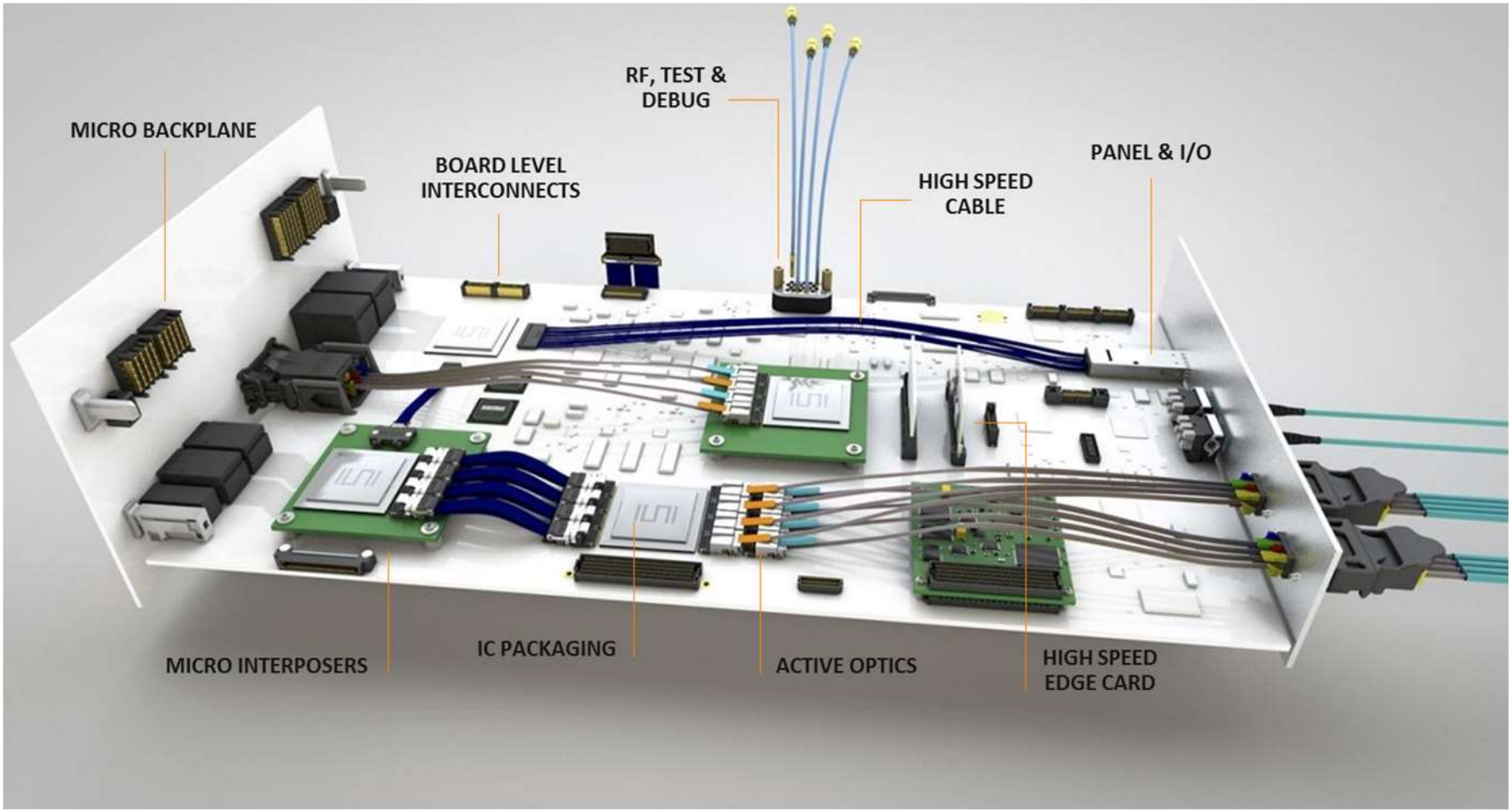
- We have discussed the differences between DDR3 and DDR4 from SI/PI perfective to help us assess what is need to evaluate DDR4 interface
- We have discussed and shown the necessary steps required for achieving a successful DDR4 interface across all operating conditions and timing requirements and standards.
- We have shown some very insightful tool correlation on a routed board between Hyperlynx BoardSim and a 2½ D field solver.
- Original paper from Rula Bakleh, SI/PI Consultant at Teraspeed Consulting

Full Signal Channel Solutions



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