Application Note

DP Array™ Final Inch™ Designs in RapidIO Short Run (Mezzanine) Applications 10mm Stack Height

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Developed in conjunction with
Teraspeed Consulting Group LLC

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Abstract

RapidIO links are based on recent advances in point-to-point interconnect technology. Designed primarily as a physical link intended as a point-to-point interface between devices, a RapidIO lane is comprised of a dual-simplex communications channel between two components physically consisting of two low-voltage, differential signal pairs. As with any modern high speed PCB design, the performance of an actual RapidIO interconnect is highly dependent on the implementation. This paper describes a measurement method applied to proven Samtec Final Inch™ designs and this industry standard to help engineers deploy systems of two PCB cards mated through Samtec's family of high speed electrical connectors, what the RapidIO specification calls "short run" or "short range" transmitter specification. To demonstrate the feasibility of using Samtec DP Array™ DPAM/DPAF connectors with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in spreadsheet format. Also, trace lengths on each side of the DPAM/DPAF connector will be gradually increased to show the limits of compliance.

In order to ensure interoperability between RapidIO transmitter and receiver devices, we will stress a typical interconnect design by stimulating their Spice model components and devices with stressed data patterns. This paper will cover techniques to stress the system with reduced driver amplitude as well as jitter injection.

Introduction

Samtec has developed a full line of connector products that are designed to support serial speeds up to and greater than 3.125 Gb/ps, the highest "Baud rate" of each RapidIO data lane used in this paper. Working with Teraspeed Consulting, they have developed a complete breakout and routing solution for each member of Samtec's line of high speed connectors, called Final Inch™. Samtec has also created a special version of the DPAF/DPAM 10 mm mated height connector called the RapidIO XMC connector. To demonstrate the feasibility of using this connector in RapidIO applications with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in a user-friendly spreadsheet format. Trace lengths will be varied to show the limits of compliance.

Analysis will consist of stimulating a typical trace-connector-trace circuit path with a worst case signal and then observing the corresponding eye closure related to reflections due to impedance discontinuities, loss, and stubs. Next, utility software will be used to extract, analyze, and format Spice-measured voltage amplitudes and differential signal crossing times. Mask violations (see Figure 3) will be recorded in pass/fail format.

Definitions

Interconnect Budget – The amount of loss and jitter that is allowed in the interconnect and still meet the target specification.

Insertion Loss – The differential voltage swing attenuation from transmitter to receiver on the trace. The trace is subject to resistive, dielectric, and skin effect loss. Insertion loss increases as trace length and and/or signal frequency increases. Vias and connectors also exhibit losses which must be included in the interconnect budget.

Jitter – The variation in the time between differential crossings from the ideal crossing time. Jitter includes both data dependent and random contributions on the interconnect.

PRBS – Pseudo Random Bit Sequence.

Tj – Total jitter, which is the convolution of the probability density functions for all the jitter sources, Random jitter (Rj) and Deterministic jitter (Dj). The UI allocation is given as the allowable Tj.

UI – Unit Interval. The time interval required for transmission of one data symbol. For a binary lane operating at 2.5 Gb/p the UI is 400 ps. For 3.125 Gb/s the UI is 320 ps.

$\mathbf{V_{DIFF}}$ – Differential voltage, defined as the difference of the positive conductor voltage and the negative conductor voltage (V_{D+} - V_{D-}).

The RapidIO Specification

RapidIO links are based on recent advances in point-to-point interconnect technology. A RapidIO lane is comprised of a dual-simplex communications channel between two components physically consisting of two low-voltage, differential signal pairs. Four of these lanes are used to convey 32-bit self-clocking data and control, each at a nominal rate of 1.25 GBaud, 2.5 GBaud, or 3.125 GBaud.

The RapidIO specification uses the name "byte stream" to describe one half of a data lane. The design model used for this paper is of six byte streams operating in tandem, one victim surrounded by 5 aggressors, with all bit streams heading in the same direction and passing through the connector on adjacent pin pairs.

Detailed electrical specifications for the electrical sub-block can be found starting in Chapter 8 of the RapidIO specification, available free of charge on their web site (www.**rapidio**.org/specs). Relevant timing and voltage constraints from this section of the specification will be referred to throughout the rest of this paper.

Setup and Measurement

Input Stimulus Setup

A PRBS 2^7-1 pattern was used for victim stimulus and a repeating 1010… pattern used for the aggressor differential pairs on each side of the victim differential pair. Xilinx supplies a stimulus generator tool kit within their VirtexII Pro™ design kit giving customers complete control over the amount of jitter in the transmitter's data output. Using their stimulus system with their RocketIO™ multi-gigabit serial transceiver model, enough total jitter was added to the driver output to just meet worst case RapidIO transmit jitter specifications. The slow-slow corner silicon model was used to come as close as possible to the minimum differential V_{DIFF} output specification. An adjustable attenuator was then used to match the RapidIO TX $Vdiff_{p-p}$(min) specification.

The Test Circuit Model

The test circuit modeled is shown in Figure 1. It consists of the following:

- One set of six of Xilinx Virtex-II Pro™ serial differential transceiver models configured as RapidIO drivers.
- Xilinx FPGA flip-chip package model.
- 1 Samtec DP Array™ Final Inch™ design, comprised of the DP Array connector model surrounded by Samtec's Break Out Routing (BOR) models, lossy trace models, and SMA connector models on both sides of the connector.
- One set of 12 AC coupling capacitors, value = 100 nF.
- One set of six 100 Ohm termination resistors.

The DP Array® connector is an array style connector tailored for differential signal pairs with 10mm mated height. Contact Samtec for more details, product series DPAM and DPAF.

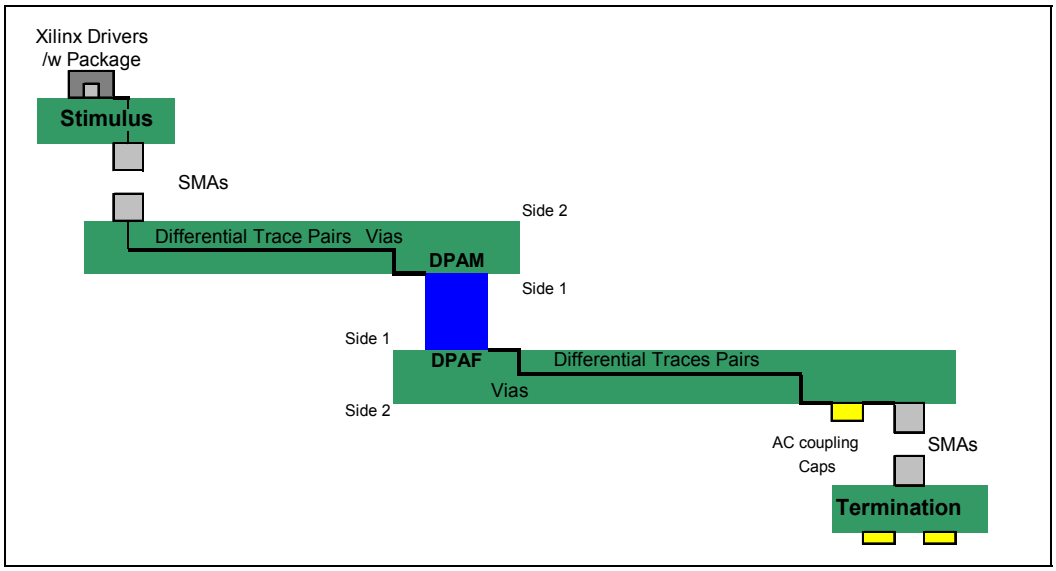


Figure 1 - RapidIO Test Circuit

The DP Array™ connector model signal mapping is shown in Figure 2.

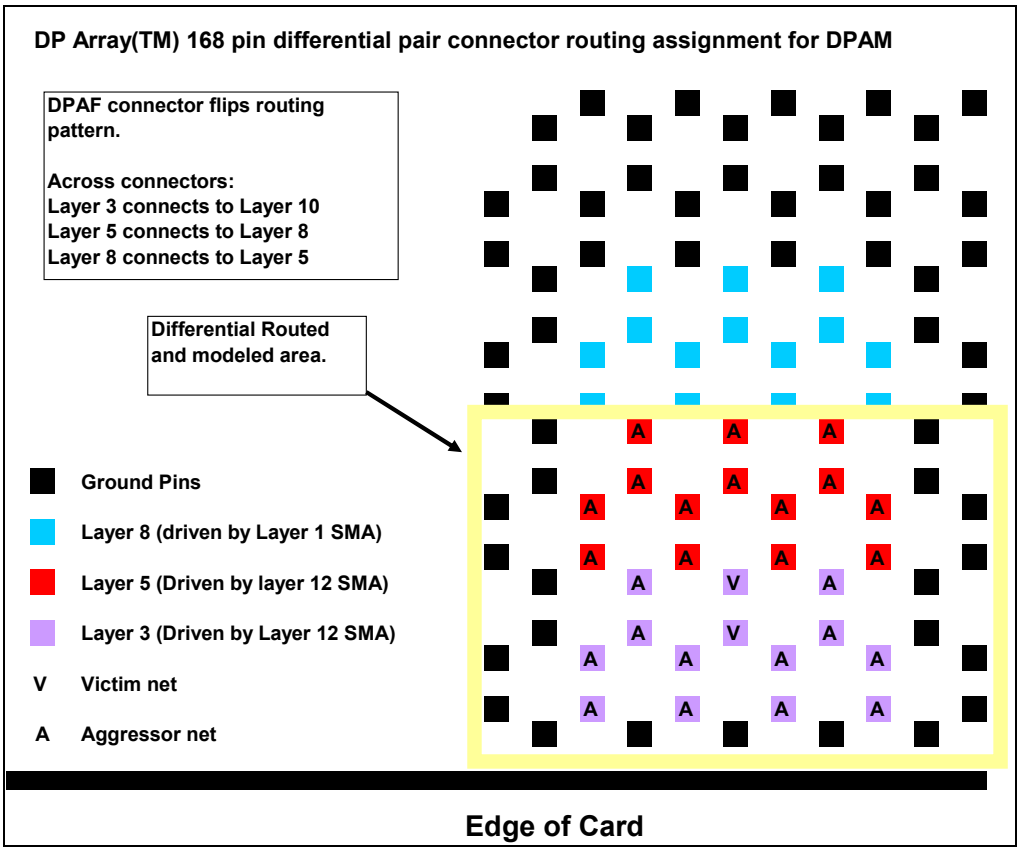


Figure 2 – RapidIO signal mapping of DP Array™ connector in Final Inch™ test circuit

Procedure

Interconnect Budget

The interconnect budget can be best illustrated by the mask shown in Figure 3. In order to pass the RapidIO constraints for loss and jitter, the simulated eye waveform must not touch any location within the grey areas shown. Calculated interconnect budget values are shown in Table 3.

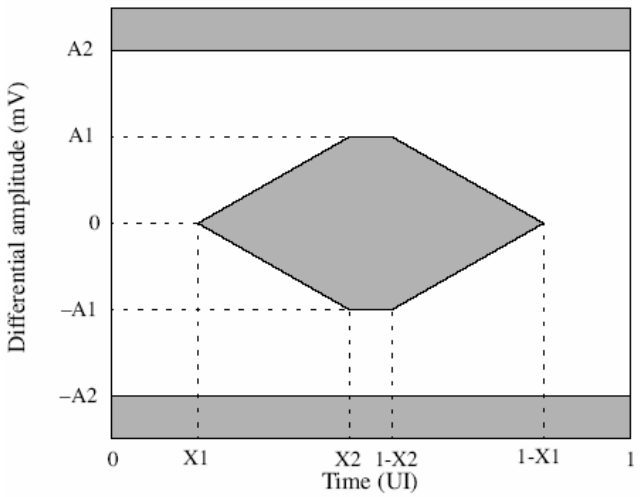


Figure 3 - Example mask template

Interval (See Fig. 3)	Near-end value	Far-end value	Units
X1 to 1-X1	260	140	psec
X2 to 1-X2	88	64	psec
A1 to –A1	500	175	mV_{p-p}
A2 to –A2	1000	1600	mV_{p-p}

Table 1 – RapidIO Short Run Driver template intervals at 2.5 Gb/s

Interval (See Fig. 3)	Near-end value	Far-end value	Units
X1 to 1-X1	208	128	psec
X2 to 1-X2	70.4	51.2	psec
A1 to –A1	500	175	mV_{p-p}
A2 to –A2	1000	1600	mV_{p-p}

Table 2 – RapidIO Short Run Driver template intervals at 3.125 Gb/s

	Maximum Loss, A1 to –A1, Both Frequencies ($V_{DIFFp-p}$)	Minimum Eye Width, 2.5Gb/ps X1 to 1-X1	Minimum Eye Width, 3.125 Gb/ps X1 to 1-X1
Driver at Package Pin	0.500	0.65UI	0.65UI
Receiver at Package Pin	0.175	0.35UI	0.40UI
Interconnect budget:	0.350	0.3UI	0.25UI
	9.12 dB loss[1]	120 ps	80 ps

Table 3 - RapidIO short run interconnect budget max loss and min eye width calculated values

[1]The worst case operational loss budget at 1.25 GHz Nyquist frequency is calculated by taking the minimum input voltage to the receiver ($V_{RX-DIFF}$ = 175 mV) divided by the minimum driver output voltage ($V_{TX-DIFF}$ = 500 mV). 175/500 = .35, which after conversion results in a maximum loss budget of 9.12 dB.

Transmitter Compliance Measurements

Setup for Tj for UI Measurements

As mentioned in the previous section, the driver stimulus' jitter was adjusted until the transmitter exhibited the maximum total jitter allowed by the RapidIO specification at the driver package pins under the compliance load shown in Figure 4 below. The RapidIO specification does not specify the range of capacitor values allowed for the AC coupling capacitors. We set C to 100nF for all simulations because it is a popular value in the industry. Table 3 shows the resulting output measurements.

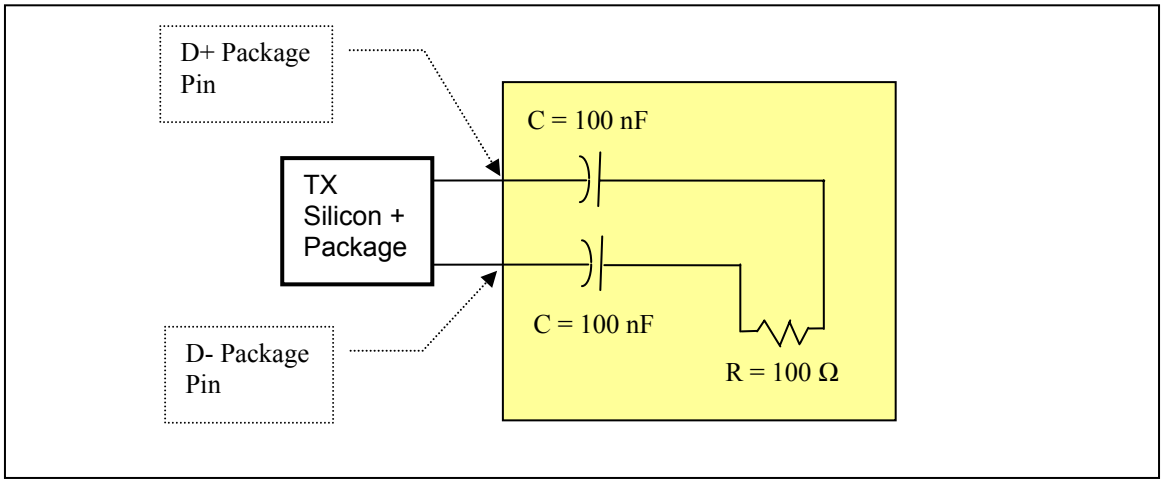


Figure 4 - RapidIO Compliance Test/Measurement load

	V_{p-p}	Total Jitter @ 2.5 Gb/s	Total Jitter @ 3.125 Gb/s
Specification	≥500 mV	≤ 140 psec	≤ 112 psec
Measured	500.8 mV	140.2 psec	111.9 psec

Table 4 - RapidIO TX Silicon + Package Measurements at TX Package Pin

The eye pattern generated in the RapidIO driver compliance test simulations can be found in Appendix A of this paper, pictures #1 and #3.

Full Circuit Compliance Measurements

Differential Voltage and Eye Width Measurements at Receiver End

2.5 Gb/s Data Rate

DPAM/DPAF Connector, 10 mm Stack Height	Max Jitter at UI = 400 psec	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Min Rx Differential Voltage, A1 to –A1[1] (See example mask template)	Pass/Fail
Specification	**≤ 260 psec**	**≥140 psec**	**≥175mV$_{p-p}$**	-
10" total trace[2]	172.4	386.9	327.8	Pass
20" total trace	172.3	381.6	250.6	Pass
30" total trace	173.0	371.7	200.2	Pass
35" total trace	176.8	369.5	188.6	Pass
36" total trace	176.3	367.7	182.8	Pass
37" total trace	173.5	365.2	173.4	Fail

Table 5 – DPAM/DPAF RapidIO Measurements at Receiver End, 2.5 Gb/s data rate

[1]X2 to 1-X2, the received bit sample interval, is 64 psec when UI = 400 psec.

[2]The total trace length specified is the sum of the two differential trace lengths in the DPAM/DPAF test fixture model, as shown in Figure 1. These traces are always kept equal in length in each simulation.

The 2.5 Gb/s eye pattern generated in the RapidIO circuit simulation with 36 inches total trace length can be found in Appendix A of this paper, picture #2.

3.125 Gb/s Data Rate

Instead of starting from scratch, we'll start the 3.125 Gb/s simulations based on the insertion loss of the circuit with 36 inches of trace. The insertion loss of the RapidIO circuit with various trace lengths is shown in Figure 4. At the Nyquist frequency for the 2.5 Gb/s data rate (1.25 Gb/s), the insertion loss of the circuit with 36 inches total trace length is -10.4 dB. Moving over to the Nyquist frequecy for 3.125 Gb/s data rate (1.5625

Gb/s) shows that the insertion loss for the circuit with 29 inches of total trace length is well above -10.4 dB, but 30 inches of total trace is below -10.4 dB. Therefore, 29 inches of trace is a good place to start the 3.125 Gb/s RapidIO simulations.

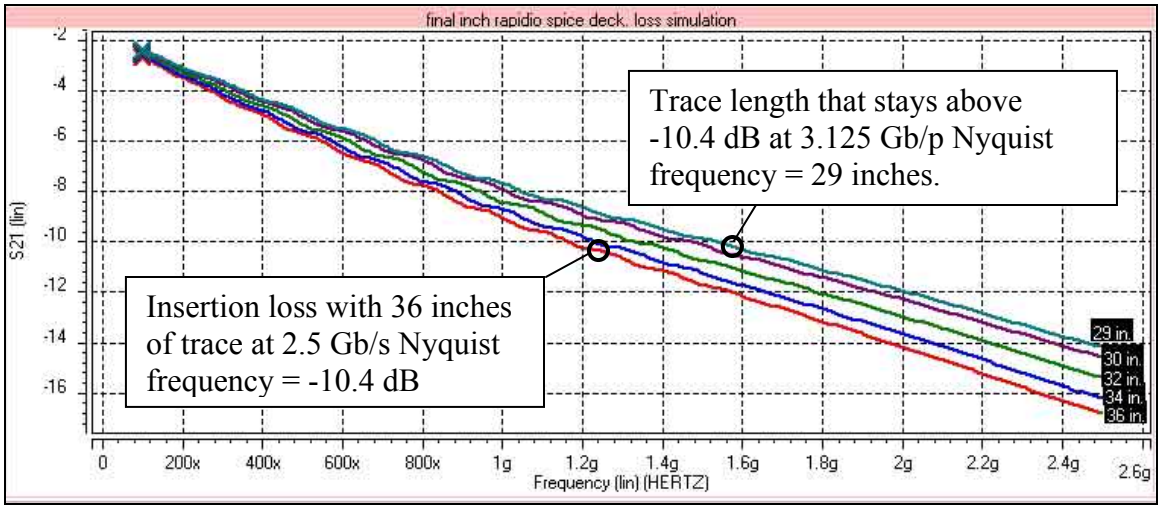


Figure 5 - RapidIO circuit insertion loss at various trace lengths

DPAM/DPAF Connector, 10 mm Stack Height	Max Jitter at UI = 320 psec	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Min Rx Differential Voltage, A1 to –A1[1] (See example mask template)	Pass/Fail
Specification	**≤ 208 psec**	**≥112 psec**	**≥175mV$_{p-p}$**	-
29" total trace	128.8	293.2	196.1	Pass
31" total trace	131.7	293.1	186.0	Pass
33" total trace	132.1	293.3	180.5	Pass
34" total trace	129.5	292.9	179.5	Pass
35" total trace	132.7	289.5	172.0	Fail

Table 6 - RapidIO Measurements at Receiver End, 3.125 Gb/s data rate

[1]X2 to 1-X2, the received bit sample interval, is 51.2 psec when UI = 320 psec.

[2]The total trace length specified is the sum of the two differential trace lengths in the DPAM/DPAF test fixture model, as shown in Figure 1. These traces are always kept equal in length in each simulation.

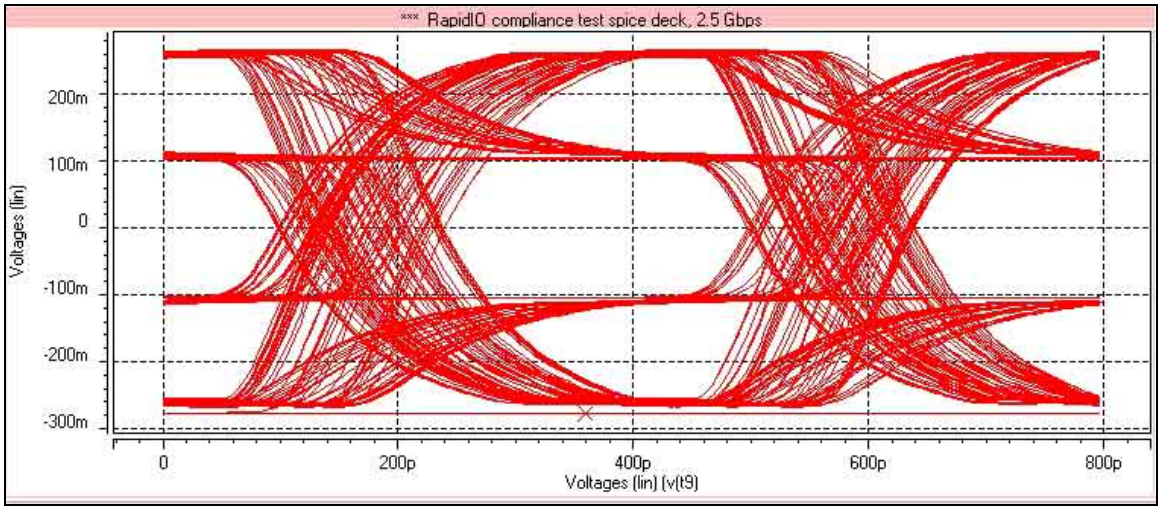
The 3.125 Gb/s eye pattern generated in the RapidIO circuit simulation with 34 inches total trace length can be found in Appendix A of this paper, picture #4.

Conclusions

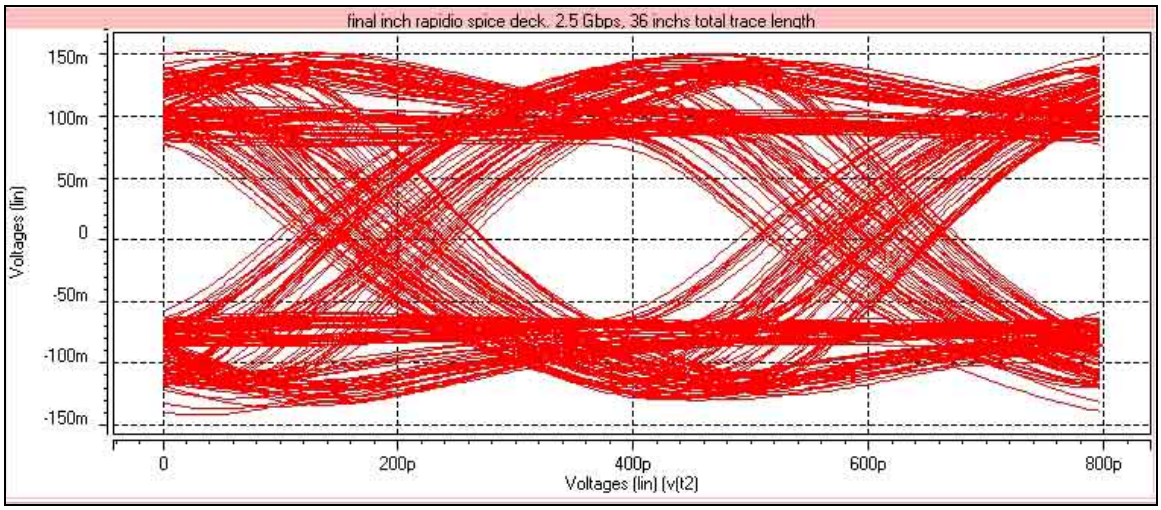
A single Samtec DP Array™ DPAM/DPAF 10 mm stack height connector in a board-to-board configuration can be used in RapidIO systems with total trace lengths not to exceed 36 inches at 2.5 Gb/s data rates, or 34 inches at 3.125 Gb/s data rates, when used with

Samtec's Final Inch™ routing, breakout, and trace width solutions. Because loss is the dominant contributor to system degradation, designers should be aware that using smaller trace widths, laminates with higher loss tangent, and sub optimal routing solutions with higher pair-to-pair coupling and additional via stubs will decrease overall performance and the maximum allowable trace length. It is advisable when designing systems that approach the maximum jitter limits to perform detailed modeling, simulation, and measurement of the target design including the effects of material properties, traces, vias, and additional components.

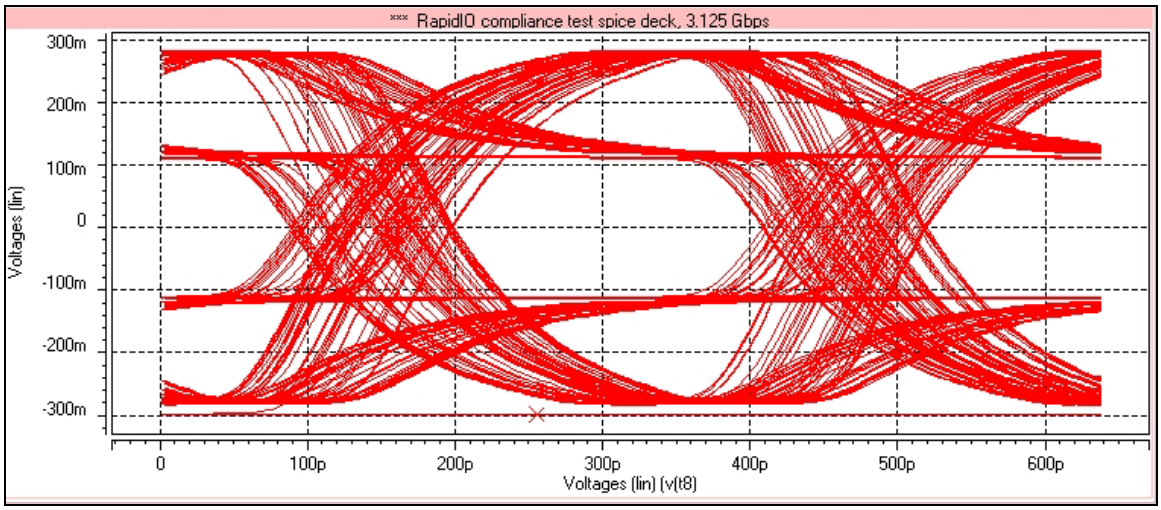
Appendix A – Waveform images



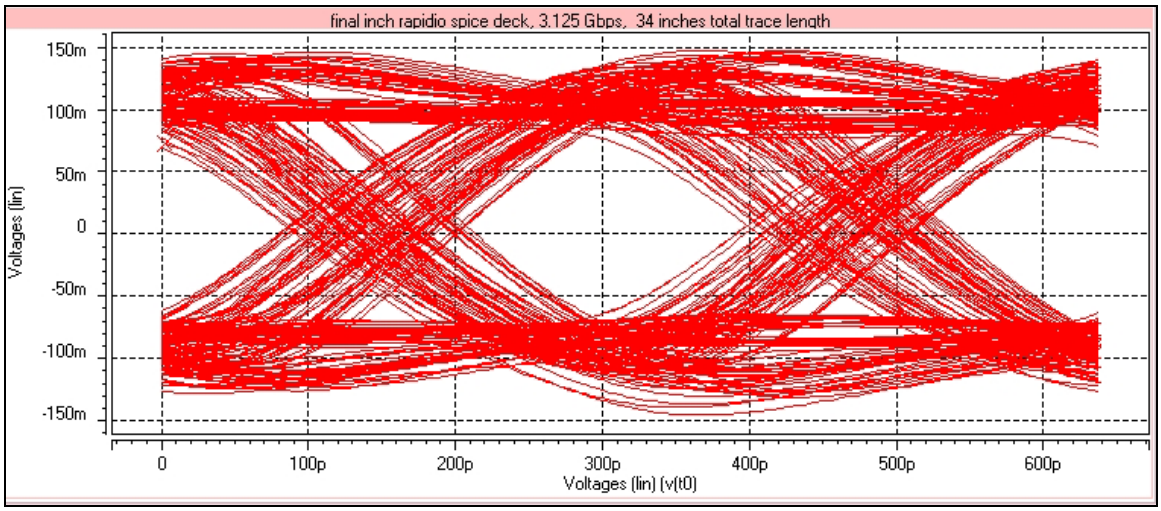
Picture 1 – Worst case stimulus eye waveform at 2.5 Gb/s, probed at Xilinx driver package pins, connected to compliance test/measurement load



Picture 2 – RapidIO circuit eye waveform at 2.5 Gb/s, probed at terminator pins, 36 inches total trace length



Picture 3 – Worst case stimulus eye waveform at 3.125 Gb/s, probed at Xilinx driver package pins, connected to compliance test/measurement load



Picture 4 – RapidIO circuit eye waveform at 3.125 Gb/s, probed at terminator pins, 34 inches total trace length