



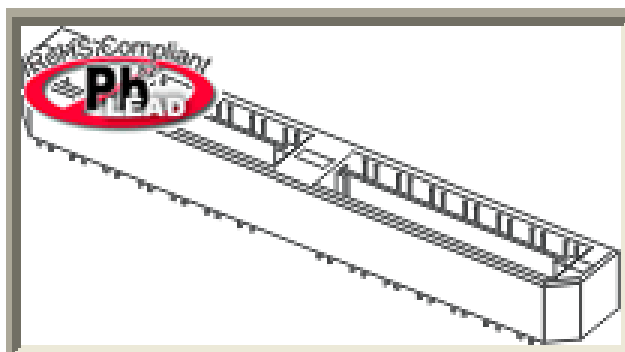
High Speed Characterization Report

Contact Plating Effects on Signal Integrity Gold on Post / Gold on Tail

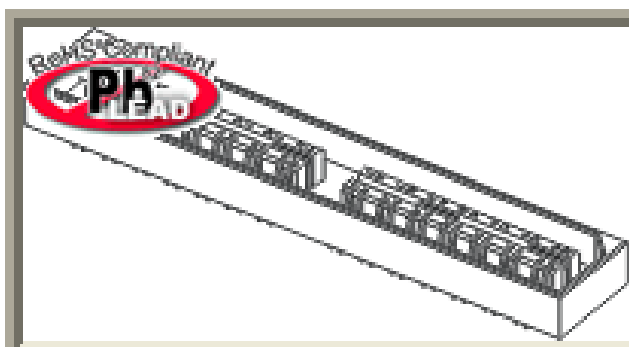
vs.

Gold on Post / Matte Tin on Tail

QTE-028-01-L-D-DP-A



Mated With



QSE-028-01-L-D-DP-A

Description:

Parallel Board-to-Board, Q Pair, 5mm (0.197") Stack Height

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

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Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Connector Overview

Q Pair interfaces (QSE-DP/QTE-DP Series) are available with up to 70 contacts per row and with standard board-to-board spacing of 5mm (0.197"), 8mm (0.315"), 11mm (0.433"), 16mm (0.630"), 19mm (0.748"), and 25mm (0.984") between boards. This report contrasts the hi-speed performance of two terminal plating schemes, gold on the post & gold on the tail compared to gold on the post & tin on the tail. The report covers plating contrasts of the Q Pair (DP) 5mm stack height.

Test Results Disclaimer

Background:

In the past several contact terminal plating options have been offered to Samtec customers. Generally the status quo has been an all gold plating applied to the post and tail of the terminal. An option is matte tin plating applied on the tail with the gold plating still applied at the post of the terminal. Samtec has recently started to supply only the gold on post/ matte tin on tail terminal plating in order to make use of the process advantages offered by using matte tin. There will be no change to the Samtec part number to indicate gold on post/ matte tin on tail only offering.

Purpose:

To provide to the customer a full high-speed characterization report that indicates electrical properties are not compromised by the changes made in the plating materials or plating processes. All data presented in this report is subject to the same characterization procedures and formats as contained in a Samtec High-Speed Connector Characterization Report.

Procedure:

Fabricate two sets of test board fixtures, one set populated with terminal contacts employing the all gold plating applied to the post and tail of the terminals and the second set employing matte tin on the tail with gold plating on the post. Perform a full high-speed characterization of a ground referenced differential pair configuration and compare results using the Samtec Speed Rating report process based on the -3 dB insertion loss point of the connector system.

Results:

Performance ratings tested identical at 8.0GHz /16Gbps for Q Pair differential test points. The largest differential frequency band of separation at the -3dB point was 320MHz with a 20MHz step frequency. Differential -3dB points occurred at 7.56 GHz for gold tail plating and 7.88 GHz for matte tin plated tails. Return Loss ratings for the differential signaling environment were -3dB. Impedance profiles were similar in shape and magnitude. Changes are less than 1.5 ohms in amplitude at a 35±5ps risetime.

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

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There is no significant difference in the percentages of time domain crosstalk or frequency response in the frequency domain crosstalk whether it be a near-end or a far-end case.

Conclusion:

Changes to metal alloys and plastic materials whether it be composition of the materials or geometric modifications raises concern as to the effects it may cause on the electrical properties of the device. For this test printed circuit board fixtures and connector bodies were manufactured using the standard materials and processes. The difference between one set of the test samples lies in the plating of the terminals where matte tin plating is substituted for the gold plating at the tail of the terminal.

This exercise was a comprehensive SI characterization of the QXX series connector system. The characterization screens the 5mm and 25mm stack heights systems. It also examines three system configurations in a two-level signaling environment and under worst and best case conditions. In total, the system characterization outcome is over 700 SI measurements culminating into four separate Samtec Hi-Speed Characterization Reports. This report examines the results from the 5mm stack height QSE-DP/QSE-DP connector series and concludes that **“the addition of the matte tin plating finish in place of a gold finish at the tail of the terminal contributes little, if at all, to any change in the connector series SI performance”**. Results from this test can be examined and compared on the following pages

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height
Description: Contact Plating Effects on Signal Integrity

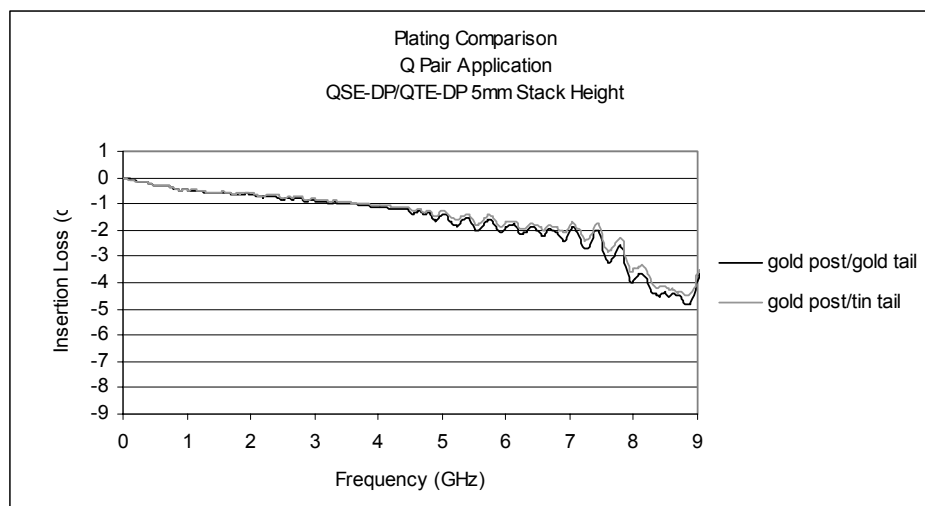
Frequency Domain Data Summary

Gold on Post / Gold on Tail

Gold on Tail – Q Pair Differential Connector System Bandwidth		
Test Parameter	Configuration	
Insertion Loss	GSSG	-3dB @ 7.56 GHz
Return Loss	GSSG	$\leq -5\text{dB}$ to 7.56 GHz
Near-End Crosstalk	GAAQQG	$\leq -25\text{dB}$ to 7.56 GHz
	Xrow, GAAG to GQQG	$\leq -42\text{dB}$ to 7.56 GHz
Far-End Crosstalk	GAAQQG	$\leq -32\text{dB}$ to 7.56 GHz
	Xrow, GAAG to GQQG	$\leq -40\text{dB}$ to 7.56 GHz

Gold on Post / Tin on Tail

Tin on Tail – Q Pair Differential Connector System Bandwidth		
Test Parameter	Configuration	
Insertion Loss	GSSG	-3dB @ 7.88 GHz
Return Loss	GSSG	$\leq -5\text{dB}$ to 7.88 GHz
Near-End Crosstalk	GAAQQG	$\leq -25\text{dB}$ to 7.88 GHz
	Xrow, GAAG to GQQG	$\leq -42\text{dB}$ to 7.88 GHz
Far-End Crosstalk	GAAQQG	$\leq -32\text{dB}$ to 7.88 GHz
	Xrow, GAAG to GQQG	$\leq -40\text{dB}$ to 7.88 GHz

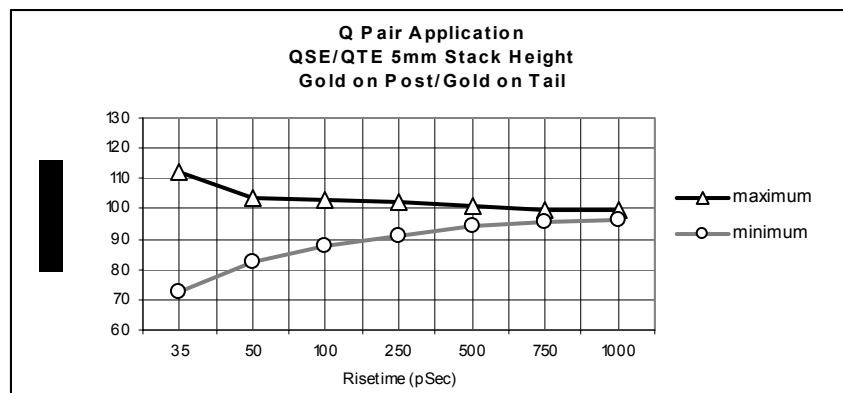


Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height
Description: Contact Plating Effects on Signal Integrity

Time Domain Data Summary

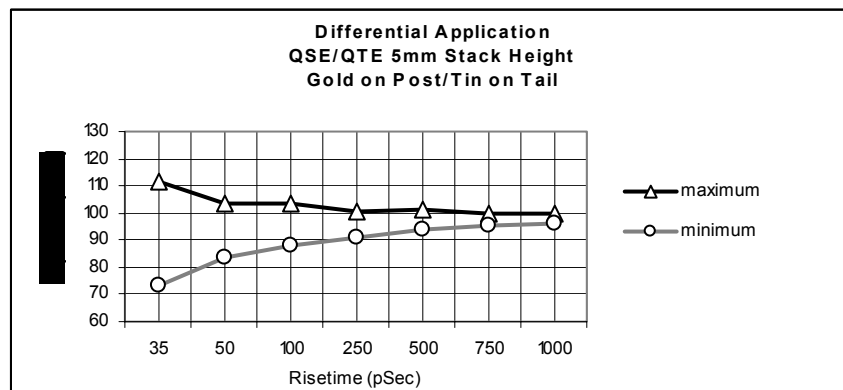
Gold on Post / Gold on Tail

Gold on Tail - Differential Impedance (Ω)							
Signal Risetime	30 $\pm$ 5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
Maximum Impedance	111.9	103.7	103.2	102.1	101.1	99.8	99.5
Minimum Impedance	72.3	82.8	87.7	90.9	94.0	95.7	96.5



Gold on Post / Tin on Tail

Tin on Tail - Differential Impedance (Ω)							
Signal Risetime	30 $\pm$ 5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
Maximum Impedance	111.4	103.8	103.2	100.4	101.1	99.8	99.5
Minimum Impedance	73.3	83.3	88.2	90.8	93.9	95.7	96.4



Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

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Gold on Post / Gold on Tail

Gold on Tail - Differential Crosstalk (%)								
Input (t _r)		30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	GAAQQG	1.7	1.4	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	Xrow ^{diff}	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	GAAQQG	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	Xrow ^{diff}	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Gold on Post / Tin on Tail

Tin on Tail - Differential Crosstalk (%)								
Input (t _r)		30±5ps	50 ps	100 ps	250 ps	500 ps	750 ps	1 ns
NEXT	GAAQQG	1.7	1.4	1.1	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	Xrow ^{diff}	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
FEXT	GAAQQG	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%
	Xrow ^{diff}	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%	< 1.0%

Gold on Post / Gold on Tail

Gold on Tail - Propagation Delay (Mated Connector)	
Q Pair (differential)	82 ps

Gold on Post / Tin on Tail

Tin on Tail - Propagation Delay (Mated Connector)	
Q Pair (differential)	82 ps

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Characterization Details

This report presents data which characterizes the signal integrity response of a connector pair in a controlled printed circuit board (PCB) environment. All efforts are made to reveal typical best-case responses inherent to the system under test (SUT).

In this report, the SUT includes the test PCB from drive side probe tips to receive side probe tips. PCB effects are not removed or de-embedded from the test data. PCB designs with impedance mismatch, large losses, skew, cross talk, or similar impairments can have a significant impact on observed test data. Therefore, great design effort is put forth to limit these effects in the PCB utilized in these tests. Some board related effects, such as pad-to-ground capacitance and trace loss, are included in the data presented in this report. But other effects, such as via coupling or stub resonance, are not evaluated here. Such effects are addressed and characterized fully by the Samtec [Final Inch®](#) products.

Additionally, intermediate test signal connections can mask the connectors' true performance. Such connection effects are minimized by using high performance test cables, adapters, and microwave probes. Where appropriate, calibration and de-embedding routines are also used to reduce residual effects.

Differential and Single-Ended Data

Most Samtec connectors can be used successfully in both differential and single-ended applications. However, electrical performance will differ depending on the signal drive type. In this report, data is presented for both differential and single-ended drive scenarios.

Connector Signal to Ground Ratio

Samtec connectors are most often designed for generic applications, and can be implemented using various signal and ground pin assignments. In high speed systems, provisions must be made in the interconnect for signal return currents. Such paths are often referred to as "ground". In some connectors, a ground plane or blade, or an outer shield is used as the signal return, while in others, connector pins are used as signal returns. Various combinations of signal pins, ground blades, and shields can also be utilized. Electrical performance can vary significantly depending upon the number and location of ground pins.

In general, the more pins dedicated to ground, the better electrical performance will be. But dedicating pins to ground reduces signal density of a connector. So care must be taken when choosing signal/ground ratios in cost- or density-sensitive applications.

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

For this connector, the following configurations were evaluated:

Single-Ended Impedance:

- GSG (ground-signal-ground)

Single-Ended Crosstalk:

- Electrical "worst case": GAQG (ground-active-quiet-ground)
- Electrical "best case": GAGQG (ground-active-ground-quiet-ground)
- Across row: Xrow^{se} (from one row of terminals to the other row across the ground blade)

Differential Impedance:

- GSSG (Ground-positive signal-negative signal-ground)

Differential Crosstalk:

- Electrical "worst case": GAAQQG (ground-active-active-quiet-quiet-ground)
- Electrical "best case": GAAGQQG (ground-active-active-ground-quiet-quiet-ground)
- Across row: Xrow^{diff} (from one row of terminals to the other row across the ground blade)

In all cases in this report, the center ground blade of the connector was grounded to the PCB. Only one single-ended signal or differential pair was driven for crosstalk measurements.

Other configurations can be evaluated upon request. Please contact sig@samtec.com for more information.

In a real system environment, active signals might be located at the outer edges of the signal contacts of concern, as opposed to the ground signals utilized in laboratory testing. For example, in a single-ended system, a pin-out of "SSSS", or four adjacent single ended signals, might be encountered, as opposed to the "GSG" and "GSSG" configurations tested in the laboratory. Electrical characteristics in such applications could vary slightly from laboratory results. But in most applications, performance can safely be considered equivalent.

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Description: Contact Plating Effects on Signal Integrity

Signal Edge Speed (Rise Time):

In pulse signaling applications, the perceived performance of an interconnect can vary significantly depending on the edge rate or rise time of the exciting signal. For this report, the fastest rise time used was 30 +/-5 ps. Generally, this should demonstrate worst case performance.

In many systems, the signal edge rate will be significantly slower at the connector than at the driver launch point. To estimate interconnect performance at other edge rates, data is provided for several rise times between 30 ps and 1.0 ns.

For this report, rise times were measured at 10%-90% signal levels.

Frequency Domain Data

Frequency domain parameters are helpful in evaluating the connector system's signal loss and crosstalk characteristics across a range of sinusoidal frequencies. In this report, parameters presented in the frequency domain are insertion loss, return loss, and near-end and far-end crosstalk. Other parameters or formats, such as VSWR or S-parameters, may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Frequency performance characteristics for the SUT are generated from time domain measurements using Fourier Transform calculations. Procedures and methods used in generating the SUT's frequency domain data are provided in the frequency domain test procedures in [Appendix E](#) of this report.

Time Domain Data

Time Domain parameters indicate impedance mismatch versus length, signal propagation time, and crosstalk in a pulsed signal environment. Time Domain data is provided in [Appendix E](#) of this report. Parameters or formats not included in this report may be available upon request. Please contact our Signal Integrity Group at sig@samtec.com for more information.

Reference plane impedance is 50 ohms for single-ended measurements and 100 ohms for differential measurements. The fastest risetime signal exciting the SUT is 30 ± 5 picoseconds.

In this report, propagation delay is defined as the signal propagation time through the PCB connector pads and connector pair. It does not include PCB traces. Delay is measured at 30 ± 5 picoseconds signal risetime. Delay is calculated as the difference in time measured between the 50% amplitude levels of the input and output pulses.

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Crosstalk or coupled noise data is provided for various signal configurations. All measurements are single disturber. Crosstalk is calculated as a ratio of the input line voltage to the coupled line voltage. The input line is sometimes described as the active or drive line. The coupled line is sometimes described as the quiet or victim line. Crosstalk ratio is tabulated in this report as a percentage. Measurements are made at both the near-end and far-end of the SUT.

Data for other configurations may be available. Please contact our Signal Integrity Group at sig@samtec.com for further information.

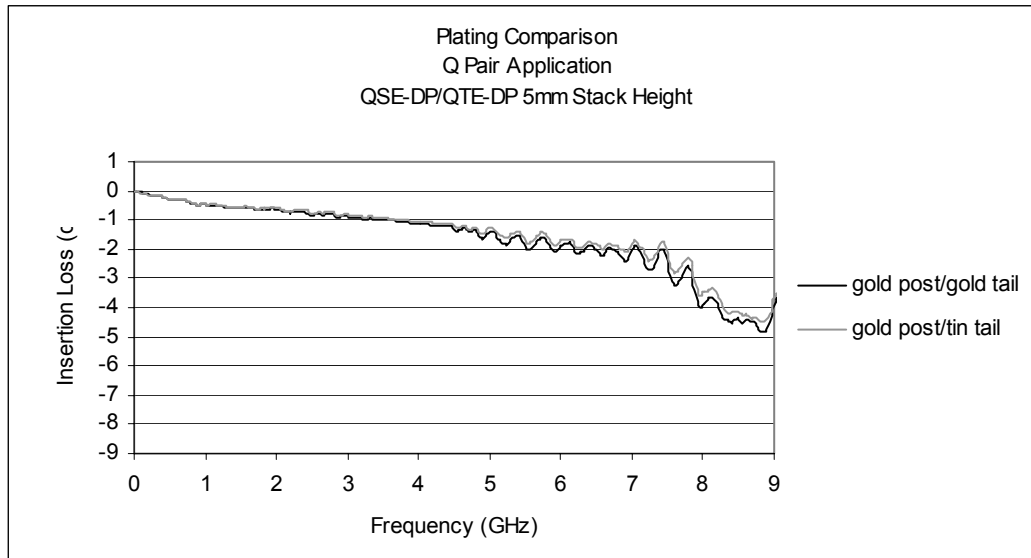
As a rule of thumb, 10% crosstalk levels are often used as a general first pass limit for determining acceptable interconnect performance. But modern system crosstalk tolerance can vary greatly. For advice on connector suitability for specific applications, please contact our Signal Integrity Group at sig@samtec.com.

Additional information concerning test conditions and procedures is located in the appendices of this report. Further information may be obtained by contacting our Signal Integrity Group at sig@samtec.com.

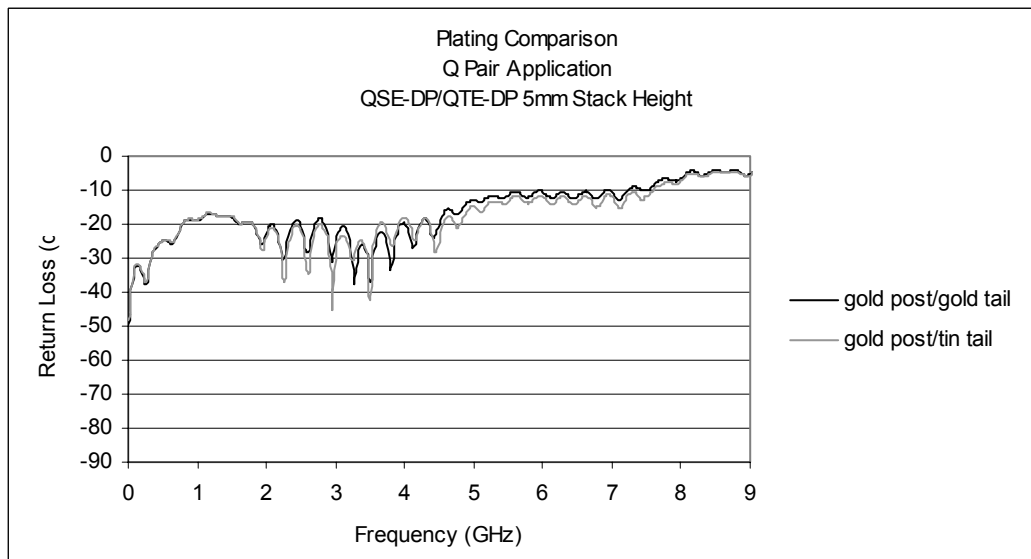
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Description: Contact Plating Effects on Signal Integrity

Appendix A – Frequency Domain Response Graphs

Differential Application – Insertion Loss



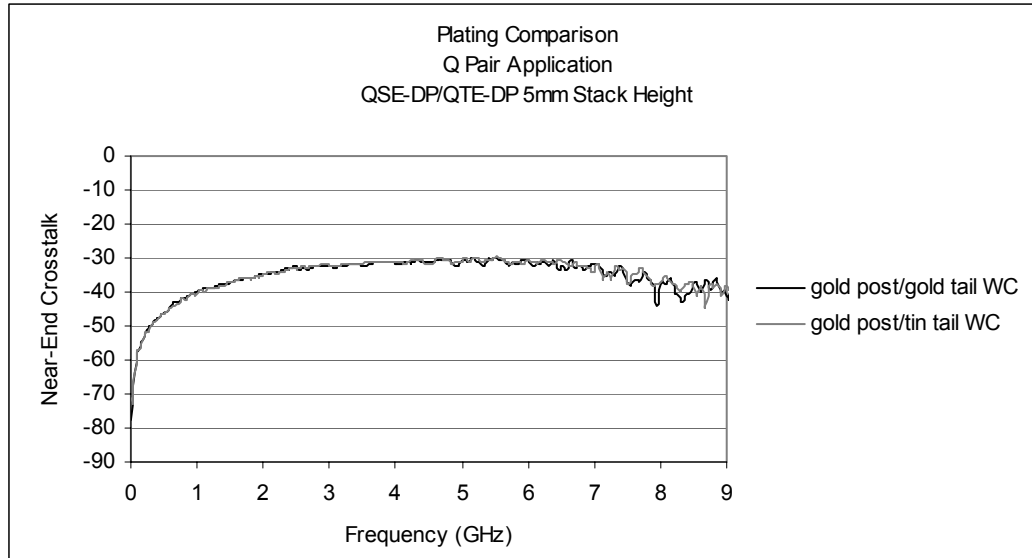
Differential Application – Return Loss



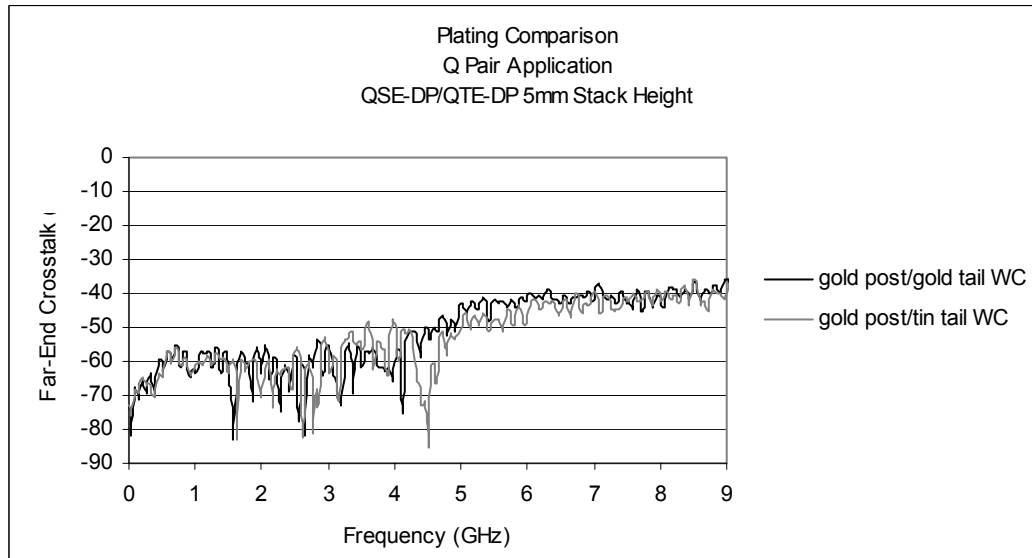
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Description: Contact Plating Effects on Signal Integrity

Differential Application –Worst Case NEXT



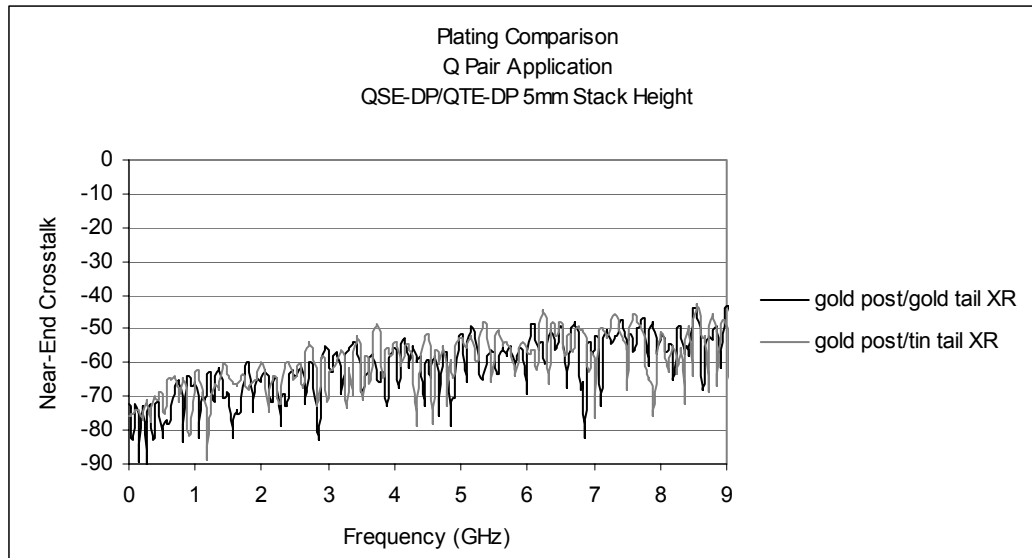
Differential Application –Worst Case FEXT



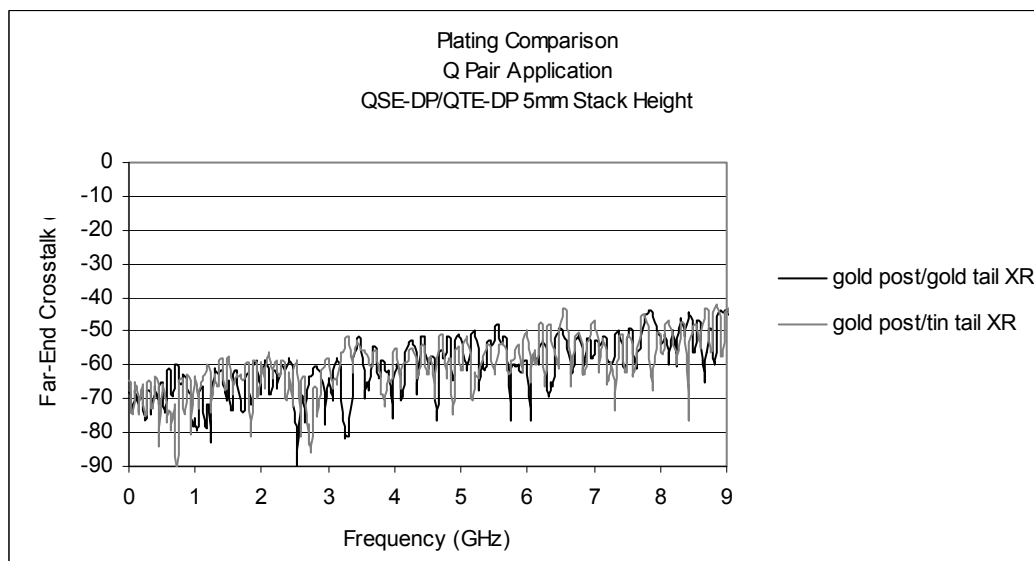
Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Differential Application – Across Row NEXT



Differential Application – Across Row FEXT

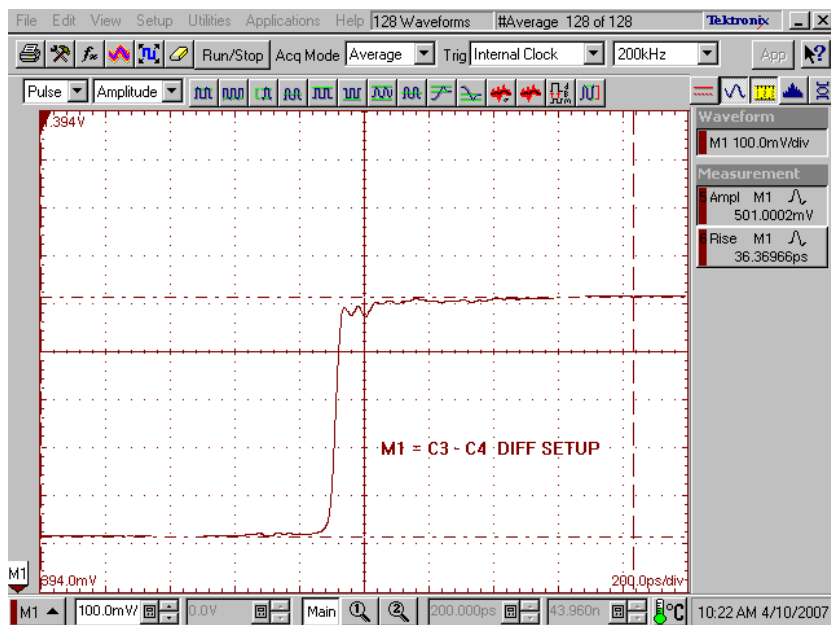


Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Appendix B – Time Domain Response Graphs

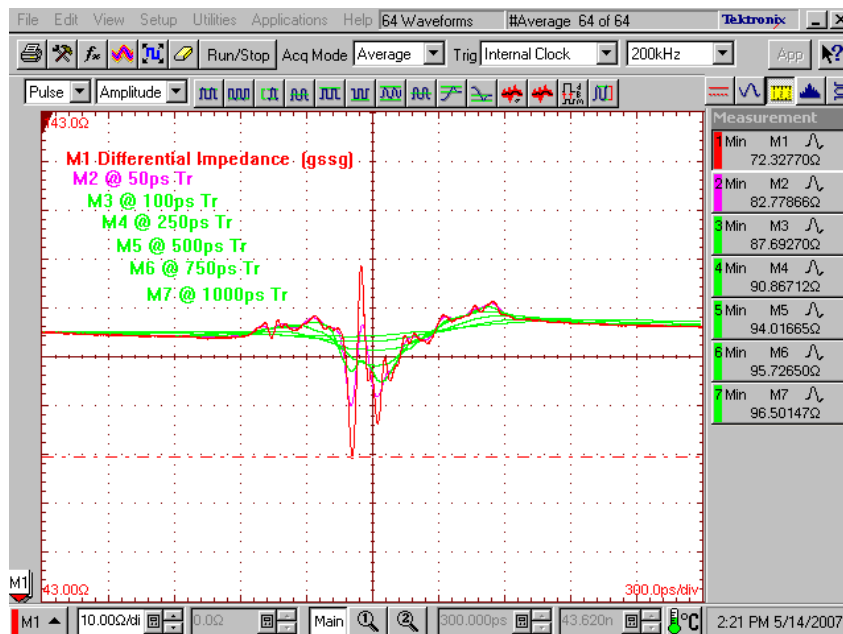
Differential Application – Input Pulse



Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height
Description: Contact Plating Effects on Signal Integrity

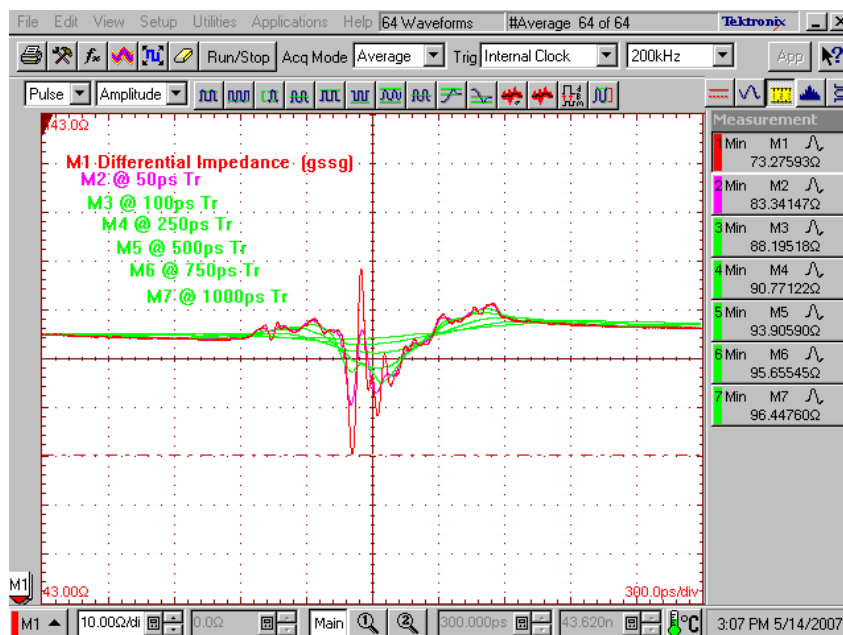
Differential Application – Impedance

Gold on Post, Gold on Tail



Differential Application – Impedance

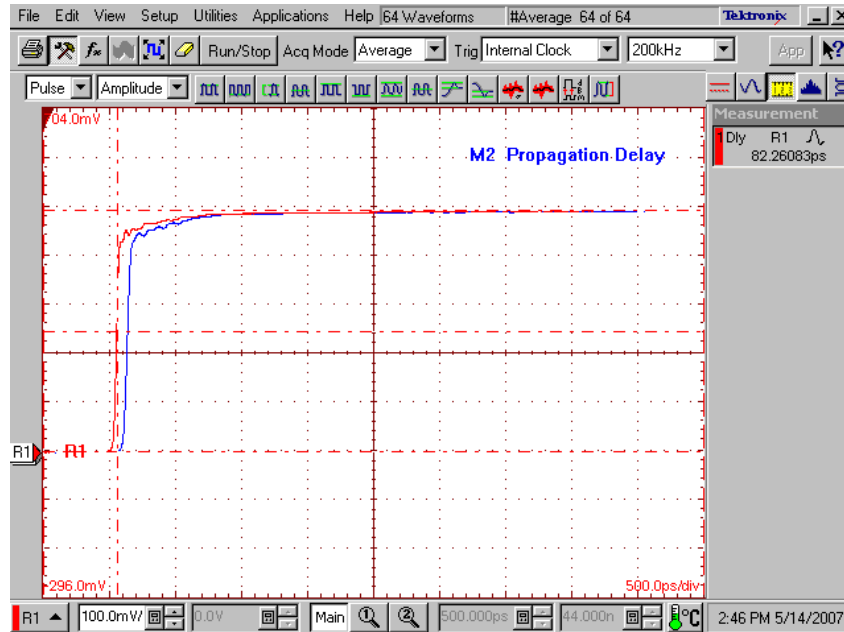
Gold on Post, Tin on Tail



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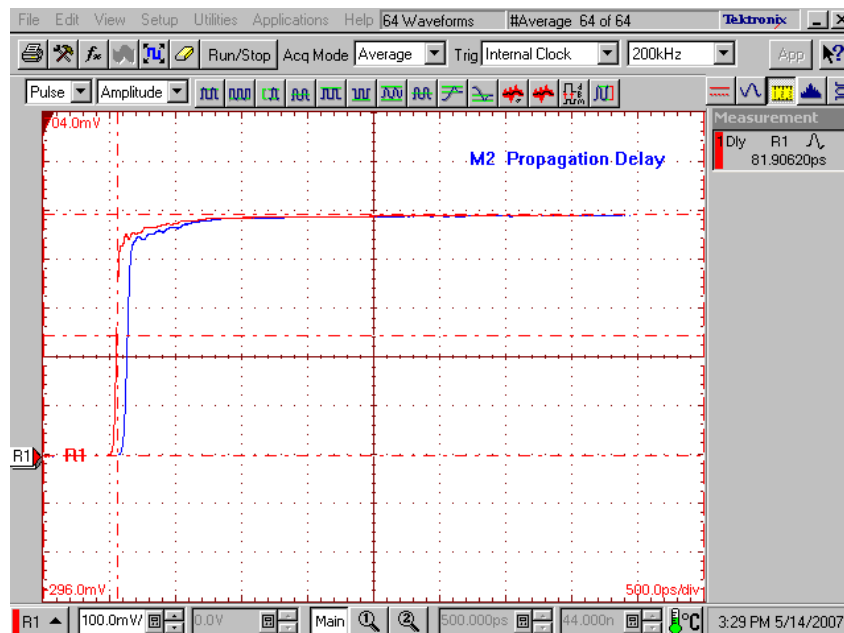
Differential Application – Propagation Delay

Gold on Post, Gold on Tail



Differential Application – Propagation Delay

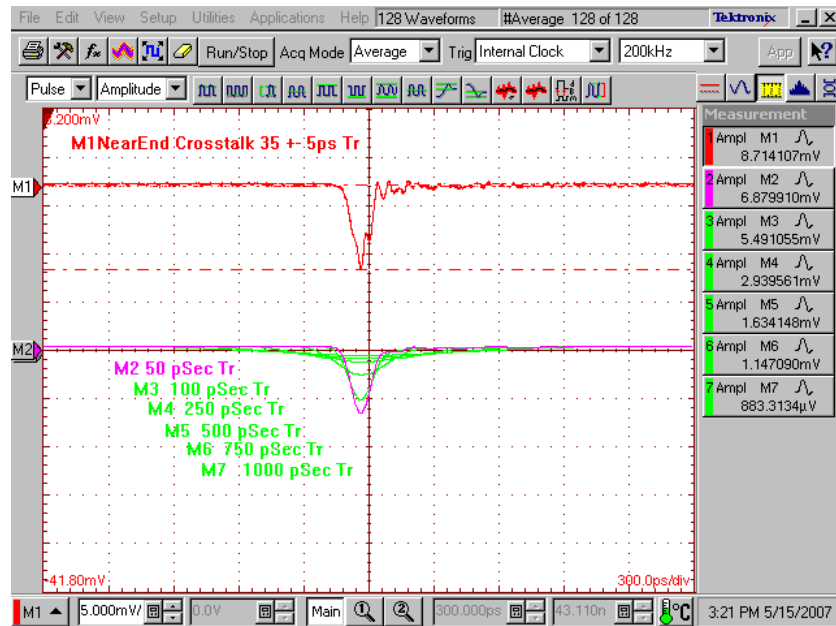
Gold on Post, Tin on Tail



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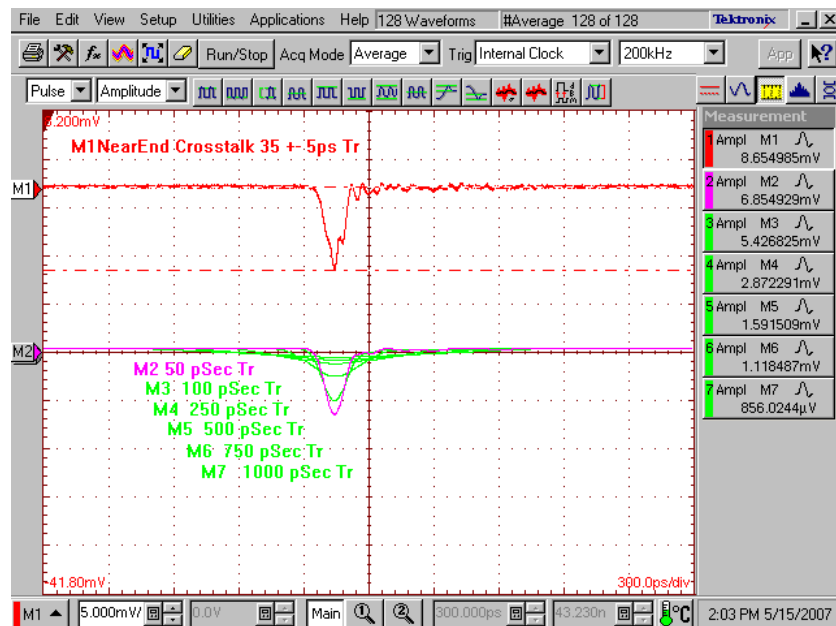
Differential Application – NEXT, “Worst Case” Configuration

Gold on Post, Gold on Tail



Differential Application – NEXT, “Worst Case” Configuration

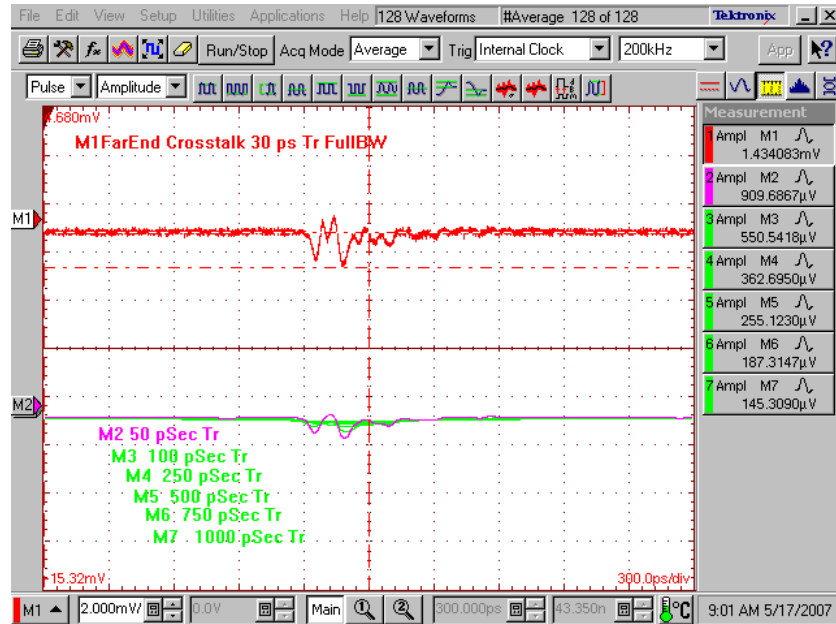
Gold on Post, Tin on Tail



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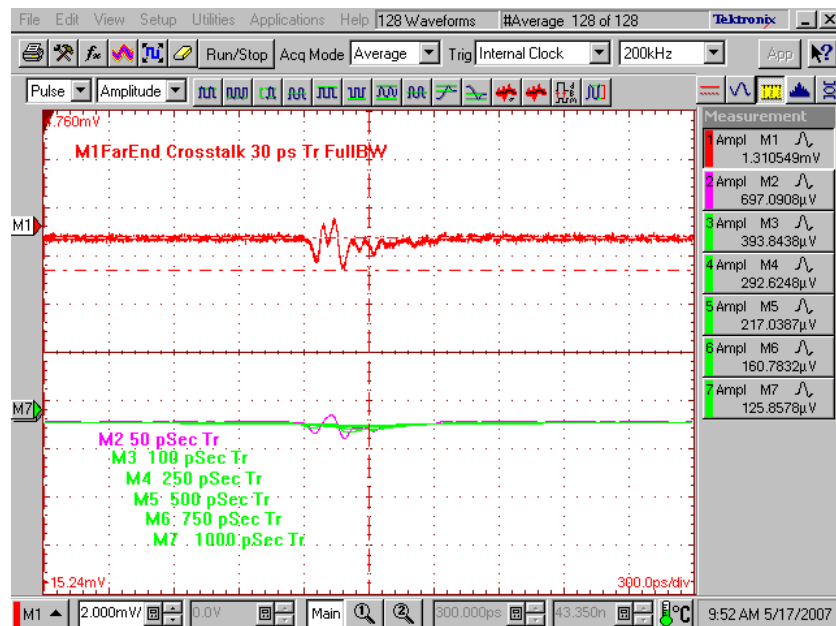
Differential Application – FEXT, “Worst Case” Configuration

Gold on Post, Gold on Tail



Differential Application – FEXT, “Worst Case” Configuration

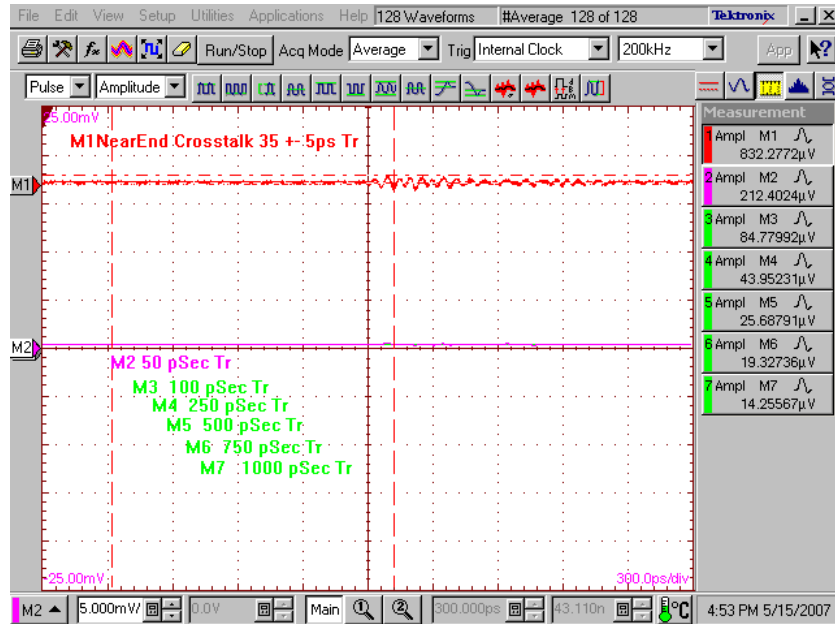
Gold on Post, Tin on Tail



Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height
Description: Contact Plating Effects on Signal Integrity

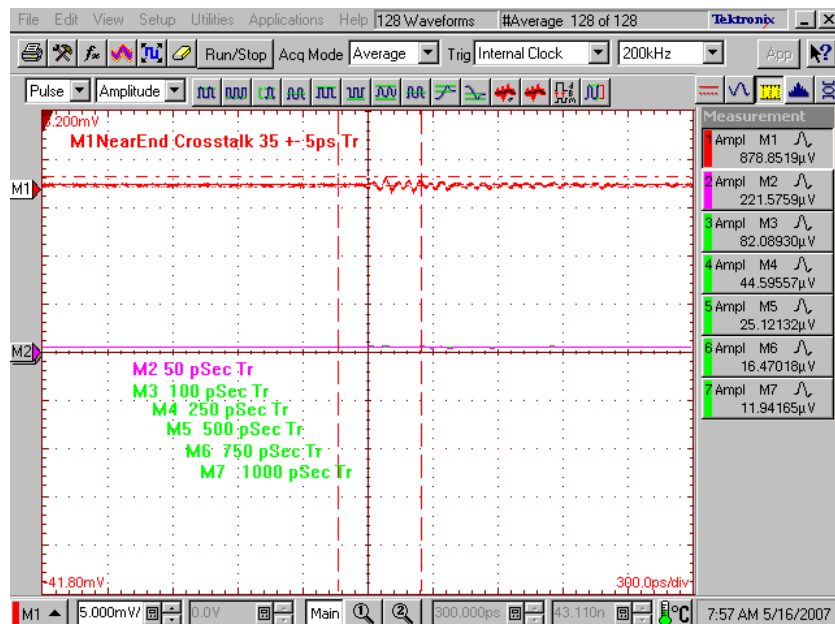
Differential Application – NEXT, “Across Row” Configuration

Gold on Post, Gold on Tail



Differential Application – NEXT, “Across Row” Configuration

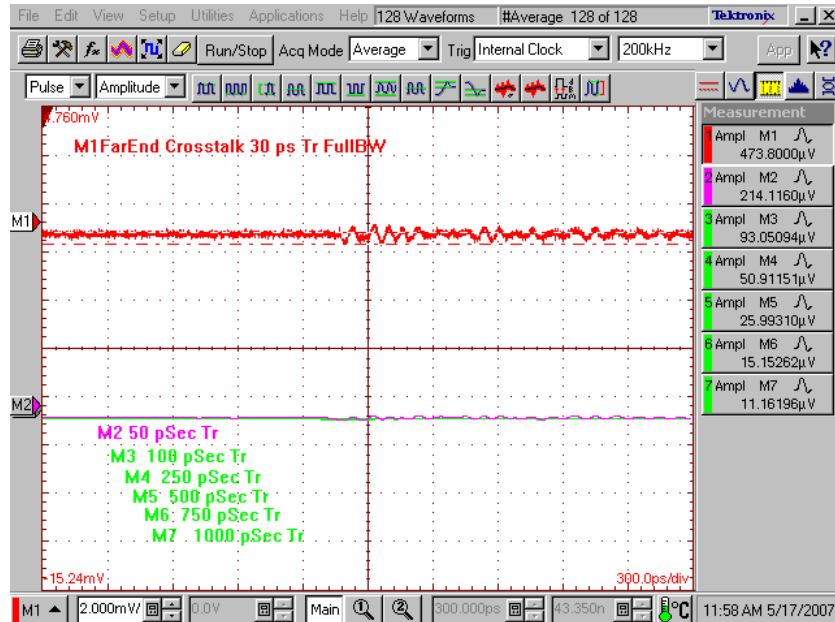
Gold on Post, Tin on Tail



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Description: Contact Plating Effects on Signal Integrity

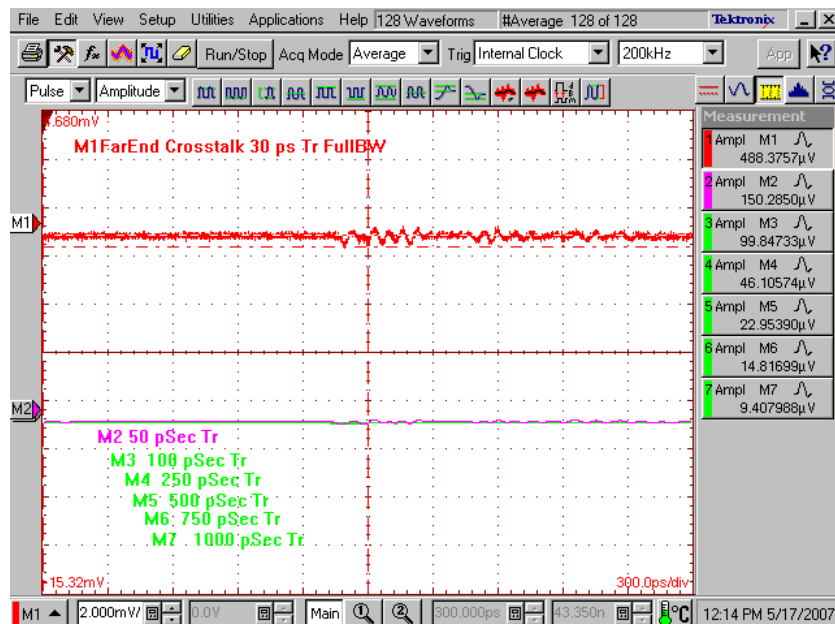
Differential Application – FEXT, “Across Row” Configuration

Gold on Post, Gold on Tail



Differential Application – FEXT, “Across Row” Configuration

Gold on Post, Tin on Tail



Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Appendix C – Product and Test System Descriptions

Product Description

Product samples are the 5mm (0.197") stack height Q Pair High Speed QSE series socket P/N QSE-020-01-L-D-DP-A and QTE series header P/N QTE-020-01-L-D-DP-A. The latter Q Pair connector part numbers are the subject for this report. The one bank and two bank connectors nearest the edges of the PCB fixture are the standard Samtec QXX series. Standard connector series' are characterized in separate reports.

Test System Description

The Test fixtures are composed of a 4-layer FR-4 material with 50Ω and 100Ω signal trace and pad configurations designed for the electrical characterization of Samtec hi-speed connector products. The pictured fixtures are specific to the QSE/QTE series connector and are identified by Samtec P/N PCB-100233-TST-01 and P/N PCB-100233-TST-02 (Figure 1).

Mated PCB Test Fixture with Mounted Test Connectors

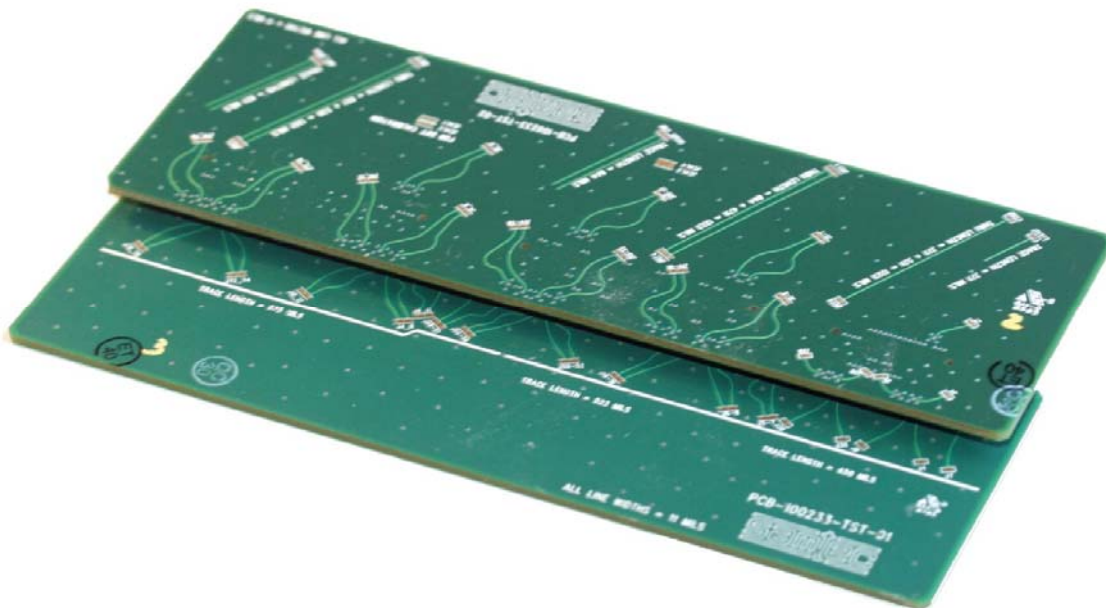


Figure 1

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Two mated sets of PCB-100233-TST type fixtures were populated with their respective QSE & QTE connector part number. One mated set consists of socket and terminal contacts plated with gold on the post and gold on the tail. The second mated set had contacts plated with gold on the post and matte tin on the tail (Figure 2). The dynamic is to observe any change in electrical characteristics due to the plating processes.

Plating Schemes for Socket & Terminal Contacts

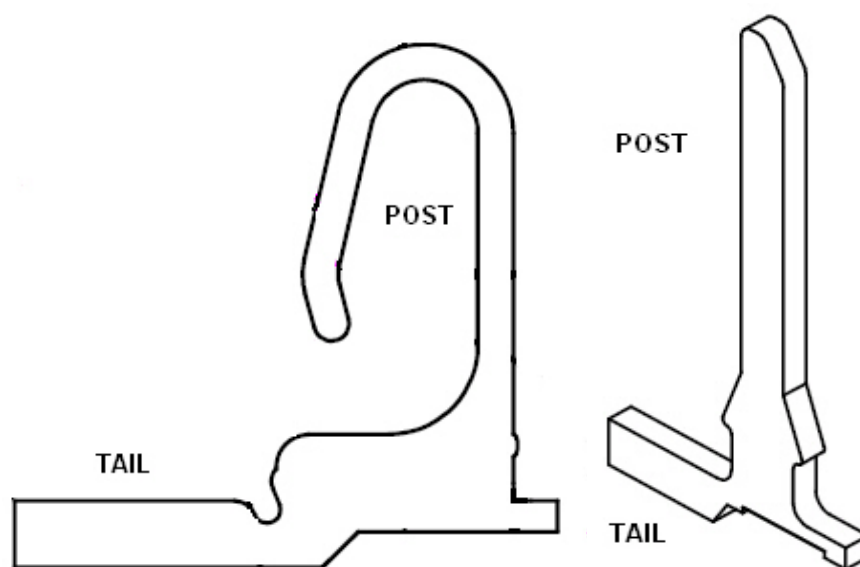


Figure 2

Differential Characterization Map

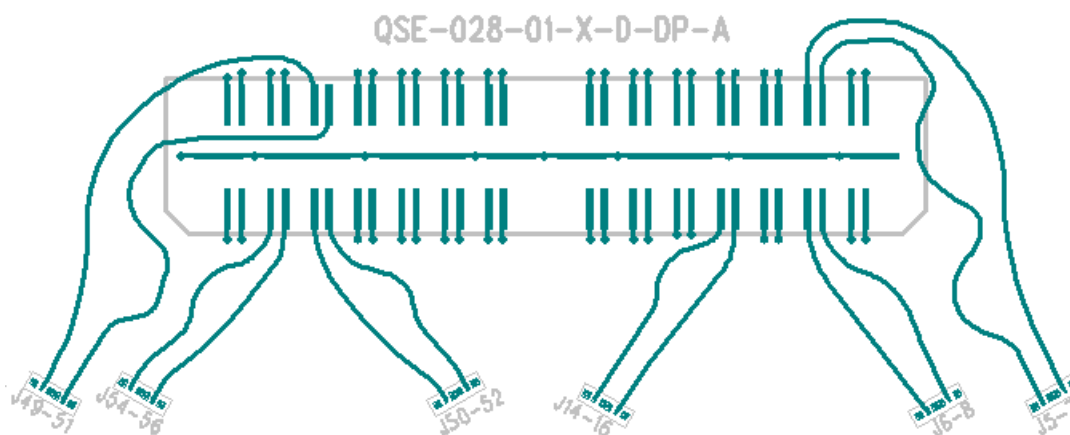


Figure 3

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Waveform Reference & Calibration IConnect Standards

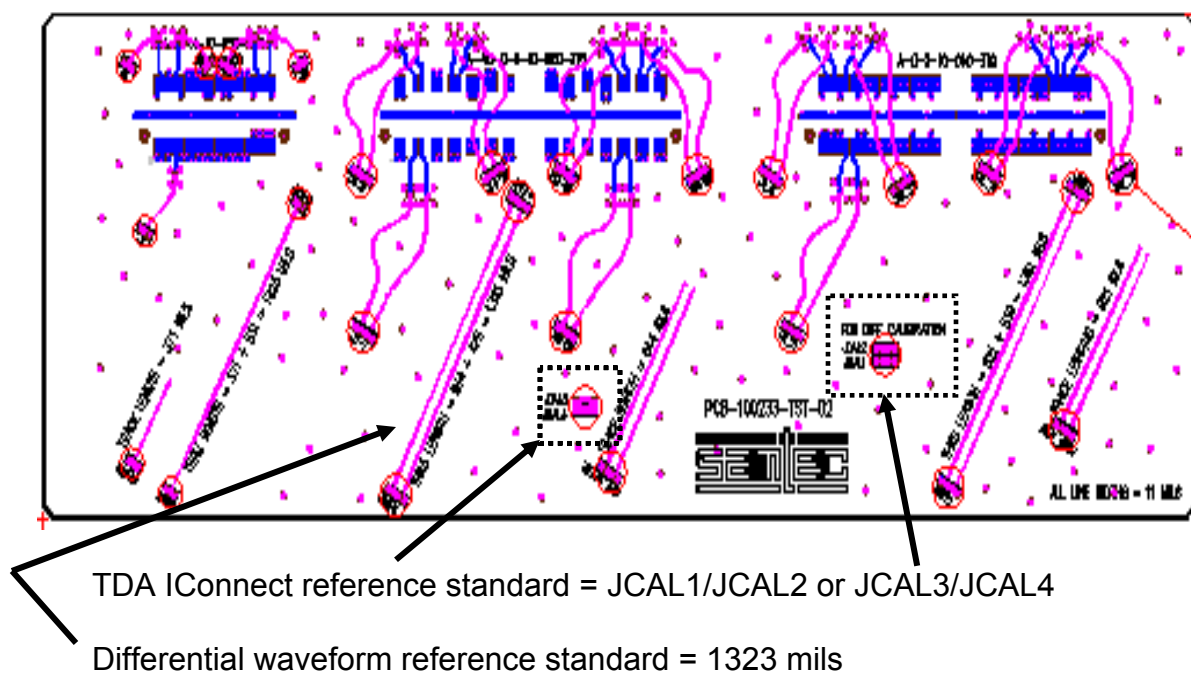


Figure 4

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Appendix D – Test and Measurement Setup

Test instruments are a Tektronix CSA8000 Communication Signal Analyzer Mainframe and the Agilent 8720ES Vector Network Analyzer. Four bays of the CSA8000 are occupied with three Tektronix 80E04 TDR/Sampling Heads and one Tektronix 80E03 Sampling Head. For this series of tests, four of the eight TDR/Sampling Head capability is used (*Figure 5*). The 8720ES serves as a supporting test instrument for verification or troubleshooting results obtained from the TDA Systems IConnect Software package. IConnect is a TDR based measurement software tool used in generating frequency domain related responses from high speed interconnects.

The probe stations illuminated video microscopy system, microprobe positioners, and 40GHz capable probes provide both the mechanical properties and electrical characteristics for obtaining the precise signal launch and calibrations that are critical in obtaining accurate high speed measurements. The 450 micron pitch probes are located to PCB launch points with 25X to 175X magnification and XYZ fine positioning adjustments available from both the probe table and micro-probe positioners. Electrically the microwave probes rate a < 1.0 dB insertion loss, a < 18 dB return loss, and an isolation of 38 dB to 40 GHz (*Figure 6*). Test cables and interconnect adapters are high quality and insure high-bandwidth and low parasitic measurements.

Microprobe Probe Station Capability



Figure 5

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

High Performance 40 GHz Microprobes

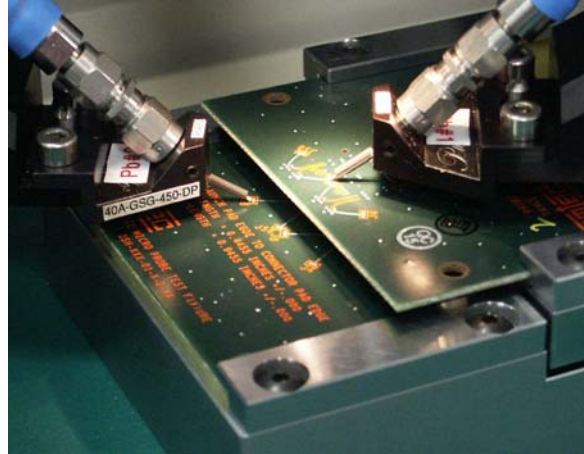


Figure 6

Test Instruments

<u>QTY</u>	<u>Description</u>
1	Tektronix CSA8000 Communication Signal Analyzer
2	Tektronix 80E04 Dual Channel 20 GHz TDR Sampling Module
1	Agilent 8720ES Vector Network Analyzer, 50 MHz to 20 GHz

Measurement Station Accessories

<u>QTY</u>	<u>Description</u>
1	GigaTest Labs Model (GTL3030) Probe Station
4	GTL Micro-Probe Positioners
2	Picoprobe by GGB Ind. Model 40A GSG (single ended applications)
2	Picoprobe by GGB Ind. Dual Model 40A GSG-GSG (differential applications)
1	Keyence VH-5910 High Resolution Video Microscope
1	Keyence VH-W100 Fixed Magnification Lens 100 X
1	Keyence VH-Z25 Standard Zoom Lens 25X-175X

Test Cables & Adapters

<u>QTY</u>	<u>Description</u>
4	Pasternack Re-shapable Semi -Rigid Assembly - 9" 2.9mm (M) to 2.9mm (M)z (IL = .33 dB@ 10 GHz)
2	Huber-Suhner Cable Assembly 36" SMA Female to SMA Female 26.5 GHz (IL = .34 dB @ 10 GHz)

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Appendix E - Frequency and Time Domain Measurements

It is important to note before gathering measurement data that TDA Systems IConnect measurements and CSA8000 measurements are virtually the same measurements with diverse formats. This means that the operator can obtain SI time and frequency characteristics in a simultaneous fashion.

Since IConnect setup procedures are specific to the frequency information sought, it is mandatory that the sample preparation and CSA8000 functional setups be consistent throughout the waveform gathering process. If the operators test equipment permits recall sequencing between the various test parameter setups, it insures IConnect functional setups remain consistent with the TDR/TDT waveforms previously recorded. Related time and frequency test parameter data recorded for this report are gathered simultaneously. [Single-Ended](#) & [Differential](#) characterization maps are provided for identifying the various test points.

Frequency (S-Parameter) Domain Procedures

Frequency data extraction involves two steps that first measure the frequency related time domain waveform followed by post-processing of the time domain waveforms into loss and crosstalk response parameters versus frequency. The first step utilizes the Tektronix CSA8000 time based instrument to capture frequency related single-ended or differential signal types propagating through an appropriately prepared SUT. The second step involves a correlation of the time based waveforms using the TDA Systems IConnect software tool to post-process these waveforms into frequency response parameters. TDA Systems labels these frequency related waveform relationships as the [Step and DUT](#) reference. This report establishes the setup procedures for defining the *Step* and *DUT* reference for frequency parameters of interest. Once established, the *Step* and *DUT* references are post-processed in IConnect's S-parameter computations window.

CSA8000 Setup

Listed below are the CSA 8000 functional menu setups used for single-ended and differential frequency response extractions. Both signal types utilize I-Connect software tools to generate S-parameter upper and lower frequency boundaries along with the step frequency. These frequency boundaries are determined by a time domain instruments functional settings such as window length, number of points and averaging capability. Once window length, number of points and averaging functions are set, maintain the same instrument settings throughout the extraction process.

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

	<u>Single-Ended Signal</u>	<u>Differential Signal</u>
Vertical Scale:	100 mV/ Div:	100 mV/ Div:
Offset:	Default / Scroll	Default / Scroll
Horizontal Scale:	1nSec/ Div = 20 MHz step frequency	1nSec/ Div = 20 MHz step frequency
Max. Record Length:	4000 = Min. Resolution	4000 = Min. Resolution
Averages:	≥ 128	≥ 128

See Characterization maps for the location of the appropriate calibration standards and test points. It is recommended that adjacent test lines not under test be terminated in 50Ω to GND single-ended or 100Ω across differential signal lines.

TDA IConnect Step Waveform Generation

Create a transmission and reflection step waveform for each signal type utilizing the six pad PCB microprobe standard shown at right. Record the waveforms.

- *Step Wfm#1* - For single-ended (SE) transmission(TDT) complete a microprobe GSG signal path from the source back to receive section of the instrument utilizing three pads of the standard.
- *Step Wfm#2* - For single-ended (SE) reflection(TDR) complete a microprobe GSG signal path from the source to port 1 of the standard. Port 2 of the standard is in an open condition.
- *Step Wfm#3* - For differential (DIFF) transmission(TDT) complete a microprobe GSGGSG signal path from the source back to receive section of the instrument utilizing three pads of the standard. Port 2 of the standard is in an open condition.
- *Step Wfm#4* - For differential (DIFF) reflection(TDR) complete a microprobe GSGGSG signal path from the source to port 1 of the standard. Port 2 of the standard is in an open condition.



Insertion Loss

Test Point(s)	PCB Fixture	Diff	Wfm#
Drive	PCB-100233-01	J54-56	IL3
Receive	PCB-100233-02	J54-56	

DUT Waveforms - Manually insert the appropriate test points of the SUT between probes in place of the transmission standard. Establish the waveform(s) by making an active TDT transmission measurement that includes all cables, adapters, and probes connected in the test systems transmission path.

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

IConnect Post Process – process differential waveforms Step #3 with DUT #IL3 for differential I.L. s-parameter response.

Return Loss

Test Point(s)	PCB Fixture	Diff	Wfm#
Drive	PCB-100233-01	J54-56	RL4
Receive	PCB-100233-02	J54-56	

DUT Waveforms - Manually insert the appropriate R.L. test point of the SUT between probes in place of a transmission standard. Establish the waveform(s) by making an active TDR reflection measurement that includes all cables, adapters, and probes connected in the test systems transmission path. In TDR mode the instrument recognizes quality cables, adapters, and probes as a matched 50Ω single-ended impedance or 100Ω differential impedance. An alternative is to load the far-end of the SUT with an appropriately sized 50Ω or 100Ω impedance chip resistor.

IConnect Post Process - process differential waveforms Step#4 with DUT #RL4 for differential R.L. s-parameter response.

Near-End Crosstalk (NEXT)

PCB Fixture	Configuration	Test Point	Diff	Wfm#
PCB-100233-01	Worst Case	Aggressor	J54-56	N8
PCB-100233-01		Victim	J50-52	
PCB-100233-01	Across Row	Aggressor	J49-51	N10
PCB-100233-01		Victim	J50-52	

DUT Wfm# N8 & N10 - Establish waveforms by driving the indicated aggressor lines while monitoring the associated victim line on the near-end. Record the four waveform responses of the energy coupled onto the victim lines for worst case and across the row (xrow) crosstalk configurations.

IConnect Post-Process - process Step Wfm#4 with DUT #N8 for worst case waveforms and Step Wfm#4 with DUT #N10 for across the row differential conditions.

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Far-End Crosstalk (FEXT)

PCB Fixture	Configuration	Test Point	Diff	Wfm#
PCB-100233-01	Worst Case	Aggressor	J54-56	F8
PCB-100233-02		Victim	J50-52	
PCB-100233-01	Across Row	Aggressor	J49-51	F10
PCB-100233-02		Victim	J50-52	

DUT Wfm# F5 thru F10 - Establish waveforms by driving the indicated aggressor lines while monitoring the associated victim line on the far-end. Record the four waveform responses of the energy coupled onto the victim lines for worst case and across the row (xrow) crosstalk configurations.

IConnect Post Process - process differential waveforms Step Wfm#3 with DUT #F8 for worst case waveforms and Step Wfm#3 with DUT#F10 for across the row differential conditions.

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Time Domain Procedures

Measurements involving digital type pulses are performed utilizing either Time Domain Reflectometer (TDR) or Time Domain Transmission (TDT) methods. For this series of tests, TDR methods are employed for the impedance and propagation delay measurements. Crosstalk measurements utilize TDT methods. The Tektronix 80E04 TDR/ Sampling Head provide both the signaling type and sampling capability necessary to accurately and fully characterize the SUT.

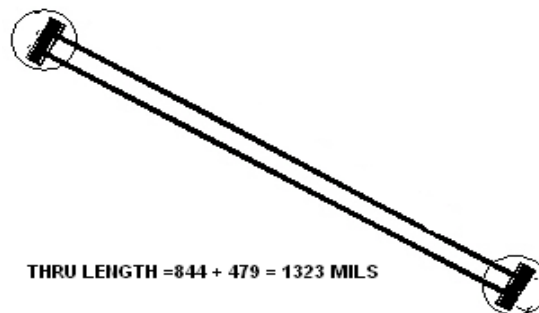
Impedance

Test Point(s)	PCB Fixture	Diff	Wfm#
Drive	PCB-100233-01	J54-56	Z4
Receive	PCB-100233-02	J54-56	

The signal line(s) of the SUT's signal configuration is energized with a TDR pulse. Impedance mismatches occurring in the resultant waveform should be those of the SUT. Test cable, adapters, and probes leading to and from the instrument should appear as fairly flat 50Ω single-ended matched impedance or 100Ω differential matched impedance transmission lines.

Propagation Delay

Test Point(s)	PCB Fixture	Diff	Wfm#
Drive	PCB-100233-01	J54-56	PD4
Receive	PCB-100233-02	J54-56	



The fastest risetime (35±5 ps) available at the SUT is used to measure propagation delay. Both the single-ended and differential signal type propagation delay is pre-referenced using the reference lines lengths pictured below. These referenced signal

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

lines represent the total line lengths running to and from the mated connector. This effectively allows isolation of the mated connector propagation delay by making additional measurements on the designated signal lines of mated PCB fixtures. Fifty percent points of the referenced amplitudes are measured and the time between these points is the propagation delay of a mated connector series.

Crosstalk (NEXT)

PCB Fixture	Configuration	Test Point	Diff	Wfm#
PCB-100233-01	Worst Case	Aggressor	J54-56	N8
PCB-100233-01		Victim	J50-52	
PCB-100233-01	Across Row	Aggressor	J49-51	N10
PCB-100233-01		Victim	J50-52	

Crosstalk (FEXT)

PCB Fixture	Configuration	Test Point	Diff	Wfm#
PCB-100233-01	Worst Case	Aggressor	J54-56	F8
PCB-100233-02		Victim	J50-52	
PCB-100233-01	Across Row	Aggressor	J49-51	F10
PCB-100233-02		Victim	J50-52	

An active TDR waveform is transmitted through a selected SUT signal line. The adjacent quiet signal line is monitored for the coupled energy at the near-end and far-end. This procedure is followed for the configurations listed in the tables above. Active and quiet lines not being monitored are terminated in the test systems characteristic impedance. Signal lines adjacent to the quiet lines remain terminated on both ends throughout the test sequence. Failing to terminate the active near or far end, quiet lines, or in some cases, signal lines adjacent to the quiet line may have an effect on amplitude and shape of the coupled energy.

Series: QSE-DP/QTE-DP, Parallel Board-to-Board, 0.8mm Pitch, 5mm (0.197") Stack Height

Description: Contact Plating Effects on Signal Integrity

Appendix F – Glossary of Terms

BC – Best Case crosstalk configuration

DP – Differential Pair signal configuration

DUT – Device under test; TDA IConnect reference waveform

FEXT – Far-End Crosstalk

GSG – Ground–Signal–Ground; geometric configuration

NEXT – Near-End Crosstalk

PCB – Printed Circuit Board

SE – Single-Ended

SI – Signal Integrity

SUT – System under test

TDR – Time Domain Reflectometry

TDI – Time Domain Transmission

WC – Worse Case crosstalk configuration

Xrow^{se} – Cross ground/ power bar crosstalk, single-ended signal

Xrow^{diff} – Cross ground/ power bar crosstalk, differential signal

Z – Impedance (expressed in ohms)