



Application Note

QPairs® QTE/QSE-DP Multi-connector Stack Designs In PCI Express Applications 16 mm Connector Stack Height

REVISION DATE: OCTOBER 13, 2004

Copyrights and Trademarks
Copyright © 2004 Samtec, Inc.

Developed in conjunction with
Teraspeed Consulting Group LLC

COPYRIGHTS, TRADEMARKS, and PATENTS

QPairs® and Final Inch® are trademarks of Samtec, Inc. Other product names used herein are trademarks of their respective owners. All information and material in this publication are property of Samtec, Inc. All related rights are reserved. Samtec, Inc. does not authorize customers to make copies of the content for any use.

Terms of Use

Use of this publication is limited to viewing the pages for evaluation or purchase. No permission is granted to the user to copy, print, distribute, transmit, display in public, or modify the contents of this document in any way.

Disclaimer

The information in this publication may change without notice. All materials published here are “As Is” and without implied or expressed warranties. Samtec, Inc. does not warrant this publication will be without error, or that defects will be corrected. Samtec, Inc. makes every effort to present our customers an excellent and useful publication, but we do not warrant or represent the use of the materials here in terms of their accuracy, reliability or otherwise. Therefore, you agree that all access and use of this publication's content is at your own risk.

NEITHER SAMTEC, INC. NOR ANY PARTY INVOLVED IN CREATING, PRODUCING, OR DELIVERING THIS PUBLICATION SHALL BE LIABLE FOR ANY DIRECT, INCIDENTAL, CONSEQUENTIAL, INDIRECT, OR PUNITIVE DAMAGES ARISING OUT OF YOUR ACCESS, USE OR INABILITY TO ACCESS OR USE THIS PUBLICATION, OR ANY ERRORS OR OMISSIONS IN ITS CONTENT.

Abstract

PCI Express is primarily intended as a high performance serial interface targeted for use in desktop, mobile, workstation, server, communications platforms, and embedded devices. As with any modern high speed PCB design, the performance of an actual PCI Express interconnect is highly dependent on the implementation. This paper describes a stacked multi-board system that emulates a real PCI Express board arrangement with various board-to-board loopback trace lengths. This stacked system takes advantage of proven Samtec Final Inch® designs and this industry standard to help engineers deploy systems of two or more PCB cards and Samtec's family of high speed electrical connectors. To demonstrate the feasibility of using Samtec QPairs® QTE/QSE-DP connectors with standard FR4 epoxy PCBs, measured differential insertion loss and simulated compliance eye information will be presented.

Introduction

Samtec has developed a full line of connector products that are designed to support serial speeds up to and greater than 2.5 Gbps, the “Baud rate” of each PCI Express differential data lane. Working with Teraspeed Consulting, they have developed a complete breakout and routing solution for each member of Samtec’s line of high speed connectors, called Final Inch®

To demonstrate the feasibility of using Samtec QPairs® QTE/QSE-DP connectors in PCI Express stacked board applications with standard FR4 epoxy PCBs, a test rig was developed comprised of the Final Inch® test board set for the QTE/QSE-DP connectors and one or more PCI Express “Spring Boards”, which are PCI form factor boards with differential traces of various lengths that loop back to the connector. Informative interconnect loss and eye compliance information will be presented.

Definitions

Interconnect Budget – The amount of loss and jitter that is allowed in the interconnect and still meet the target specification.

Insertion Loss – The differential voltage swing attenuation from transmitter to receiver on the trace. The trace is subject to resistive, dielectric, and skin effect loss. Insertion Loss increases as trace length and and/or signal frequency increases. Vias and connectors also exhibit losses which must be included in the interconnect budget. Total loss allowed in the interconnect is 13.2 dB.

Jitter – The variation in the time between differential crossings from the ideal crossing time. Jitter includes both data dependent and random contributions on the interconnect. Total jitter allowed is 0.3UI, or 120 ps when UI = 400 ps.

PRBS – Pseudo Random Bit Sequence.

T_j – Total jitter, which is the convolution of the probability density functions for all the jitter sources, Random jitter (R_j) and Deterministic jitter (D_j). The UI allocation is given as the allowable T_j. The PCI Express specification does not specify allocation of R_j and D_j.

UI – Unit Interval. The time interval required for transmission of one data symbol. For a binary lane operating at 2.5 Gbps, the UI is 400 ps.

V_{DIFF} – Differential voltage, defined as the difference of the positive conductor voltage and the negative conductor voltage (V_{D+} - V_{D-}).

V_{DIFFp-p} – Differential peak-to-peak voltage, defined by the following equations:

$$V_{DIFFp-p} = (2 * \max | V_{D+} - V_{D-} |) \text{ (Applies to a symmetric differential swing)}$$

$$V_{DIFFp-p} = (\max |V_{D+} - V_{D-}| \{ V_{D+} > V_{D-} \} + \max |V_{D+} - V_{D-}| \{ V_{D+} < V_{D-} \})$$

(Applies to an asymmetric differential swing)

The PCI Express Specification

PCI Express links are based on recent advances in point-to-point interconnect technology. A PCI Express link is comprised of a dual-simplex communications channel between two components physically consisting of two low-voltage, differential signal pairs. The PCI Express Base Specification defines one half of a link (one transmitter and receiver) an electrical sub-block. The design model used for this paper is of one differential pair (one electrical sub-block) passing through two or more PCBs.

The PCI Express specification is available through the PCI SIG organization (<http://www.pcisig.com>) by becoming a member. Detailed specifications for an electrical sub-block can be found starting in Section 4.3 of the PCI Express Base Specification and will be referred to throughout the rest of this paper. Detailed electrical signal specifications start in Sub-section 4.3.2.

PCI Express Stack Test System

The PCI Express stacked test system is comprised of one or more “spring boards” installed between the two Final Inch® Test PCBs. A side view of the test system with four Spring Boards installed is shown in Figure 1.

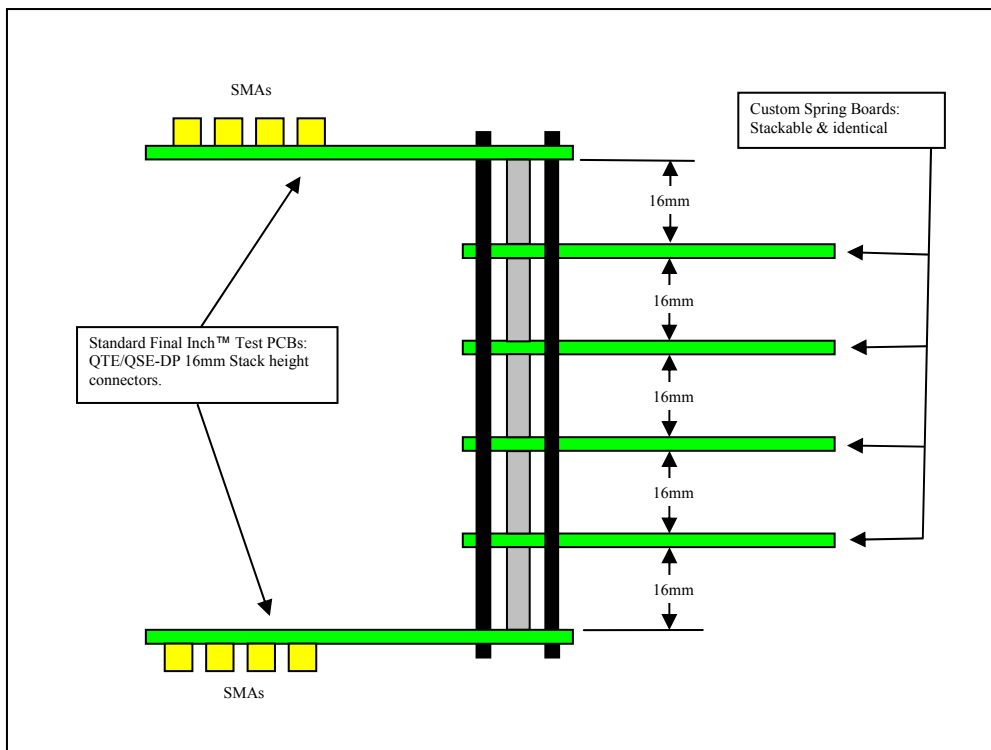


Figure 1 - PCI Express Test Rig, Side View

Illustrations of the spring board are shown in Figures 2 and 3. The top connector pads are tied directly to the bottom connector pads, allowing the PCI Express signals to pass through to the next board. Connectors have been strategically placed to allow use with Samtec's Final Inch® QTE/QSE-DP PCB set. Differential trace loops of various lengths have been routed to simulate the effects of connector-connector separation in real PCI Express multi-board systems.

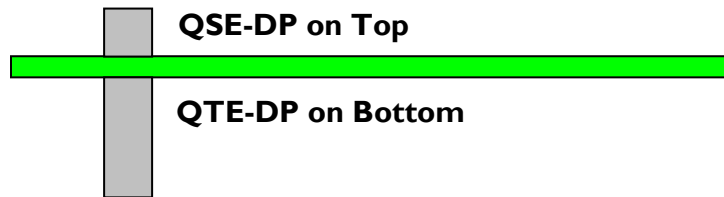


Figure 2 - Spring Board side view

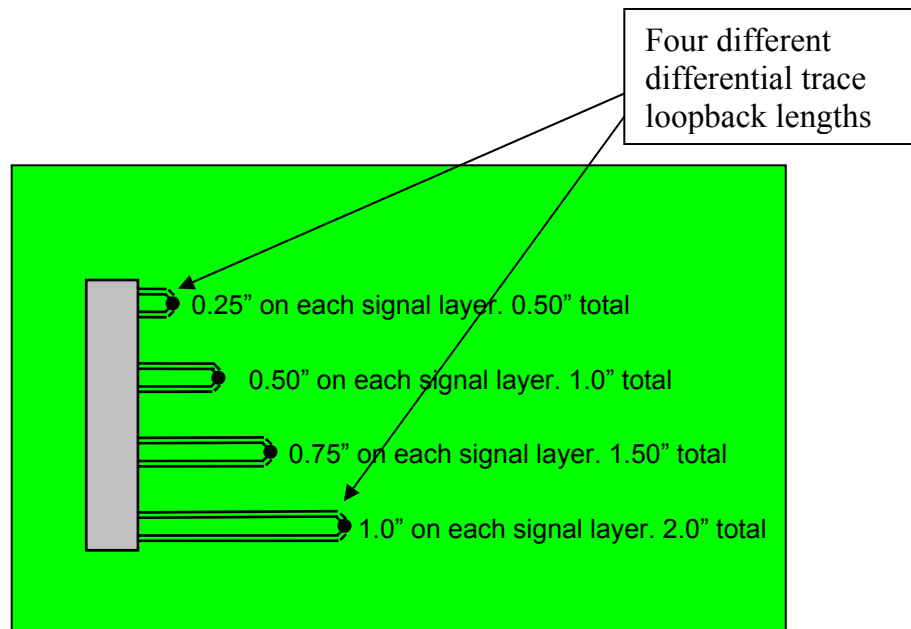


Figure 3 - Spring Board top view

Differential Insertion Loss Measurements

The next four pictures show the results from differential insertion loss measurements taken of real PCI Express test rigs. In each figure, the loopback trace length is held constant and the number of spring boards installed is increased from 1 to 4.

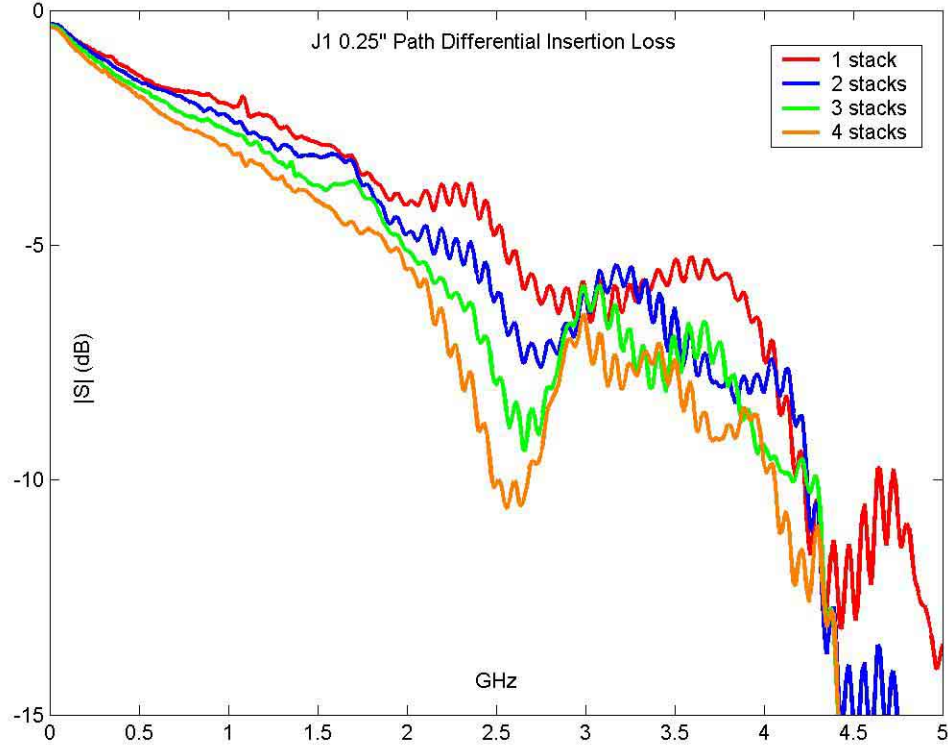


Figure 4 – Differential Insertion loss comparison, 0.25 inch loopback path with various stack combinations

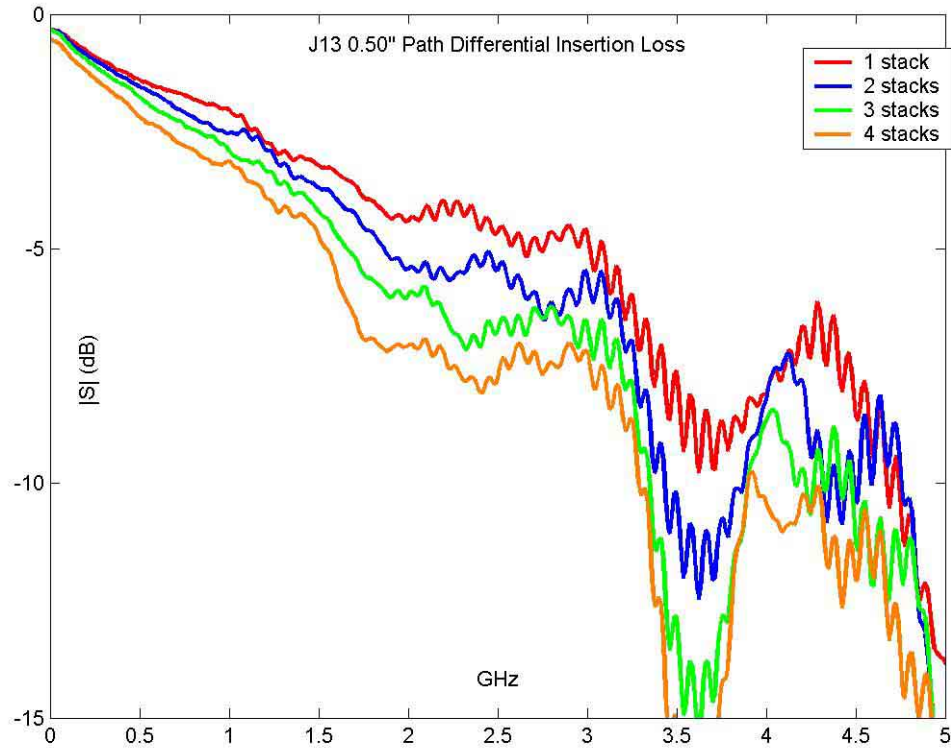


Figure 5 – Differential Insertion loss comparison, 0.50 inch loopback path with various stack combinations

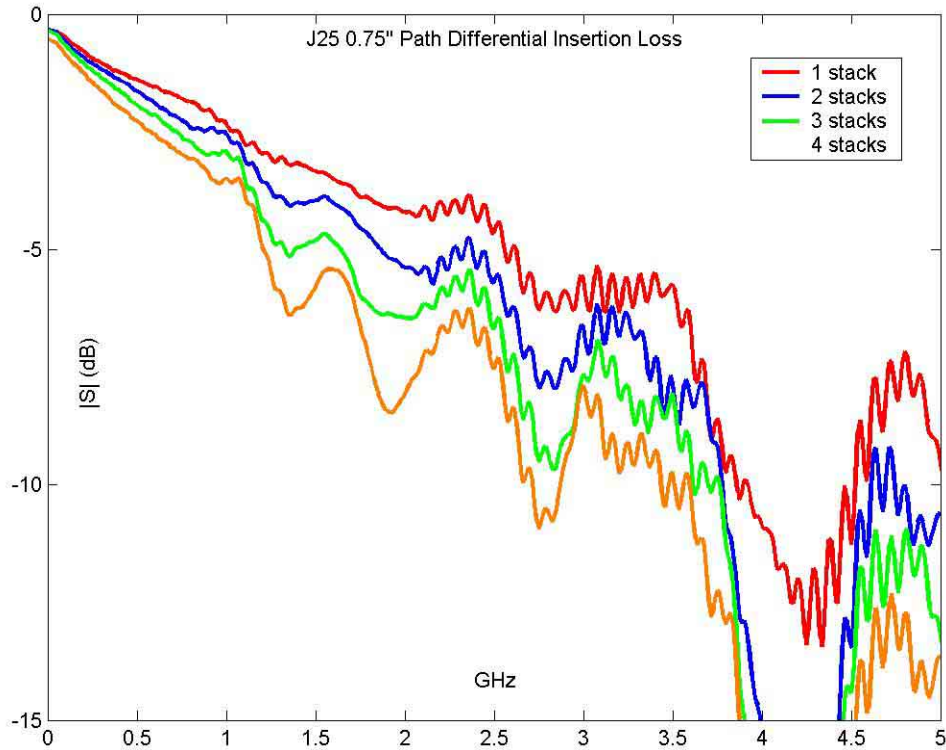


Figure 6 - Differential Insertion loss comparison, 0.75 inch loopback path with various stack combinations

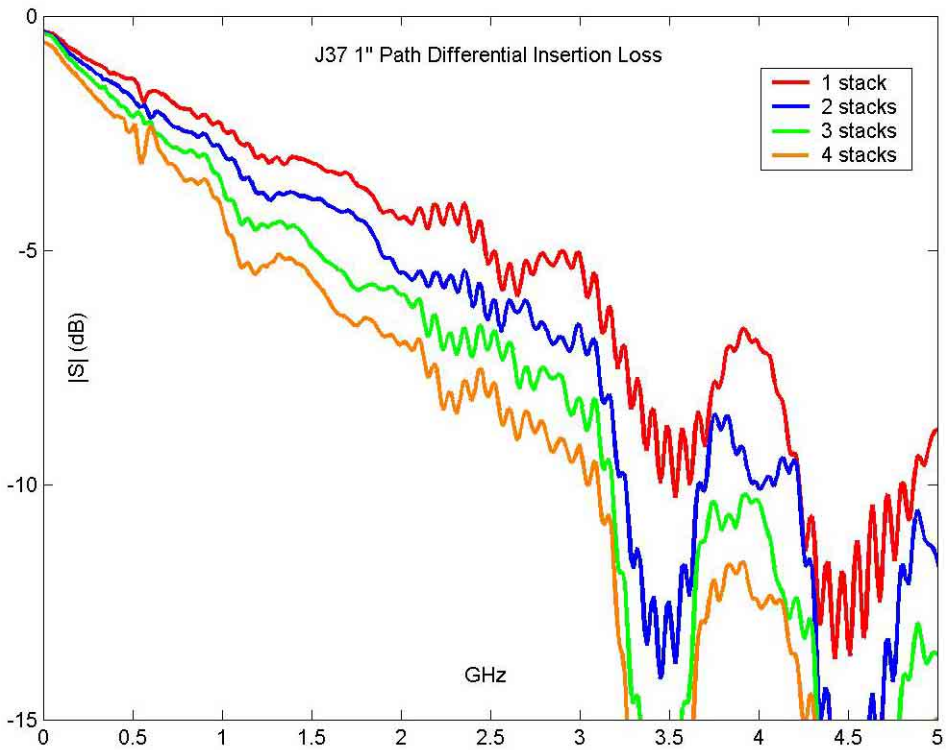


Figure 7 - Differential Insertion loss comparison, 1.00 inch loopback path with various stack combinations

Conclusion

At the Nyquist frequency (1.25 GHz), all four of the loopback path lengths had less differential insertion loss than the -13.2 dB allowed by the PCI Express specification when measured in PCI Express stack test fixtures containing from 1 to 4 Spring Boards. Any dips that may be caused by resonances in the connector that are tuned by the loopback trace lengths stayed above 2 GHz.

Compliance Eye Simulations

Input Stimulus Setup

A PRBS 2⁷-1 pattern was used for stimulus. Xilinx supplies a stimulus generator tool kit within their VirtexII Pro™ design kit giving customers complete control over the amount of jitter in the transmitter's data output. Using the generated stimulus with their RocketIO™ multi-gigabit serial transceiver model the PCI Express specification, enough total jitter was added to the driver output to just meet worst case PCI Express transmit jitter specifications. The slow-slow corner silicon model was used to come as close as possible to the minimum differential V_{DIFFp-p} output specification.

The Test Circuit Model

The test circuit modeled is shown in Figure 1. It consists of the following:

- Xilinx Virtex-II Pro™ serial transceiver model configured as PCI Express driver.
- Xilinx FPGA flip-chip package model.
- AC coupling capacitors, value = 100 nF.
- One of four measurement based spice models of the 4-connector stacked system, one model for each loopback trace path on the Spring Boards.
- 50 Ohm termination resistors to Ground (as required per Note 7 in Section 4.3.4 of the PCI Express Base Specification, Rev 1.0a).

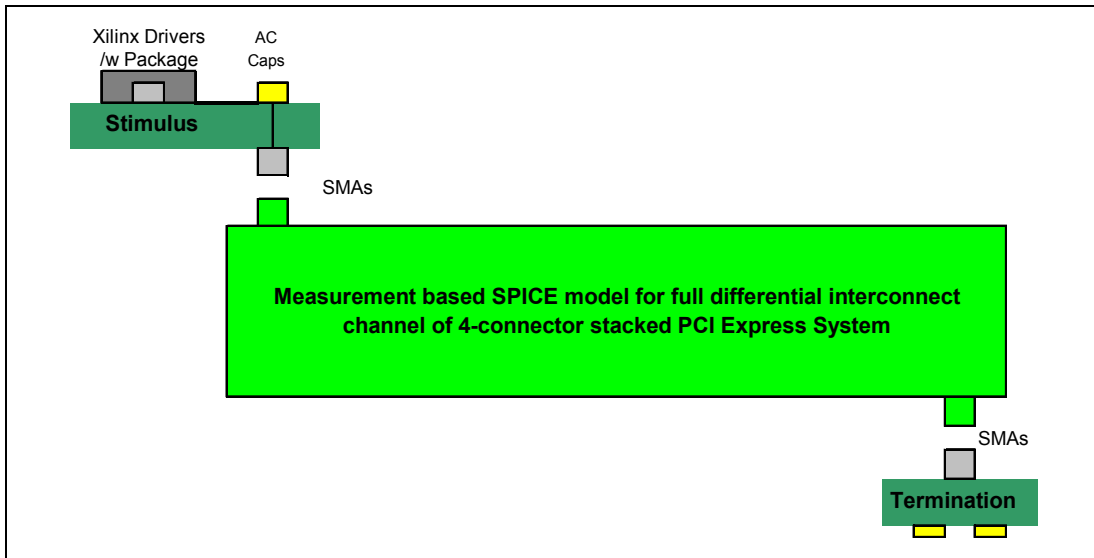


Figure 8— PCI Express Test Circuit

Procedure

Interconnect Budget

The interconnect budget can be best illustrated by the mask shown in Figure 2. In order to pass the PCI Express constraints for loss and jitter, the simulated eye waveform must not touch any location within the grey areas shown. Calculated interconnect budget values are shown in Table 1.

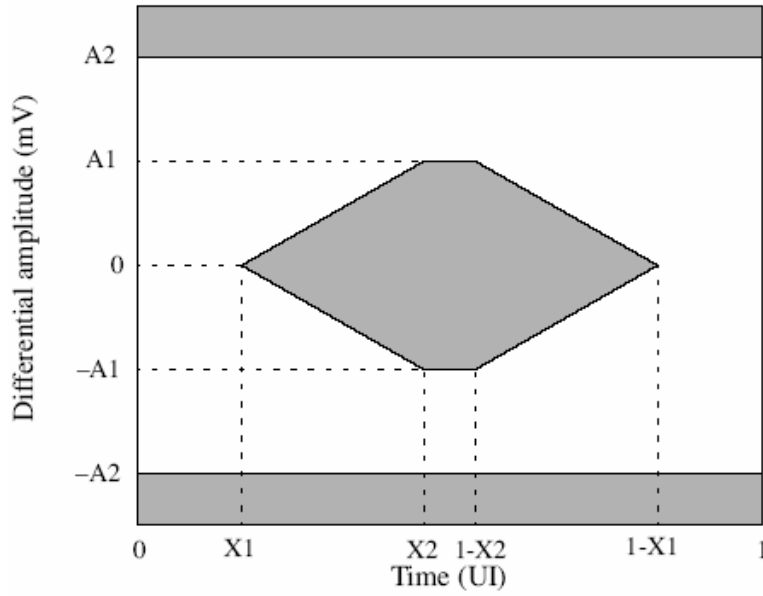


Figure 9 - Example eye mask template

	Maximum Loss, A1 to -A1 (See example mask template) ($V_{DIFFp-p}$)	Minimum Eye Width, X1 to 1-X1 (See example mask template) (UI_{p-p})
Driver at Package Pin	0.800	0.7
Receiver at Package Pin	0.175	0.4
Interconnect budget:	13.2 dB loss ¹	0.3 UI (120ps when UI = 400 ps)

Table 1 - PCI Express interconnect budget max loss and min eye width calculated values

¹The worst case operational loss budget at 1.25 GHz Nyquist frequency is calculated by taking the minimum driver output voltage ($V_{TX-DIFFp-p} = 800$ mV) divided by the minimum input voltage to the receiver ($V_{RX-DIFFp-p} = 175$ mV). $175/800 = .219$, which after conversion results in a maximum loss budget of 13.2 dB.

Driver Compliance

Setup for Tj for UI Measurements

Before the PCI Express circuit model can be simulated and measured, we must first set up the driver stimulus to provide minimum TX eye width (maximum jitter) and minimum amplitude. As mentioned in the previous section, the driver stimulus' jitter can be adjusted until it just reaches the maximum total jitter allowed under the compliance load shown in Figure 4-25 of Section 4.3.3.2 in the PCI Express Base Specification and re-

created in Figure 3 below. The AC coupling capacitor C_{TX} can be set anywhere between 75pF and 200pF. We set C_{TX} to 100nF for all simulations because it is a popular value in the industry. Table 2 shows the resulting output measurements. The eye pattern generated in the PCI Express driver compliance test simulation is shown in Figure 9 below.

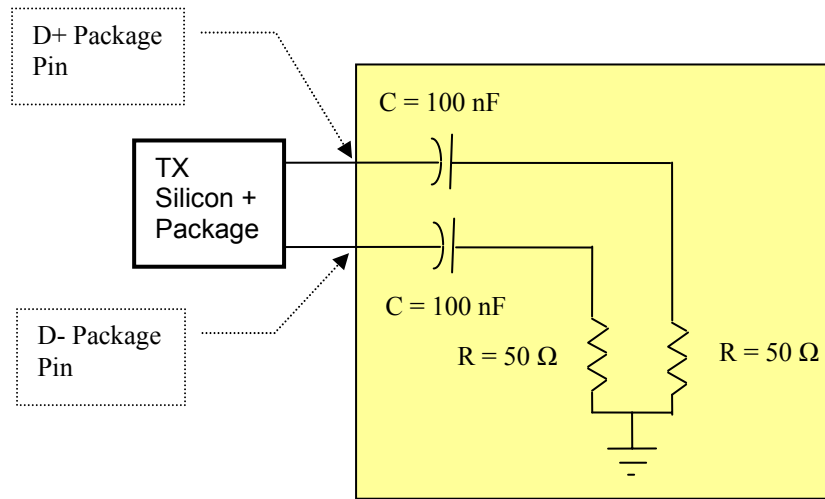


Figure 10 - PCI Express Compliance Test/Measurement load

	Vdiff_{p-p}	Total Jitter
Specification	≥800 mV	≤120 ps
Measured	800.4 mV	120.1 ps ¹

Table 2 - PCI Express TX Silicon + Package Measurements at Package Pin

¹The PCI Express Base Specification defines X2 to 1-X2 = 0. The minimum TX height measurements were taken at mid bit.

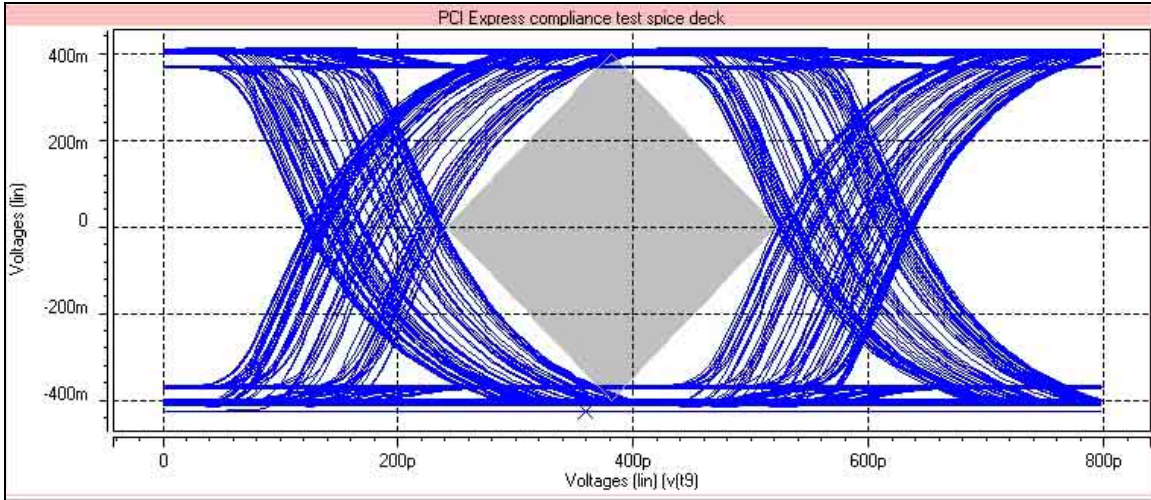


Figure 11 - PCI Express TX Compliance Eye

Receiver Compliance Eye Results

Differential Voltage and Eye Width Measurements at Receiver End

QTH-DP/QSH-DP Connector, 16 mm Stack Height	Max Jitter at UI = 400 ps	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Min RX Differential Voltage, A1 to -A1 ¹ (See example mask template)	Pass/Fail
Specification	≤240 ps	≥160 ps	≥175mV_{DIFFP-p}	-
0.25" loopback	157.2	346.0	436.8	Pass
0.50" loopback	165.4	324.2	347.8	Pass
0.75" loopback	187.0	332.4	305.8	Pass
1.00" loopback	196.0	318.2	249.4	Pass

Table 3 – PCI Express Far-end Measurements, 16 mm stack height connectors

¹The PCI Express Base Specification defines X2 to 1-X2 = 0. The minimum RX height measurements were taken at mid bit.

The following four images show the results of the PCI Express receiver compliance simulations when applied to a stack system with 4 Spring Boards, with the Spring Board loopback trace lengths of 0.25, 0.50, 0.75, and 1.00 inch.

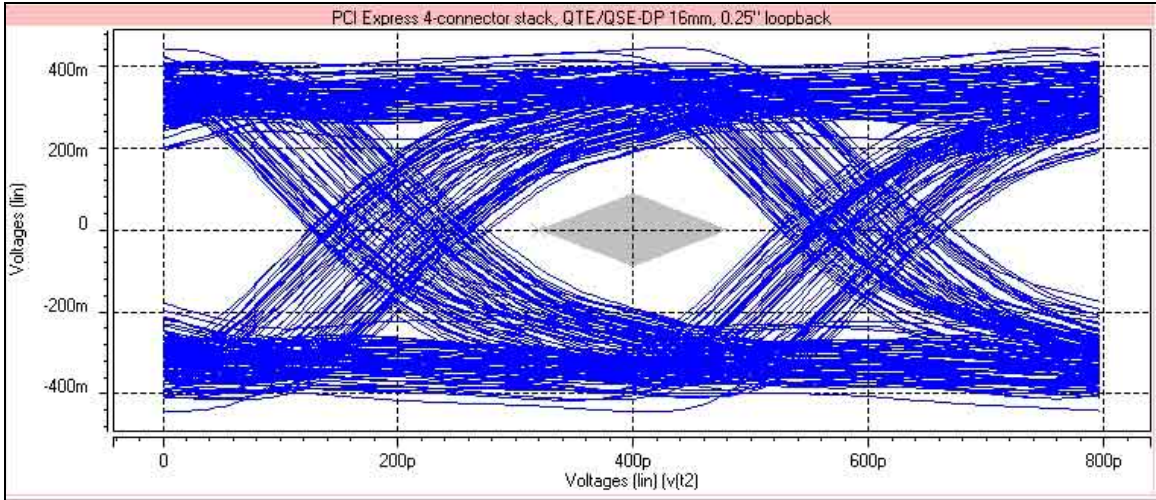


Figure 12 - PCI Express RX compliance eye, 4-connector stack, 0.25 inch loopback path

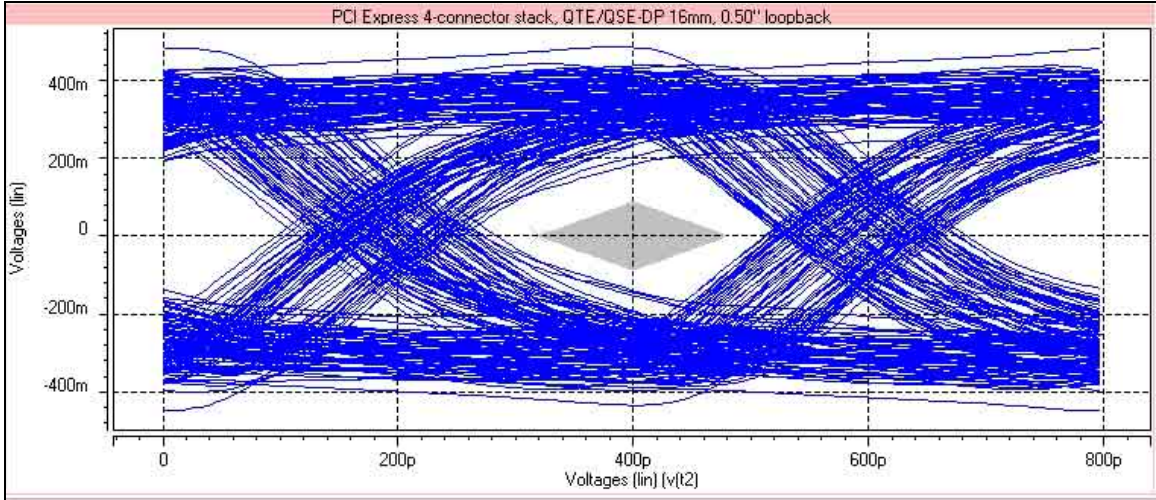


Figure 13 - PCI Express RX compliance eye, 4-connector stack, 0.50 inch loopback path

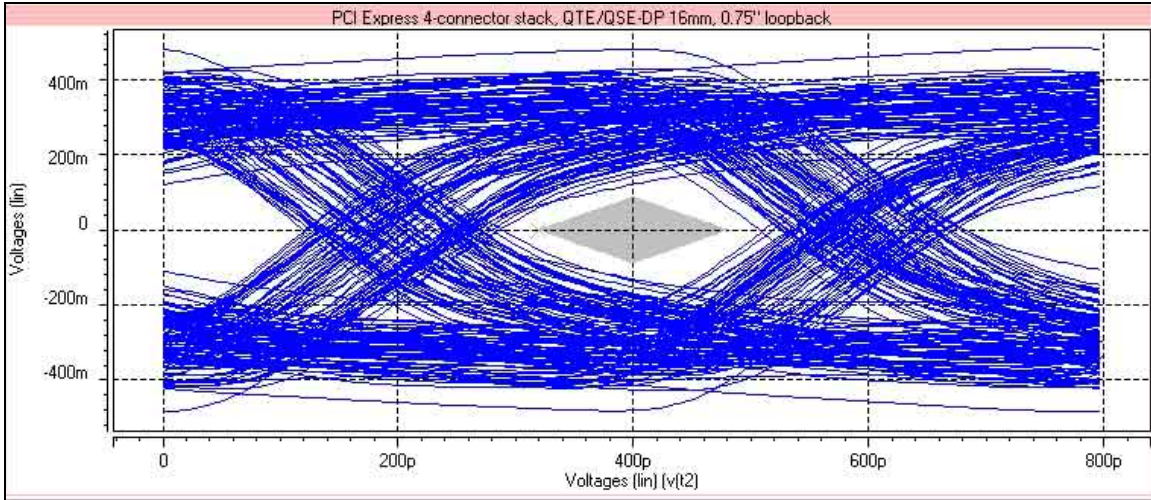


Figure 14 - PCI Express RX compliance eye, 4-connector stack, 0.75 inch loopback path

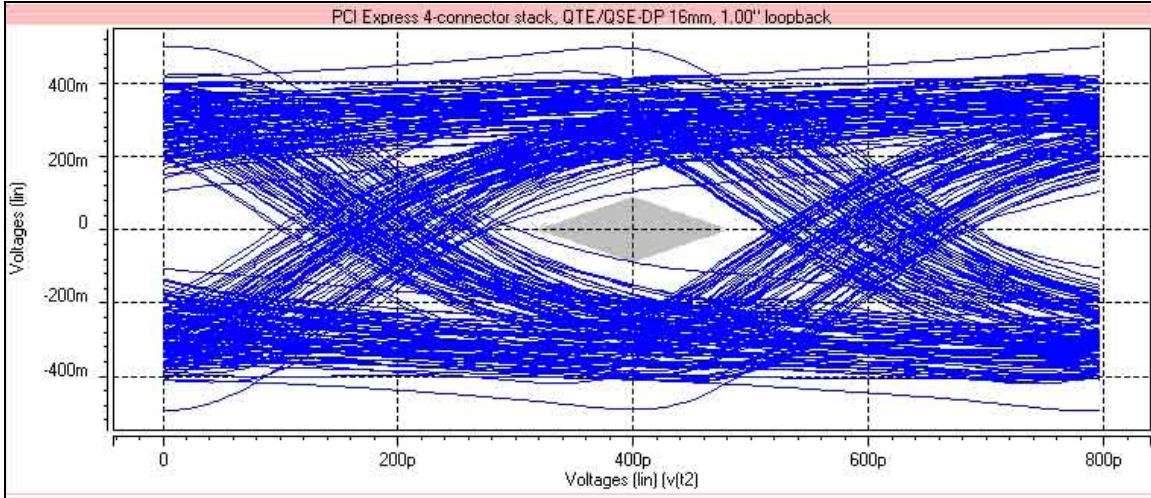


Figure 15 - PCI Express RX compliance eye, 4-connector stack, 1.00 inch loopback path

Conclusions

The receiver compliance eye patterns indicate that Samtec Q Pairs® QTE/QSE-DP 16 mm stack height connectors can be used in the 4-connector stacked configuration shown in Figure 1 for PCI Express systems with total loop back trace lengths up to 2.0 inches when used with Samtec's Final Inch® routing, breakout, and trace width solutions.

Final Conclusion

Using criteria taken directly from the PCI Express specification, and through experimental measurements of the test boards and simulation, we have shown that multiple stacks of QTE/QSE-DP 16 mm connectors will work in PCI Express applications with loopback paths as long as 2.0 inches in total length when used with Samtec's Final Inch™ routing, breakout, and trace width solutions.