Application Note

Q Pairs® QTE/QSE-DP Final Inch™ Designs In PCI Express Applications 16 mm Stack Height

Developed in conjunction with
Teraspeed Consulting Group LLC

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Abstract

The PCI Express is primarily intended as a high performance serial interface targeted for use in desktop, mobile, workstation, server, communications platforms, and embedded devices. As with any modern high speed PCB design, the performance of an actual PCI Express interconnect is highly dependent on the implementation. This paper describes a measurement method applied to proven Samtec Final Inch™ designs and this industry standard to help engineers deploy systems of two PCB cards mated through Samtec's family of high speed electrical connectors. To demonstrate the feasibility of using Samtec Q Pairs® QTE/QSE-DP connectors with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in spreadsheet format. Also, trace lengths on each side of the QTE/QSE-DP connector will be gradually increased to show the limits of compliance.

In order to ensure interoperability between PCI Express transmitter and receiver devices, we will stress a typical interconnect design by stimulating their Spice model components and devices with stressed data patterns. This paper will cover techniques to stress the system with reduced driver amplitude as well as jitter and noise injection.

Introduction

Samtec has developed a full line of connector products that are designed to support serial speeds up to and greater than 2.5 Gbps, the "Baud rate" of each PCI Express data lane. Working with Teraspeed Consulting, they have developed a complete breakout and routing solution for each member of Samtec's line of high speed connectors, called Final Inch™. To demonstrate the feasibility of using Samtec Q Pairs® QTE/QSE-DP connectors in PCI Express applications with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in a user-friendly spreadsheet format. Trace lengths will be varied to show the limits of compliance.

Analysis will consist of stimulating a typical trace-connector-trace circuit path with a worst case signal and then observing the corresponding eye closure related to reflections due to impedance discontinuities, loss, and stubs. Next, utility software will be used to extract, analyze, and format Spice-measured voltage amplitudes and differential signal crossing times. Mask violations (see Figure 2) will be recorded in pass/fail format.

Definitions

Interconnect Budget – The amount of loss and jitter that is allowed in the interconnect and still meet the target specification.

Loss – The differential voltage swing attenuation from transmitter to receiver on the trace. The trace is subject to resistive, dielectric, and skin effect loss. Loss increases as trace length and and/or signal frequency increases. Vias and connectors also exhibit losses which must be included in the interconnect budget. Total loss allowed in the interconnect is 13.2 dB.

Jitter – The variation in the time between differential crossings from the ideal crossing time. Jitter includes both data dependent and random contributions on the interconnect. Total jitter allowed is 0.3UI, or 120 ps when UI = 400 ps.

PRBS – Pseudo Random Bit Sequence

Tj – Total jitter, which is the convolution of the probability density functions for all the jitter sources, Random jitter (Rj) and Deterministic jitter (Dj). The UI allocation is given as the allowable Tj. The PCI Express specification does not specify allocation of Rj and Dj.

UI – Unit Interval. The time interval required for transmission of one data symbol. For a binary lane operating at 2.5 Gbps, the UI is 400 ps.

V_{DIFF} – Differential voltage, defined as the difference of the positive conductor voltage and the negative conductor voltage (V_{D+} - V_{D-}).

$V_{DIFFp-p}$ – Differential peak-to-peak voltage, defined by the following equations:

$V_{DIFFp-p}$ = (2*max | V_{D+} - V_{D-} |) (Applies to a symmetric differential swing)
$V_{DIFFp-p}$ = (max | V_{D+} - V_{D-} | { V_{D+} > V_{D-}} + max | V_{D+} - V_{D-} | { V_{D+} < V_{D-}})
(Applies to a asymmetric differential swing)

The PCI Express Specification

PCI Express links are based on recent advances in point-to-point interconnect technology. A PCI Express link is comprised of a dual-simplex communications channel between two components physically consisting of two low-voltage, differential signal pairs. The PCI Express Base Specification defines one half of a link (one transmitter and receiver) an electrical sub-block. The design model used for this paper is of three electrical sub-blocks operating in tandem, the victim surrounded by 2 aggressors, with all bit streams heading in the same direction.

Detailed specifications for an electrical sub-block can be found starting in Section 4.3 of the PCI Express Base Specification and will be referred to throughout the rest of this paper. Detailed electrical signal specifications start in Sub-section 4.3.2. Measurement techniques specified in this section have been rigidly adhered to including the requirement for finding the median within the jitter for use in jitter measurements. See Note 8 of Table 4-6 in the PCI Express Base Specification for more details.

Setup and Measurement

Input Stimulus Setup

A PRBS 2^7-1 pattern was used for victim stimulus and a repeating 1010… pattern used for the aggressor differential pairs on each side of the victim differential pair. Xilinx supplies a stimulus generator tool kit within their VirtexII Pro™ design kit giving customers complete control over the amount of jitter in the transmitter's data output. Using their stimulus system with their RocketIO™ multi-gigabit serial transceiver model, enough total jitter was added to the driver output to just meet worst case PCI Express transmit jitter specifications. The slow-slow corner silicon model was used to come as close as possible to the minimum differential $V_{DIFFp-p}$ output specification.

The Test Circuit Model

The test circuit modeled is shown in Figure 1. It consists of the following:

- One set of three of Xilinx Virtex-II Pro™ serial transceiver models configured as PCI Express drivers.
- Xilinx FPGA flip-chip package model
- One set of six AC coupling capacitors, value = 100 nF
- 1 Samtec Q Pairs® QTE/QSE-DP Final Inch™ design, comprised of the QTE-014-04-L-D-A-DP/QSE-014-01-L-D-A-DP 16 mm stack height connector models surrounded by Samtec's BOR models, lossy trace models and SMA connector models on both sides of the connector.
- 50 Ohm termination resistors to Ground (as required per Note 7 in Section 4.3.4 of the PCI Express Base Specification, Rev 1.0a.

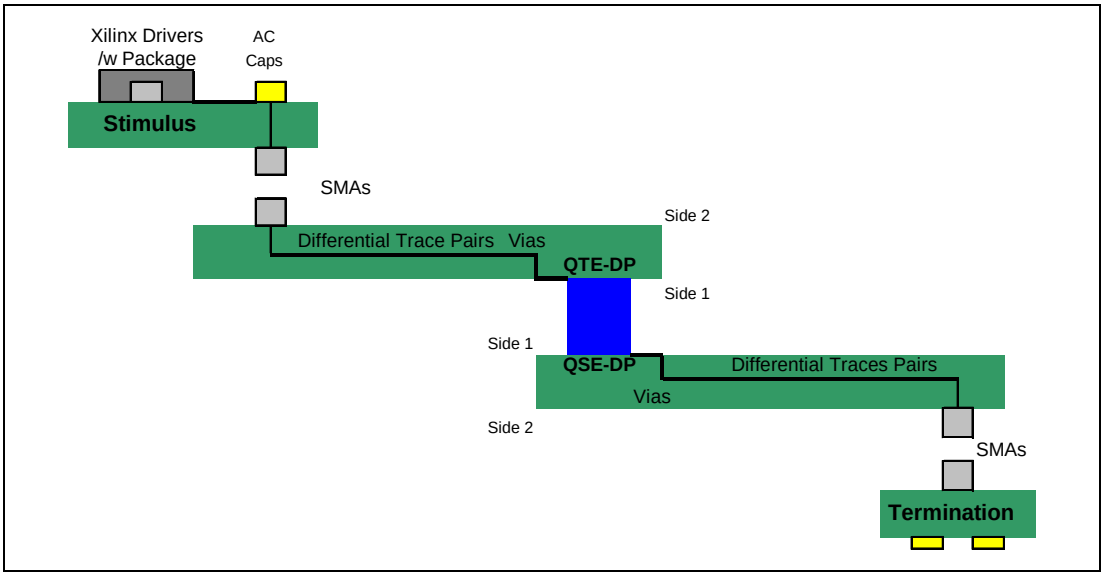


Figure 1 PCI Express Test Circuit

Procedure

Interconnect Budget

The interconnect budget can be best illustrated by the mask shown in Figure 2. In order to pass the PCI Express constraints for loss and jitter, the simulated eye waveform must not touch any location within the grey areas shown. Calculated interconnect budget values are shown in Table 1.

Figure 2—Example eye mask template

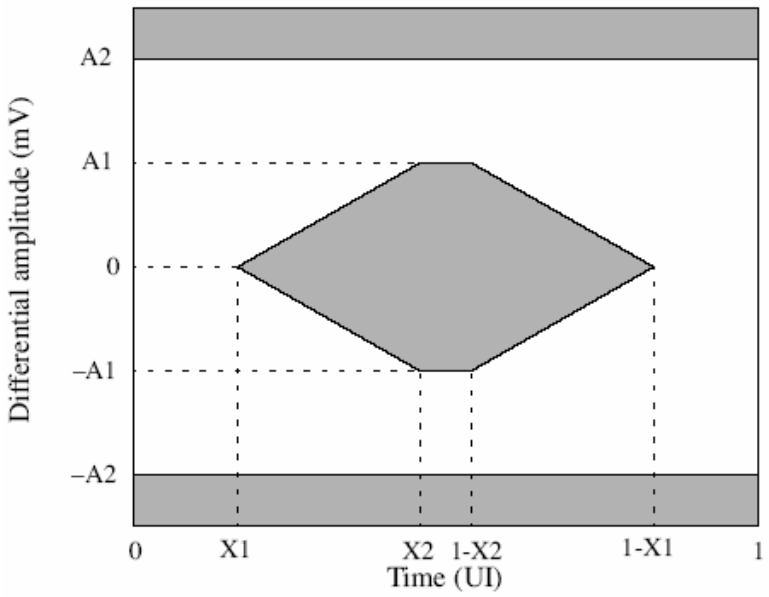


Table 1—PCI Express interconnect budget max loss and min eye width calculated values

	Maximum Loss, A1 to –A1 (See example mask template) ($V_{DIFFp-p}$)	Minimum Eye Width, X1 to 1-X1 (See example mask template) (UI_{p-p})
Driver at Package Pin	0.800	0.7
Receiver at Package Pin	0.175	0.4
Interconnect budget:	13.2 dB loss[1]	0.3 UI (120ps when UI = 400 ps)

[1]The worst case operational loss budget at 1.25 GHz Nyquist frequency is calculated by taking the minimum driver output voltage ($V_{TX-DIFFp-p}$ = 800 mV) divided by the minimum input voltage to the receiver ($V_{RX-DIFFp-p}$ = 175 mV). 175/800 = .219, which after conversion results in a maximum loss budget of 13.2 dB.

Transmitter Compliance Measurements

Setup for Tj for UI Measurements

Before the PCI Express circuit model can be simulated and measured, we must first set up the driver stimulus to provide minimum TX eye width (maximum jitter) and minimum amplitude. As mentioned in the previous section, the driver stimulus' jitter can be adjusted until it just reaches the maximum total jitter allowed by the PCI Express specification, under the compliance load shown in Figure 4-25 of Section 4.3.3.2 in the PCI Express Base Specification and re-created in Figure 2 below. The AC coupling capacitor C_{TX} can be set anywhere between 75pF and 200pF. We set C_{TX} to 100nF for all

simulations because it is a popular value in the industry. Table 2 shows the resulting output measurements. The eye pattern generated in the PCI Express driver compliance test simulation can be found in Appendix A, Picture 1, of this paper.

Figure 3 – PCI Express Compliance Test/Measurement load

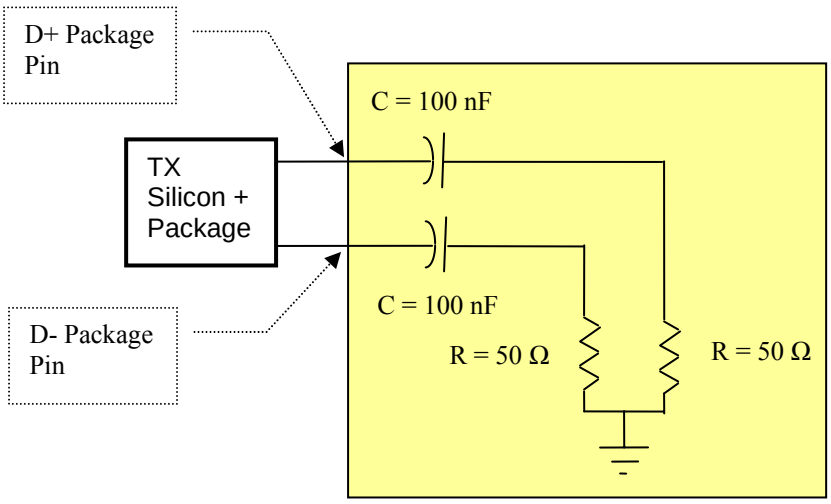


Table 2 – PCI Express TX Silicon + Package Measurements at Package Pin

	$Vdiff_{p-p}$	Total Jitter
Specification	≥800 mV	≤120 ps
Measured	968.4 mV	120 ps

Since the driver output is 168.4 mV above the minimum $V_{DIFFp-p}$ specification under compliance/measurement loading, the minimum differential voltage allowed when the full PCI Express circuit model is simulated and measured must be adjusted upward. The added voltage value will be based on the ratio of near-end to far-end minimum $V_{DIFFp-p.}$

$$V_{DIFFp-pRX}\ \text{correction} = 168.4 \times (175/800) = 36.8\ \text{mV}_{DIFFp-p}$$

Full Circuit Compliance Measurements

Differential Voltage and Eye Width Measurements at Receiver End

QTE-DP/QSE-DP Connector, 16 mm Stack Height	Max Jitter at UI = 400 ps	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Min RX Differential Voltage, A1 to –A1[1] (See example mask template)	Pass/Fail
Specification	**<240 ps**	**>160 ps**	**>211.8mV$_{DIFFp-p}$[2]**	-
10" total trace[3]	141.1	374.0	593.7	Pass
20" total trace	163.8	363.5	517.6	Pass
30" total trace	176.6	344.0	441.3	Pass
40" total trace	182.1	331.3	364.4	Pass
50" total trace	195.1	300.3	226.5	Pass
51" total trace	192.3	295.1	202.4	Fail
52" total trace	201.1	295.6	195.3	Fail

Table 3 – PCI Express Far-end Measurements, 16 mm stack height connector

[1]X2 to 1-X2, the mid bit sample time, is .1UI (40 ps when UI = 400 ps).

[2]36.8 mV$_{DIFFp-p}$ has been added to RX minimum V$_{DIFFp-p}$ specification of 175 mV$_{DIFFp-p}$ to account for the difference in the Xilinx TX driver/package output, which is 168.4 mV$_{DIFFp-p}$ above the PCI Express minimum V$_{TX-DIFFp-p}$ specification. See Table 2 in this document and Table 4-5 in the PCI Express Base Specification.

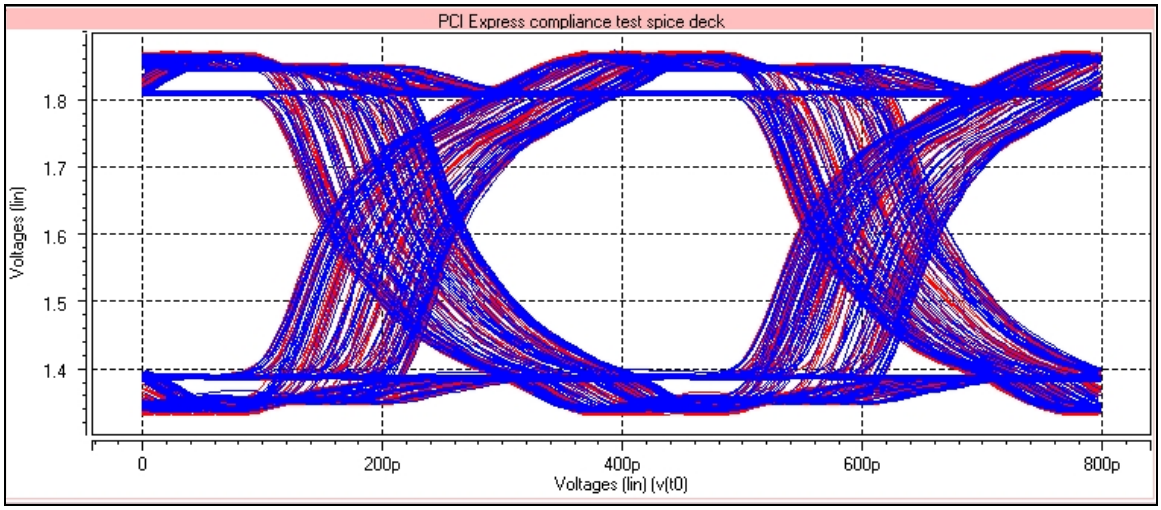
[3]The total trace length specified is the sum of the two differential trace lengths in the QTE-DP/QSE-DP test fixture model, as shown in Figure 1. These traces were always kept equal in length in each simulation.

The eye pattern generated in the PCI Express circuit simulation with 50 inches total trace length can be found in Appendix A, Picture 2, of this paper.

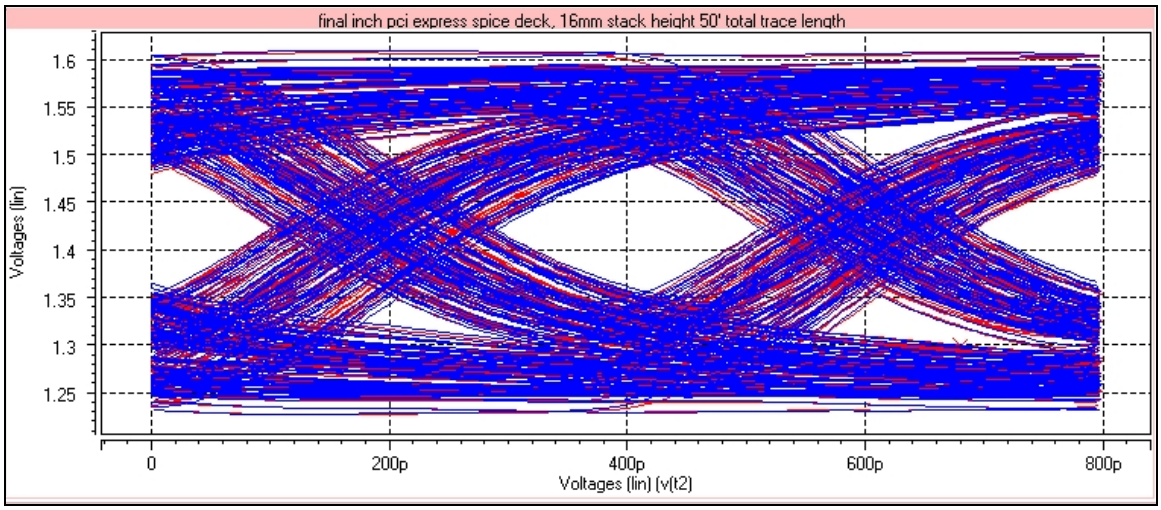
Conclusions

A single Samtec Q Pairs® QTE/QSE-DP 16 mm stack height connector in a board-to-board configuration can be used in PCI Express systems with total trace lengths not to exceed 50 inches when used with Samtec's Final Inch™ routing, breakout, and trace width solutions. Because loss is the dominant contributor to system degradation, designers should be aware that using smaller trace widths, laminates with higher loss tangent, and sub optimal routing solutions with higher pair-to-pair coupling and additional via stubs will decrease overall performance and the maximum allowable trace length. It is advisable, when designing systems that approach the maximum trace length limits, to perform detailed modeling, simulation, and measurement of the target design including the effects of material properties, traces, vias, and additional components.

Appendix A – Waveform images



Picture 1 – Worst case stimulus eye waveform, probed at Xilinx driver package pins, connected to compliance test/measurement load



Picture 2 – PCI Express circuit eye waveform, probed at terminator pins, 50 inches total trace length