Application Note

Q Pairs® QTH-DP/QSH-DP Final Inch™ Designs In XAUI Applications 5mm Stack Height

Developed in conjunction with
Teraspeed Consulting Group LLC

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Abstract

The 10 Gigabit Attachment Unit Interface (XAUI) is primarily intended as a point-to-point interface of up to approximately 50 cm (19.685 inches) between integrated circuits using controlled impedance traces on low-cost printed circuit boards (PCBs). As with any modern high speed PCB design, the performance of an actual XAUI interconnect is highly dependent on the implementation. This paper describes a measurement method applied to proven Samtec Final Inch™ designs and this industry standard to help engineers deploy systems of two PCB cards mated through Samtec's family of high speed electrical connectors. To demonstrate the feasibility of using Samtec Q Pairs® QTH/QSH-DP connectors with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in spreadsheet format. Also, trace lengths on each side of the QTH/QSH-DP connector will be gradually increased to show the limits of compliance.

In order to ensure interoperability between XAUI transmitter and receiver devices, we will stress a typical interconnect design by stimulating their Spice model components and devices with stressed data patterns. This paper will cover techniques to stress the system with reduced driver amplitude as well as jitter injection.

Introduction

Samtec has developed a full line of connector products that are designed to support serial speeds up to and greater than 3.125 Gb/ps, the "Baud rate" of each XAUI data lane. Working with Teraspeed Consulting, they have developed a complete breakout and routing solution for each member of Samtec's line of high speed connectors, called Final Inch™. To demonstrate the feasibility of using Samtec Q Pairs® QTH/QSH-DP connectors in XAUI applications with standard FR4 epoxy PCBs, informative interconnect loss and jitter values will be measured through Spice simulation and presented in a user-friendly spreadsheet format. Trace lengths will be varied to show the limits of compliance.

Analysis will consist of stimulating a typical trace-connector-trace circuit path with a worst case signal and then observing the corresponding eye closure related to reflections due to impedance discontinuities, loss, and stubs. Next, utility software will be used to extract, analyze, and format Spice-measured voltage amplitudes and differential signal crossing times. Mask violations (see Figure 2) will be recorded in pass/fail format.

Definitions

Interconnect Budget – The amount of loss and jitter that is allowed in the interconnect and still meet the target specification.

Loss – The differential voltage swing attenuation from transmitter to receiver on the trace. The trace is subject to resistive, dielectric, and skin effect loss. Loss increases as trace length and and/or signal frequency increases. Vias and connectors also exhibit

losses which must be included in the interconnect budget. Total loss allowed in the XAUI interconnect is -12.0dB.

Jitter – The variation in the time between differential crossings from the ideal crossing time. Jitter includes both data dependent and random contributions on the interconnect. Total jitter allowed in the XAUI interconnect is +/-0.275UI, or +/-88 ps when UI = 320 ps.

PRBS – Pseudo Random Bit Sequence.

Tj – Total jitter, which is the convolution of the probability density functions for all the jitter sources, Random jitter (Rj) and Deterministic jitter (Dj). The UI allocation is given as the allowable Tj.

UI – Unit Interval. The time interval required for transmission of one data symbol. For a binary lane operating at 3.125 Gbps, the UI is 320 ps.

$\mathbf{V_{DIFF}}$ – Differential voltage, defined as the difference of the positive conductor voltage and the negative conductor voltage (V_{D+} - V_{D-}).

The XAUI Specification

XAUI links are based on recent advances in point-to-point interconnect technology. A XAUI lane is comprised of a dual-simplex communications channel between two components physically consisting of two low-voltage, differential signal pairs. Four of these lanes are used to convey 32-bit self-clocking data and control, each at a nominal rate of 3.125 GBaud resulting in a 10 Gb/ps effective data rate.

The XAUI specification uses the name "byte stream" to describe one half of a data lane. The design model used for this paper is of three byte streams operating in tandem, one the victim surrounded by 2 aggressors, with all bit streams heading in the same direction and passing through the connector on adjacent pin pairs.

Detailed specifications for the XAUI electrical sub-block can be found starting in Section 47 of IEEE 802.3ae™ Specification. Relevant timing and voltage constraints from this section of the specification will be referred to throughout the rest of this paper.

Setup and Measurement

Input Stimulus Setup

A PRBS 2^7-1 pattern was used for victim stimulus and a repeating 1010… pattern used for the aggressor differential pairs on each side of the victim differential pair. Xilinx supplies a stimulus generator tool kit within their VirtexII Pro™ design kit giving customers complete control over the amount of jitter in the transmitter's data output. Using their stimulus system with their RocketIO™ multi-gigabit serial transceiver model, enough total jitter was added to the driver output to just meet worst case XAUI transmit

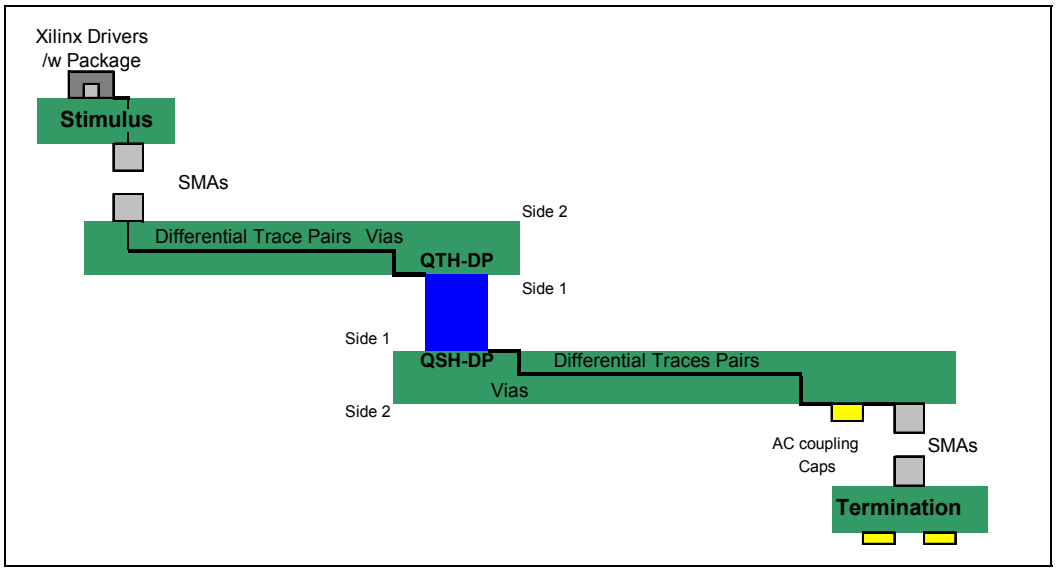
jitter specifications. The slow-slow corner silicon model was used to come as close as possible to the minimum differential V_{DIFF} output specification.

The Test Circuit Model

The test circuit modeled is shown in Figure 1. It consists of the following:

- One set of three of Xilinx Virtex-II Pro™ serial transceiver models configured as XAUI drivers.
- Xilinx FPGA flip-chip package model.
- 1 Samtec Q Pairs® QTH/QSH-DP Final Inch™ design, comprised of the QTH-014-01-L-D-DP-A/QSH-014-01-L-D-DP-A 5mm stack height connector models surrounded by the Samtec's BOR models, lossy trace models, and SMA connector models on both sides of the connector.
- One set of six AC coupling capacitors, value = 100 nF.
- 100 Ohm termination resistors.

Figure 1 - XAUI Test Circuit



Procedure

Interconnect Budget

The interconnect budget can be best illustrated by the mask shown in Figure 2. In order to pass the XAUI constraints for loss and jitter, the simulated eye waveform must not touch any location within the grey areas shown. Calculated interconnect budget values are shown in Table 1.

Figure 2—Example mask template

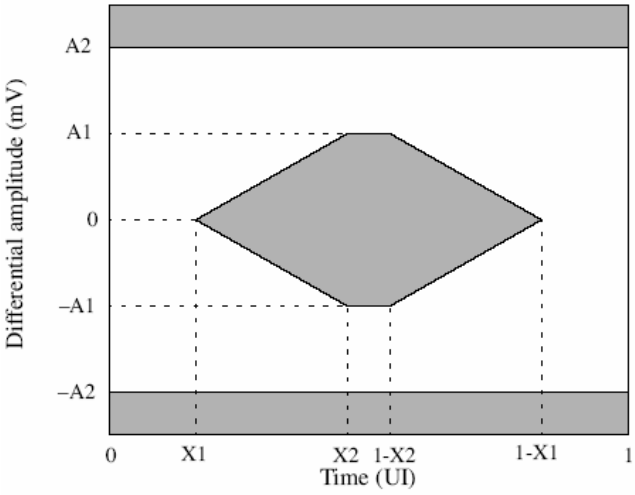


Table 1—Driver template intervals at 3.125 Gb/ps

Symbol	Near-end value	Far-end value	Units
X1	+/-56	+/-88	psec
X2	124.8	128	psec
A1	400	100	mV
A2	800	800	mV

Table 2—XAUI interconnect budget max loss and min eye width calculated values

	Maximum Loss, A1 to –A1 (See example mask template) ($V_{DIFFp-p}$)	Minimum Eye Width, X1 to 1-X1 (See example mask template) (UI_{p-p})
Driver at Package Pin	0.400	0.65
Receiver at Package Pin	0.100	0.45
Interconnect budget:	12.04 dB loss[1]	0.2 UI_{p-p} (64ps when UI=320 ps)

[1]The worst case operational loss budget at 1.5625 GHz Nyquist frequency is calculated by taking the minimum driver output voltage ($V_{TX-DIFF}$ = 400 mV) divided by the minimum input voltage to the receiver ($V_{RX-DIFF}$ = 100 mV). 100/400 = .25, which after conversion results in a maximum loss budget of 12.04 dB.

Transmitter Compliance Measurements

Setup for Tj for UI Measurements

As mentioned in the previous section, the driver stimulus' jitter was adjusted until the transmitter exhibited the maximum total jitter allowed by the XAUI specification at the driver package pins under the compliance load shown in Figure 3 below. The XAUI specification does not specify the range of capacitor values allowed for the AC coupling capacitors. We set C to 100nF for all simulations because it is a popular value in the industry. Table 3 shows the resulting output measurements.

Figure 3 – XAUI Compliance Test/Measurement load

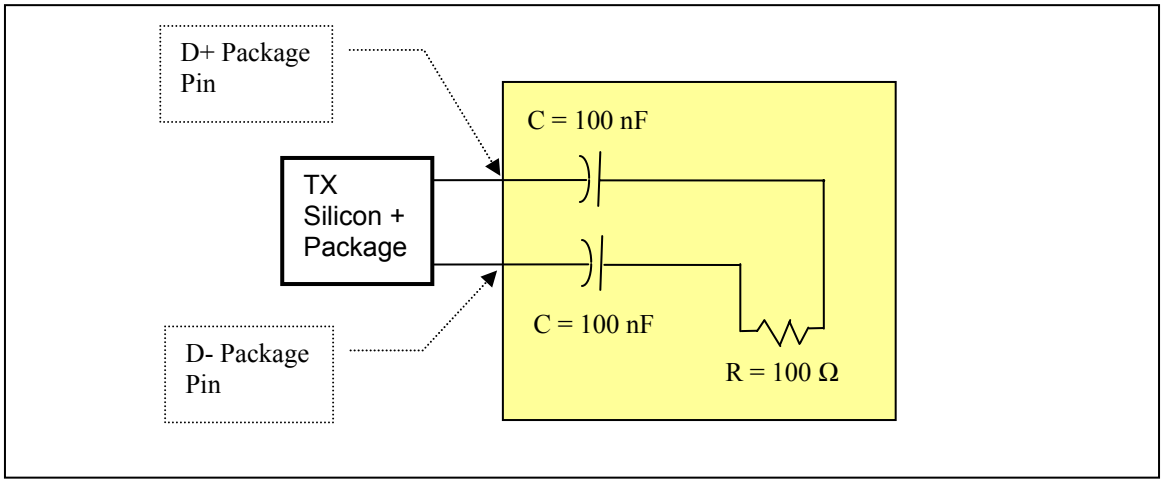


Table 3 – XAUI TX Silicon + Package Measurements at Package Pin

	V_{p-p}[1]	Total Jitter
Specification	≥400 mV	≤ ±56 psec
Measured	400.1 mV	±55.9 psec

[1]X2 to 1-X2, the TX mid bit sample time, is 70.4 psec when UI = 320 psec.

The eye pattern generated in the XAUI driver compliance test simulation can be found in Appendix A of this paper, picture #1.

Full Circuit Compliance Measurements

Differential Voltage and Eye Width Measurements at Receiver End

Table 4 – XAUI Measurements at Receiver End, 5 mm stack height

QTH-DP/QSH-DP Connector, 5 mm Stack Height	Max Jitter at UI = 320 psec	Min RX Eye Width, X1 to 1-X1 (See example mask template)	Min Rx Differential Voltage, A1 to –A1[1] (See example mask template)	Pass/Fail
Specification	**≤ ±88 psec**	**≥112 psec**	**≥100mV$_{p-p}$**	-
10" total trace[2]	±57.3	311.8	251.6	Pass
20" total trace	±49.9	300.7	155.4	Pass
22" total trace	±59.8	288.0	138.2	Pass
24" total trace	±63.9	276.8	127.3	Pass
26" total trace	±61.8	271.6	110.0	Pass
27" total trace	±67.9	262.5	92.9	Fail

[1]X2 to 1-X2, the RX mid bit sample time, is 64 psec when UI = 320 psec.

[2]45.5 mV$_{DIFF}$ has been added to RX minimum V$_{DIFF}$ specification of 88 mV$_{DIFF}$ to account for the difference in the Xilinx TX driver/package output, which is 44.4 mV$_{DIFF}$ above the XAUI minimum V$_{TX-DIFF}$ specification. See Table 3 in this document.

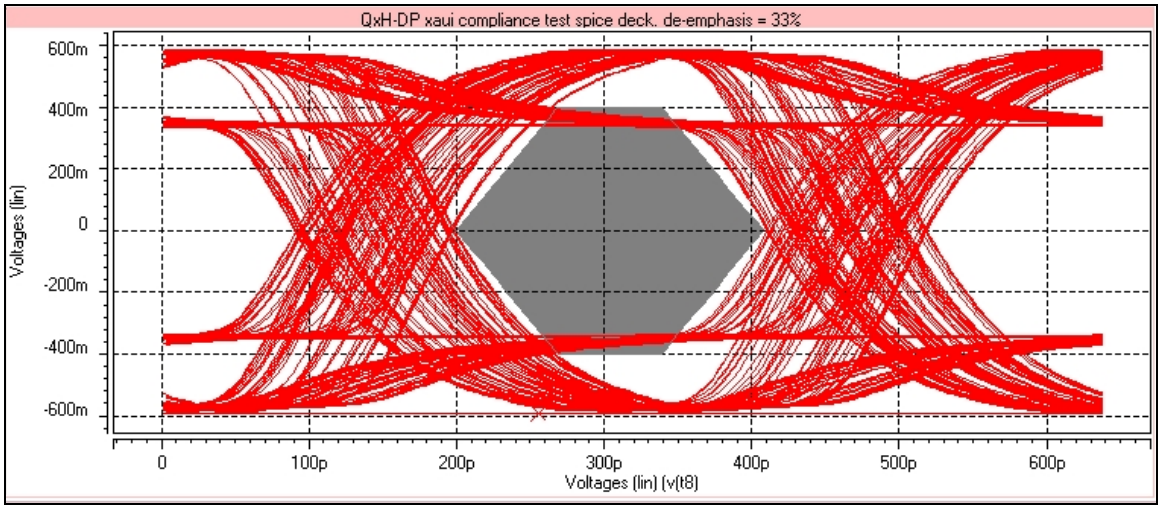
[3]The total trace length specified is the sum of the two differential trace lengths in the QTH-DP/QSH-DP test fixture model, as shown in Figure 1. These traces are always kept equal in length in each simulation.

The eye pattern generated in the XAUI circuit simulation with 26 inches total trace length can be found in Appendix A of this paper, picture #2.

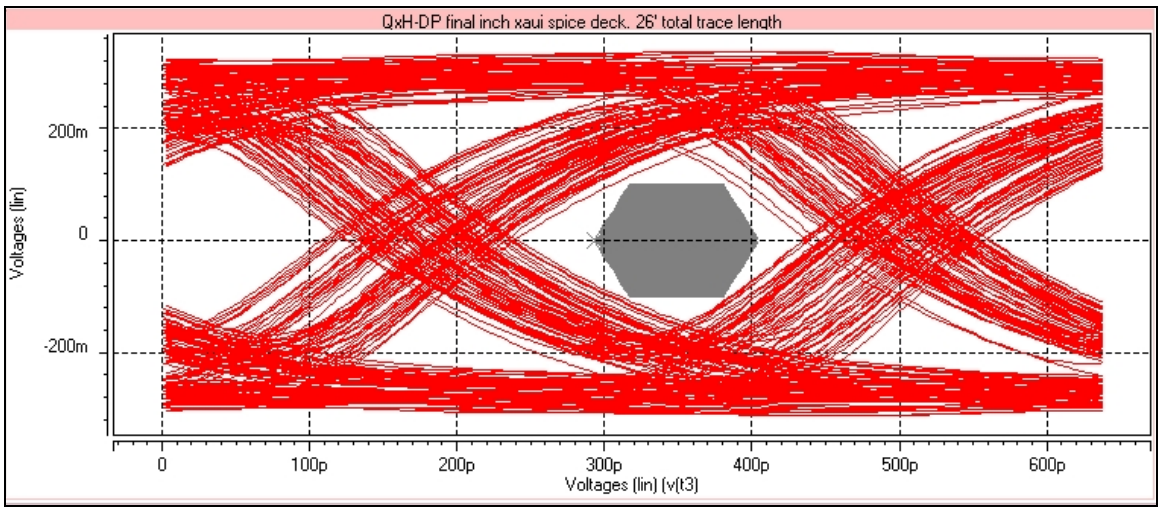
Conclusions

A single Samtec Q Pairs® QTH/QSH-DP 5 mm stack height connector in a board-to-board configuration can be used in XAUI systems with total trace lengths not to exceed 26 inches when used with Samtec's Final Inch™ routing, breakout, and trace width solutions. Because loss is the dominant contributor to system degradation, designers should be aware that using smaller trace widths, laminates with higher loss tangent, and sub optimal routing solutions with higher pair-to-pair coupling and additional via stubs will decrease overall performance and the maximum allowable trace length. It is advisable when designing systems that approach the maximum jitter limits to perform detailed modeling, simulation, and measurement of the target design including the effects of material properties, traces, vias, and additional components.

Appendix A – Waveform images



Picture 1 – Worst case stimulus differential eye waveform, probed at Xilinx driver package pins, connected to compliance test/measurement load



Picture 2 – XAUI circuit differential eye waveform, probed at terminator pins, 26 inches total trace length