400+ Gbps Interconnects: Technical Challenges, Solutions, and What's Needed

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Abstract

This white paper outlines the application needs and market forces driving the specifications for 400+ Gbps systems, the emerging technical challenges for interconnects above 224 Gbps, the need for future work, and possible ways forward.

Integration leads to Innovation

Samtec is structured like no other company in the interconnect industry: we work in a fully integrated capacity that enables true collaboration. The result is innovative solutions and effective strategies supporting optimization of the entire signal channel.

For more information contact SIG@samtec.com

Introduction

AI and cloud infrastructure scaling is driving development of 400+ Gbps systems. Data rates above 224 Gbps require higher performance test equipment, interconnects, and fixtures. The result is increased demand for creatively engineered hardware and test setups, and work is centered on both copper and optical interconnects at these speeds. This white paper outlines the application needs and market forces driving the specifications for 400+ Gbps systems, the emerging technical challenges for interconnects above 224 Gbps, the need for future work, and possible ways forward.

Application Needs: The Rise of AI Infrastructure

Traditionally, as data rates increased, such as in the shift from 56 to 112 Gbps or 112 to 224 Gbps, the industry standardized a design approach for a specific data rate across applications. That will likely not be the case above 224 Gbps, as specific data rates and technology approaches may be driven by a variety of applications, use cases, budgets, or business needs. For some designs above 224 Gbps, customized engineered solutions might prevail rather than a standardized approach.

Currently, data center designs and build outs are dominant industry drivers, but the server, storage, and networking equipment used inside the data center has distinctly different sets of requirements. The traditional role of data centers moving and storing data led to standardized system architectures, including front panel access and rack form factors.

AI disrupts the traditional role of data centers. While GPUs continue to dominate AI infrastructure, scaling GPUs does not require traditional rack and stack form factors, and the front panel approach is inefficient for AI scale-up/scale-out. AI computing in data centers may require non-standard system architectures to satisfy required data rates. One industry example of a successful non-standard engineered solution is NVLink™, a customized interconnect technology developed by Nvidia to communicate between GPUs and CPUs using mesh networking (unlike the central hub configuration used by PCIe, the industry standard). As other non-GPU AI accelerators scale, new system architectures, signal channels, and application needs will arise demanding 400G channel data rates.

Technical Challenges: Modulation Schemes

The lack of a released standard for 400G could mean that design teams continue to mature a particular configuration until it reaches its data rate limit. For instance, a copper system running at 300G PAM8 uses 56G Nyquist, the same as 224 Gbps PAM4, so there is a good understanding of the physics and no need to switch out the front-panel connectors.

There is ongoing discussion about whether PAM4 or PAM6 will be used in 400+ Gbps copper systems. SERDES signal performance at PAM4 modulation is well understood; a switch to PAM6 signaling requires investigation into effective noise and channel modeling. It will be important to understand if the current test and measurement equipment captures the relevant noise penalties associated with PAM6 modulation.

The path to 400+ Gbps systems can benefit from a flexible architecture that preserves future technology choices, one that, for example, allows the same platform to map ports to PAM6 copper and PAM4 optics. CPX is a versatile co-packaged copper (CPC) and co-packaged optics (CPO) interconnect topology that achieves these objectives. It also improves serviceability, supports multi-vendor ecosystems [1-3], and maintains competitive sourcing options from multiple suppliers.

Defining Metrics for 448 Gbps

CPX topologies were introduced for 224 Gbps and are well studied and documented [1-3]. The data discussed here comes from preliminary work with a prototype CPC (co-packaged copper) 448 Gbps cable assembly believed to be representative of next-generation interconnects (Figure 1). It is proving useful to help define key metrics for 448 Gbps and analyze frequency response and SNR.

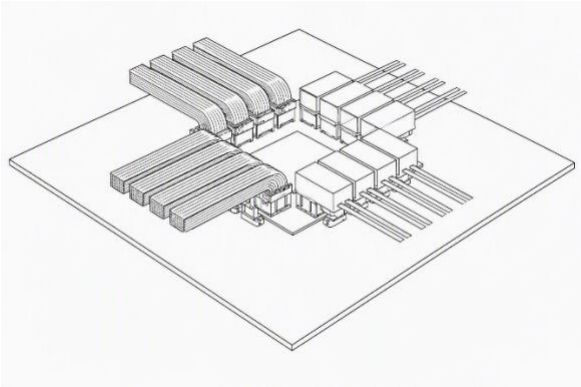

Figure 1: A CPX topology that supports copper cable and/or optics, such as this Samtec Si-Fly® HD co-packaged cable assembly, is used in prototype systems for 448 Gbps.

CPC places the high-speed separable electrical interface directly on the package substrate. In this topology, the twinax cable is not lossless, but it is better controlled with a larger copper cross-section medium than long package and PCB routing for high-speed links. The benefit comes from eliminating package-to-board transitions, PCB breakout, via fields, and connector launches from the highest-speed portion of the channel.

With this interconnect, two primary challenges emerged for channel response performance at 448 Gbps: (1) achieving a smooth frequency response with minimal

resonances, and (2) maintaining sufficient signal-to-noise ratio (SNR) to enable detection at a target symbol error rate.

Measured Results

The measured channel in the 448 Gbps CPX prototype interconnect includes precision RF interfaces, short PCB routing, and a twinax cable segment, resulting in approximately 20 dB insertion loss at frequencies slightly above 100 GHz (Figure 2).

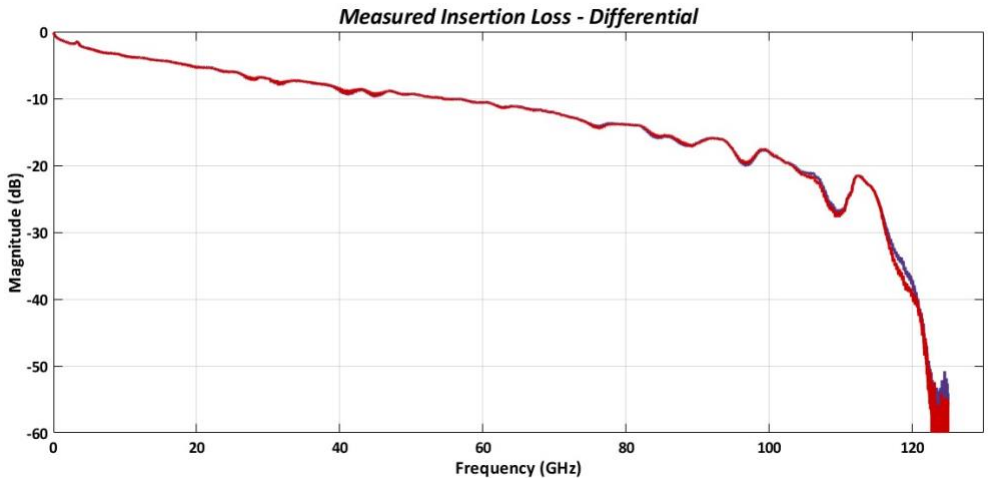

Figure 2: 448 Gbps CPX prototype measurement including RF connectors, test fixture PCB routing, and twinax cable.

The channel response remains relatively smooth, with minimized impedance discontinuities and controlled reflections, underscoring the importance of careful channel design in mitigating resonance-induced impairments. We identified the following major areas of concern in channel design: electrical resonance, crosstalk and shielding, and ensuring manufacturability.

At 224 Gbps PAM4, the Samtec CPX topology has industry-leading performance with separable interface capability. This same topology, which features a short contact wipe (stub) was used as a basis for the 448 Gbps prototype. Our work showed that at 448G, it is necessary to further reduce stubs; however, this could impact mechanical tolerance due to extremely small feature sizes (Figure 3).

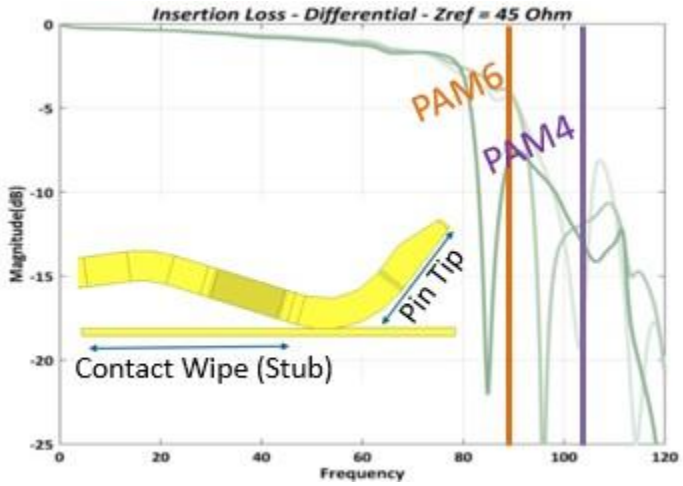

Figure 3: At 448G, it is necessary to further reduce stubs, which could impact mechanical tolerance.

Reducing crosstalk at 448 Gbps requires additional shielding and an improved return path as compared to a 224 Gbps topology. It is best if shielding cavity modes are managed simultaneously. Unfortunately, additional shielding and continuity paths increase the design size and lead to reduced density. Ways to address this could include miniaturization and novel contact designs.

It is important to note that connector density is not only a mechanical placement issue. At 224 and 448G, it also controls the distribution of loss, skew, return loss, and crosstalk across the lane population. A lower-density connector can appear easier to route yet still produce a worse-case lane if added rows force long detours around the connector field.

The design target should, therefore, be the full lane distribution rather than only the nominal lane. A HDI topology with slightly higher typical loss but a much tighter tail can be easier to equalize, train, test, and manufacture than a topology with a few long, lossy outliers (Figure 4).

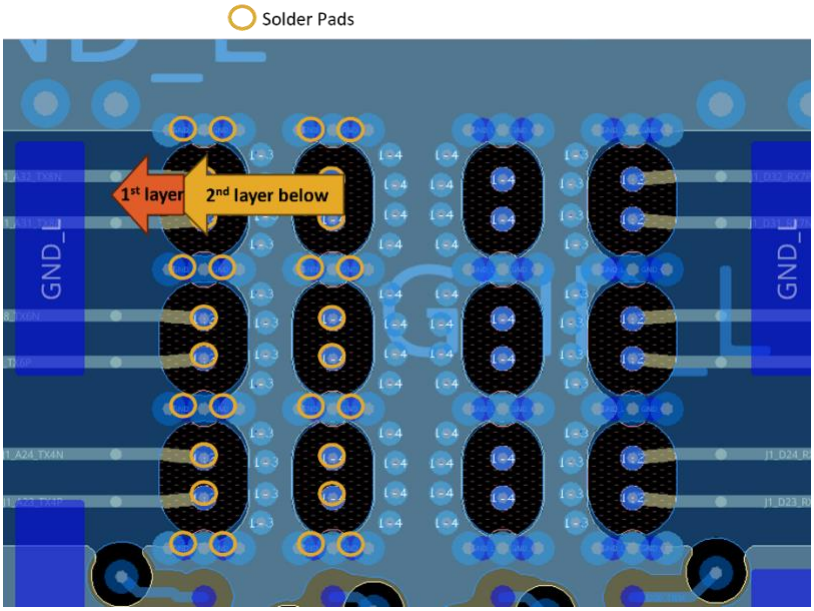

Figure 4: HDI escape for dense co-packaged connectors. Terminated microvias and HDI layers (indicated by orange arrows) reduce detours and narrow lane-to-lane loss variation relative to row-wise non-HDI breakout.

While designing for optimal channel performance (SI) is a priority, real-world production introduces variability, which can result in missing design targets for impedance and return loss (RL). In addition, current tooling capabilities are at their limit, so we can expect more RL at extreme frequencies. Also of note, silicon capability is expected to absorb more of the SNR budget.

As a result, there is increased pressure to tighten tolerancing and creative solutions need to be found for manufacturing. There are numerous possibilities to reduce variation in interconnect performance that require further study: increase coupling to highly controlled conductors; decrease coupling to highly variable conductors; incorporate more precise mating and latching features; use design variation-resistant structures; and incorporate compression and elastomers.

Uncertain Nyquist

In the tradeoff between interconnect size, manufacturability, and performance, interconnect designers must determine what levels of performance are acceptable. This is especially challenging with targeted Nyquist frequency for 448 Gbps designs ranging from 86 to 90 GHz for PAM6 and 106 to 112 GHz for PAM4. In these circumstances, interconnects with a typical 0.5 to 1.0 mm pitch will experience cavity resonance near Nyquist frequency due to the shielding around the differential pair.

The quality of the Rx filter will be important and impact the performance calculation. At 224 Gbps PAM4, the Rx filter is 5% beyond Nyquist frequency, significantly derating more high frequency noise content than the previous generations (Figure 5). It is unclear if that will be the same at 448 Gbps. Given the very wide bandwidth, every increase in operation frequency without impairment makes the manufacturability of cost-effective solutions very challenging. Further work is needed to determine if resonances or suck out below Nyquist will be acceptable.

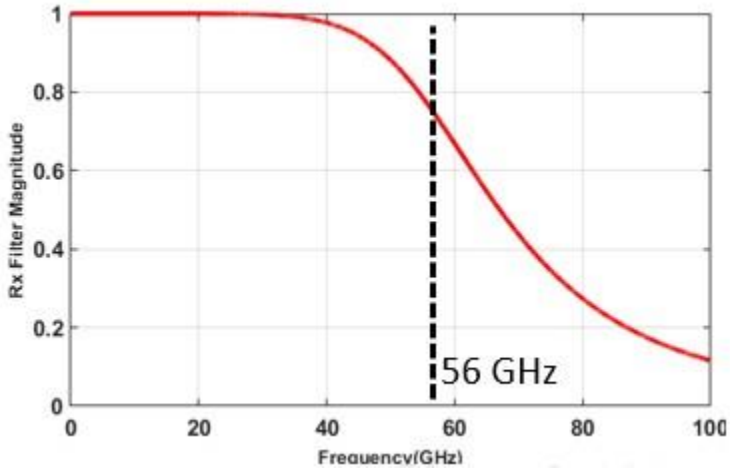

*Figure 5: 224G Rx Bessel-Thompson Filter fb*0.55*

Market Drivers: Hardware, Costs, and Skills

Traditionally, standards bodies have taken the position that a standard must be compatible with copper and optical transmissions; for 400+ Gbps, they are considering that it may only be an electrical (copper) path for PAM6 modulation. It is likely that the OIF will standardize on PAM4 for optical links; this will avoid engineering and hardware costs that would be required to convert optical current module designs to PAM6. Fortunately, there are many packaging strategies that do not require PAM6 above 224 Gbps, such as CPX [3]. Co-packaged optics (CPO) as part of a CPX architecture allow the optics to be very close to the transceivers that can be running at a full PAM4 signaling rate.

Meanwhile, OEM demand for hardware puts pressure on system designers. If they can integrate technology and deploy it, there are customers ready to purchase and deploy that hardware before standards are finalized. This is already happening for 200G systems, with hardware shipping before a completed 200G specification.

Another major market driver is the cost of test. During silicon testing at 224 Gbps data rates, tradeoffs are regularly made between bandwidth and cost. For instance, test engineers must decide: Are 1.0 mm front-panel connectors necessary for 224 Gbps signals or would 1.85 mm connectors be good enough? [4] Technical challenges can

change dramatically at higher data rates, where it quickly becomes a concern that even 1.0 mm front-panel connectors might not offer high enough test bandwidths.

Fortunately, test and measurement companies have been addressing these challenges and are subsequently demonstrating performance well beyond the traditional 110 GHz from 1.0 mm connectors [5]. For copper, 448 Gbps PAM4 has a 112G Nyquist frequency. In order to perform test, measurement, and validation, engineers need a measurement bandwidth greater than 112 Gbps. This translates into 120 GHz or 130 GHz test fixtures and test infrastructure, which are now available (see Figure 6) [6]. (Note that at 448 Gbps PAM6, Nyquist is 80 GHz, so measurements can be performed on 110 GHz test equipment with standard 1 mm interconnect.)

Figure 6: The Samtec BE130 features mode-free performance to 130 GHz and lowest insertion loss and highest frequency possible for 1.0 mm-based equipment. It has an expanded mode-free bandwidth beyond 448 Gbps fundamental frequencies.

Characterizing silicon at 400+ Gbps PAM4 requires the use of mmWave level test fixtures, cables, and connectors at 130 GHz or higher. Engineering teams may require a significant capex investment to make these millimeter wave measurements.

In addition to an investment in test equipment and fixtures, those designing for 400+ Gbps PAM4 will need access to expertise in mmWave engineering. This could be achieved by partnering with an interconnect or test company that offers engineering services. Without in-depth understanding of mmWave engineering, the loss from the test fixture could lead to a failure to meet the required levels of performance.

Packaging Strategy: CPX Offers Pathways

CPX is attractive because it provides flexibility at the system configuration item level during a period when PHYs, modulation schemes, optics, and packaging technologies are still evolving. It is a high-density interconnect architecture that places high-speed copper and/or optical I/O very close to the ASIC, GPU, switch silicon, or processor package rather than routing signals across PCB traces or to traditional front-panel pluggable modules. The goal is to reduce channel loss, power consumption, latency, and board complexity while increasing bandwidth density. As a practical architectural step that can be implemented with today's technologies and supply chains, it is proving

to be a well-suited approach for 224 Gbps systems as well as emerging higher data rate systems.

As a packaging strategy, CPX provides system architects with freedom, field serviceability, and a migration path when designing a system, which is especially important during times of early adoption. CPX architectures, (see Figure 7) such as the Samtec Si-Fly® HD systems [7], allow for co-packaged copper and optics to exist simultaneously, allowing system integrators to choose a technology to satisfy loss budgets, with copper cables for short runs and fiber optics for longer connections. Because the connectors work with both copper and optical solutions, the type of channel can be decided in the field. Samtec has arranged second-source agreements to license its Si-Fly® HD interconnect with other industry-leading interconnect suppliers.

The Open Co-Packaging Multi-Source Agreement (Open CPX MSA) is an industry consortium founded in 2026. Its focus is on developing open specifications that make CPX interoperable across multiple vendors, with an initial focus on co-packaged optical interconnects [3]. Samtec's Si-Fly® HD CPX technology is an implementation of this architecture, and Samtec is a founding member helping to define the Open CPX ecosystem. Other founding members include Marvell, Molex, Ciena, Coherent, and TeraHop. The Open CPX MSA aims to standardize connector mechanicals, thermal requirements, electrical pinouts, mechanical form factors, as well as optical, electrical, and management interfaces.

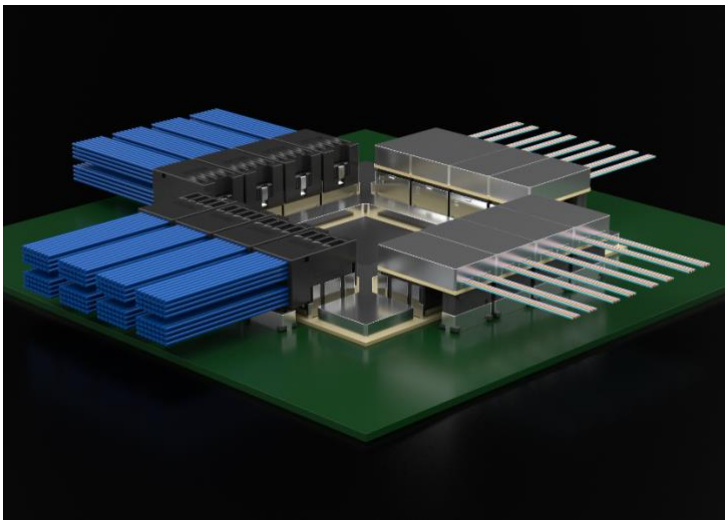

Figure 7: The Samtec Si-Fly® HD CPX architecture currently supports 224 Gbps with development to 448 Gbps.

Looking Ahead

AI clusters are driving bandwidth requirements far beyond what traditional front-panel networking architectures were designed to support. As data rates move toward 448 Gbps and beyond, the electrical channel between the ASIC and the optical module becomes increasingly difficult to manage. There will likely be multiple ways forward,

including standards driven by OIF and IEEE for 224 Gbps and 448 Gbps signaling. We can also expect to see engineered solutions at various bandwidths and modulation schemes above 224 Gbps PAM4. Much work still needs to be done, but new interconnect packaging technologies, such as CPX, will be instrumental in driving the high-density, high-performance solutions of the future.

Resources

[1] B. T. Gore, R. Mellitz, A. Josephson, F. de Paulis, L. Boluna, J. Calvin, R. Rabinovich, and M. Resso, "Beyond 200G: Brick Walls of 400G Links per Lane," DesignCon 2025.
[2] O. Shimizu, S. Krooswyk, S. Sankararaman, A. Mizumura, and C. Faith, “Extending Co-Packaged Copper for 448G,” ICSJ 2026.
[3] Open CPX MSA, "Open Co-packaging Multi-Source Agreement," accessed July 2026.
[4] B. T. Gore, R. Mellitz, A. Josephson, F. de Paulis, L. Boluna, J. Calvin, R. Rabinovich, and M. Resso “Are 1.0 mm Precision RF Connectors Really Required for 224 Gbps PAM4 Verification?” DesignCon 2024.
[5] “Race to 448 Gbps” Keysight White Paper, March 2026.
[6] Bulls Eye® High Performance Testing Solutions to 130 GHz Product Information
[7] Si-Fly® HD 224 Gbps PAM4, Co-Packaged & Near Chip Systems Product Information