# Achieving 224 Gbps PAM4: **New Interconnect Methods to Ensure Signal Integrity**

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## Abstract

Successfully delivering 224 Gbps PAM4 signals requires careful analysis of signal integrity and thermal effects. This paper explains how 224 Gbps PAM4 systems differ from previous generations in terms of interconnects, what technologies and methodologies enable 224 Gbps PAM4 interconnects, and what may be required to reach beyond 224 Gbps.

## Integration Leads to Innovation

Samtec is structured like no other company in the interconnect industry: we work in a fully integrated capacity that enables true collaboration. The result is innovative solutions and effective strategies supporting optimization of the entire signal channel.

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## Interconnects are Critical at 224 Gbps and Beyond

Signal integrity, power delivery, and thermal issues are all major concerns in 224 Gbps deployments. As data rates have increased, so have the number of features on the die itself, resulting in a diminished loss margin for the “off chip” part of the design. Mitigating signal integrity and thermal issues while supporting increased power requirements of 224 Gbps systems can be addressed by selecting the right materials, design techniques, system architecture, and provisioning.

High-performance, high-speed interconnects (see Figure 1) with low latency are required for the backplane, mezzanine, near-chip/on-chip, and front panel (copper and pluggable optics). This white paper explains the interconnect architecture choices available to designers at 224 Gbps, with a look beyond to 448 Gbps needs. Analysis includes measured data for comparison.

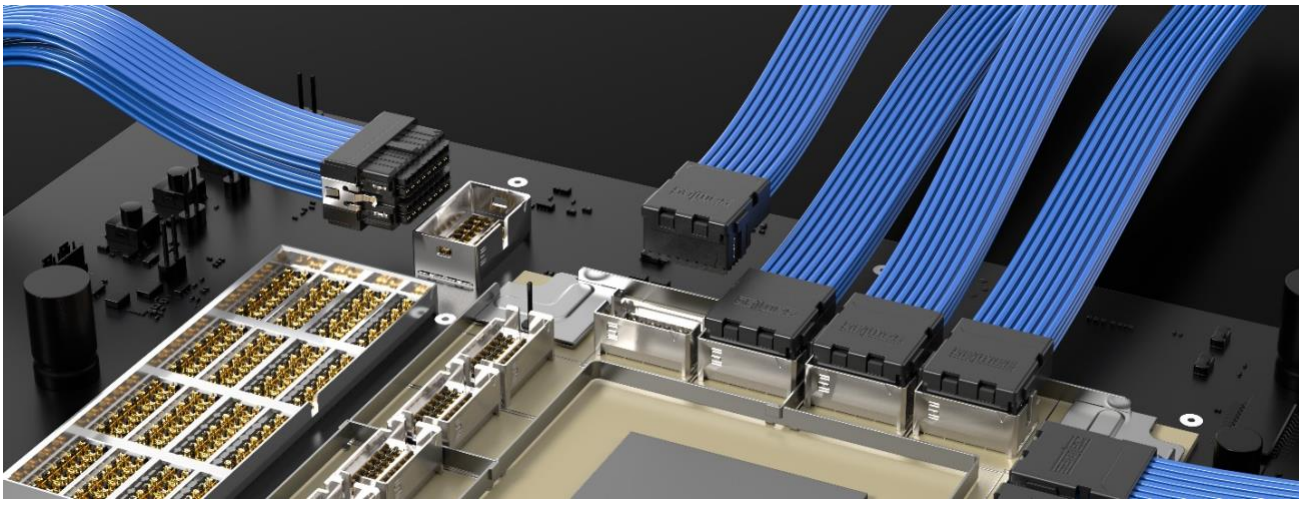


*Figure 1: New interconnects, such as the Si-Fly HD® system shown, are required to support 224 Gbps data rates and beyond.*

## 224 Gbps Design Options: Near Chip Connectors

112 Gbps PAM4 designs frequently use a near-chip approach, where connectors are placed adjacent to the ASIC and connected to twinax, which then links to the front panel, back panel, or mid-board. This approach reduces the overall loss of the channel [1, 2].

This near-chip approach can be deployed in some 224 Gbps PAM4 system designs, dependent on design density and power needs. In a near-chip approach, the designer must break the IO out to BGA and PCB solder balls, with the resulting size limited by current plated through-hole (PTH) PCB technology (in other words, limiting it to 0.8 mm BGA pitch). With this approach, it can be difficult to achieve signal integrity out to and beyond 56 GHz. An additional issue is that the interconnect allocated for IO is now unavailable to use on equally demanding power issues.

## 224 Gbps Design Option: Co-Packaged Connectors

A related design challenge for near-chip (ASIC adjacent) cable systems is the reflections from the vertical package components: BGA via, solder ball, and package core. The system margin will be greatly improved if the connector is placed directly on the package—a co-packaged copper or optics (CPX) solution—which avoids these reflections and addresses scaling issues. Of course, CPX solutions must be low profile enough to be placed underneath the heatsink.

PCB feature scaling is much slower than ASIC feature scaling with silicon CMOS, setting up the need for a new approach to bridge the gap (see Figure 2). Today's design needs are naturally pushing designers towards using co-packaged copper (CPC) so they can meet the required IO density scale. In contrast to a near-chip approach, CPX enables higher density footprints in the separable interfaces for assembly due to a different systemic hardware breakdown. The CPX approach is much finer, with a small connector at the substrate, allowing IO counts of 512 ports and higher.

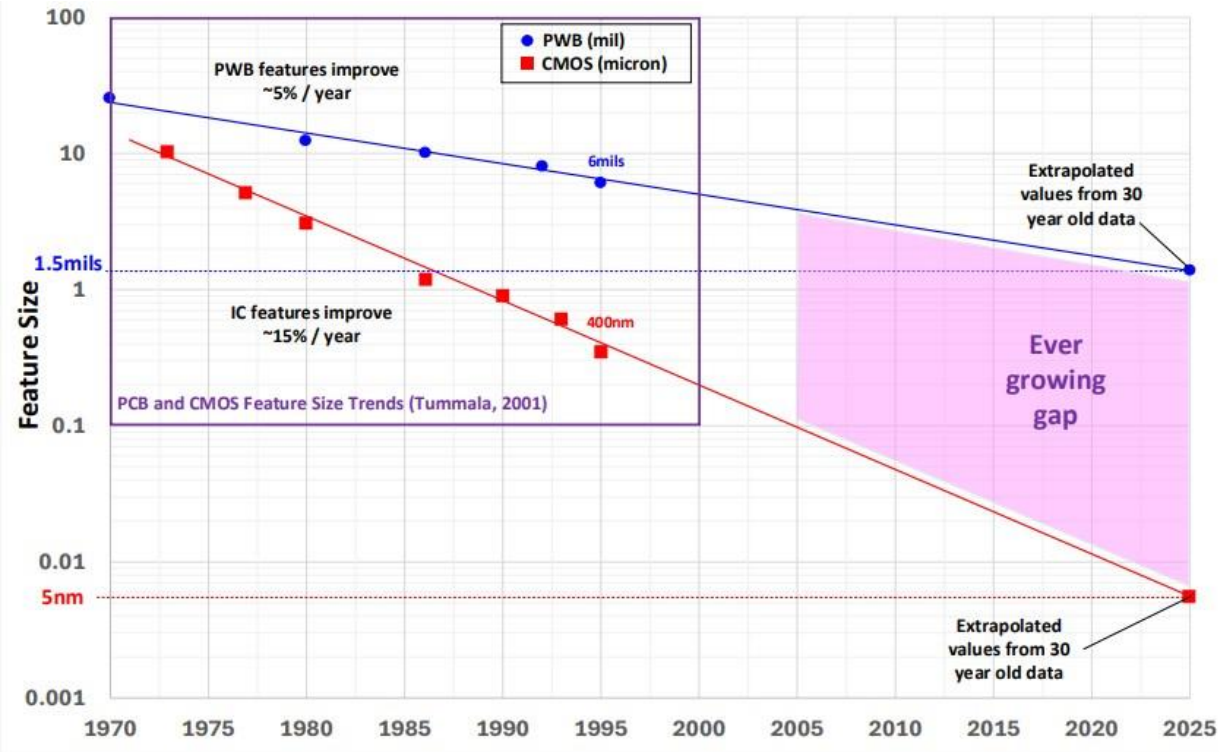



*Figure 2: PCB feature scaling is much slower than ASIC feature scaling with silicon CMOS. That gap has become too large to cross without a giant step function, such as moving the twinax termination to the package in co-packaged connectors.*

At a 224 Gbps data rate, CPX presents a higher value to recover system margin from package reflections and losses from PCB trace routing. Samtec has been developing direct-to-package technology for years, initially for 112 Gbps and now for 224 Gbps PAM4 [3].

## New Connectors for 224 Gbps Systems

The Samtec Si-Fly HD® connector was specifically developed for 224 Gbps and beyond, and it can either be placed adjacent to the ASIC or placed on the chip package itself (see Figure 3). In the co-packaged (CPX) configuration, there is no trace through the PCB, and no subsequent "loss per inch." Moving to a CPX configuration can save as much as 3 dB of loss from package via and ball and PCB routing, which can make the difference for a successful 224 Gbps PAM4 system.

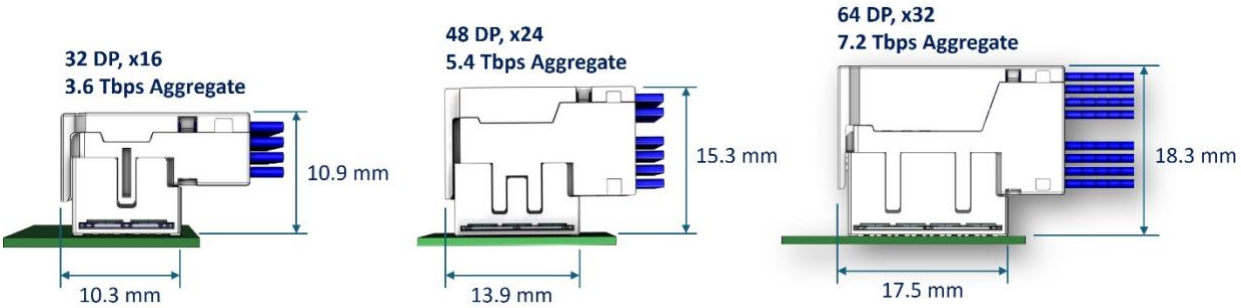



*Figure 3: Samtec Si-Fly HD CPX connector for 224 Gbps PAM4 is available to support 32, 48, or 64 differential pairs.*

The silicon die is placed on a chip substrate, which is the most expensive real estate in the system, so any connectors built into the chip package must be extremely small. The Si-Fly HD connector measures 14 $mm^2$, and it can support 64 differential pairs (64 twinax cables).

Processing is different for CPX because the connectors need to be soldered onto the chip substrate. Figure 4 demonstrates the assembly process. The Si-Fly HD connector uses Samtec's column tail design for advanced structural integrity of the solder joint during and after reflow. This non-solder ball design improves uniformity, repeatability, and coplanarity [4]. Copper or optical cables are then plugged directly into the chip package. Specific solder (designed for SAC305, but Indium-based low-temperature solders also can be used), stiffener, and assembly process can vary by application.

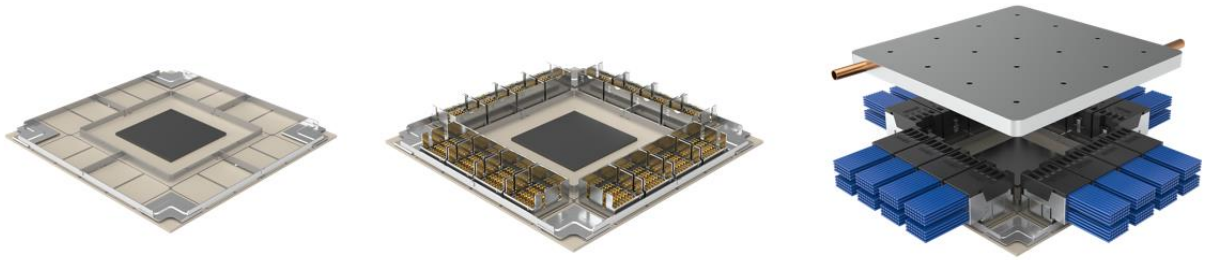


*Figure 4: Si-Fly HD processing requires the non-solder ball connectors to be attached to a supported substrate. Cables are then plugged directly into the chip package. Specific solder, stiffener (left), and assembly process (center) varies by application before adding cables and installing cooling plate hardware (right).*

## Si-Fly HD Performance

Samtec tests its 224 Gbps PAM4 interconnect solutions against channel models from industry standards groups such as IEEE 802.3. Measurements performed on the Samtec Si-Fly HD CPC exceeded expectations, showing a significant improvement in insertion loss as compared to a near-chip in a similar implementation.

In fact, connectivity from the top of the package offers a compelling reflection and insertion loss advantage. A simulation model for system design along with measurement validation for loss and reflection are shown in Figures 5a and 5b. Si-Fly HD cable assembly measurements demonstrate excellent insertion loss with smooth insertion loss deviation (ILD) on Samtec Eye Speed® Hyper Low Skew Twinax.

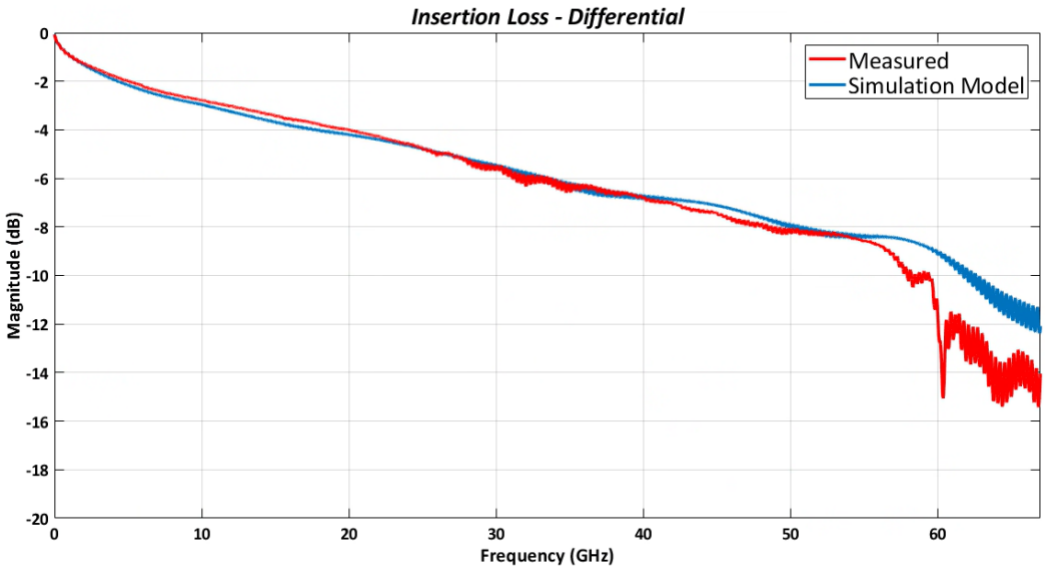



*Figure 5a: Differential insertion loss for the Si-Fly HD CPC at 224 Gbps PAM4 measured versus model, showing smooth insertion loss with minimal insertion loss deviation.*

Return loss measurement and model correlation are shown in Figure 5b. Low return loss is critical in co-packaged applications where connectors or discontinuities may re-reflect close to the transceiver. Figure 5b shows that Si-Fly HD CPC achieves low return loss and correlation to models.

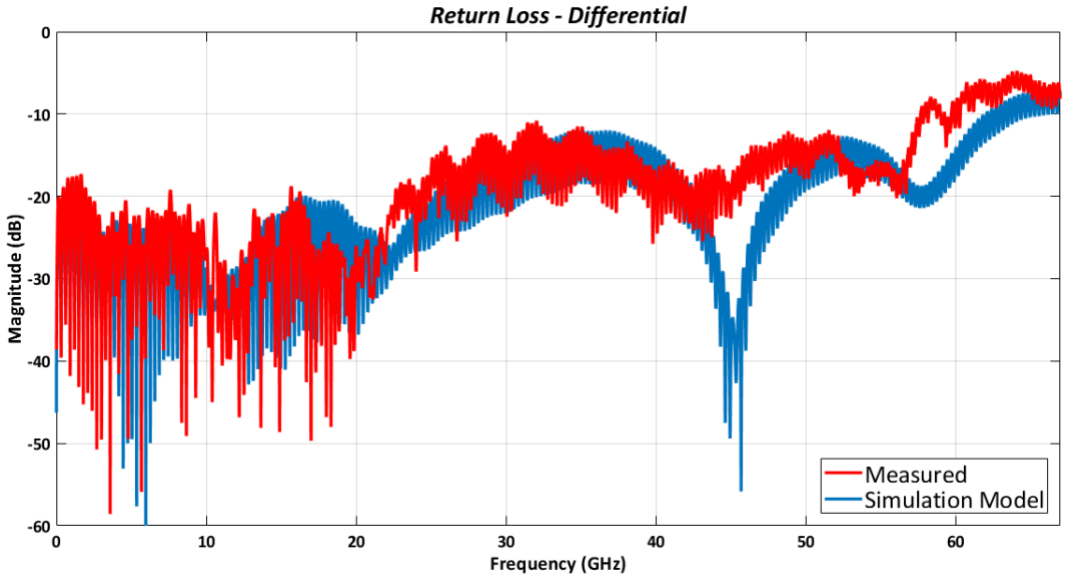



*Figure 5b: Differential return loss for the Si-Fly HD CPC at 224 Gbps PAM4 measured versus model, showing low noise for the co-packaged device.*

At 112 Gbps and 224 Gbps, insertion loss is a critical consideration. But one of the most difficult electrical performance criteria is crosstalk. When driven to ultra-high density (64 DPs in 14x14 mm), crosstalk usually increases due to the proximity between pins. Fortunately, measurements performed on the Si-Fly HD CPC show impressive crosstalk performance. Figure 6 demonstrates measured crosstalk on the Si-Fly HD CPC and simulation model, achieving accurate correlation, and integrated crosstalk noise (ICN) FEXT performance of 0.36 mV rms that is far below the targets at 224 Gbps.

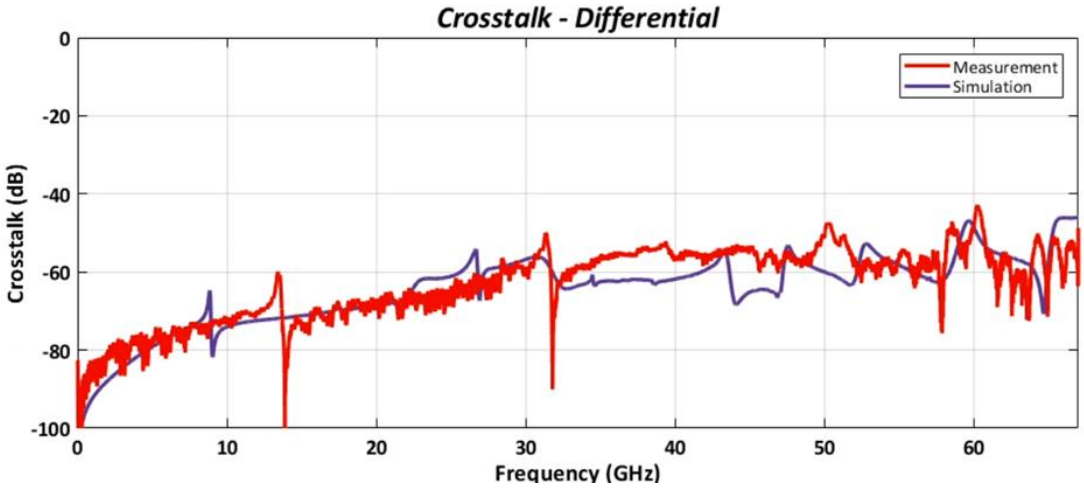



*Figure 6: Si-Fly HD CPC demonstrates extremely low crosstalk, and measurement correlates well with model expectations.*

## Skew: Issues and Avoidance

Skew is another design concern for 224 Gbps PAM4, and its impact can be significant. Skew-like distortion can manifest as delay differences within a differential pair (due to physical and electrical construction in the channel), asymmetry in the compliment trace (e.g. n or p) during the construction of a differential pair, or differences in the driving signals. The design of the coupling and the amount of reflection determines the significance of the impact [5-7]. Figure 7 displays the differential skew vs frequency of a complete cable assembly. These levels of skew produce signal to common mode ratio (SCMR) of the channel in the range of 18 to 36 dB [8].

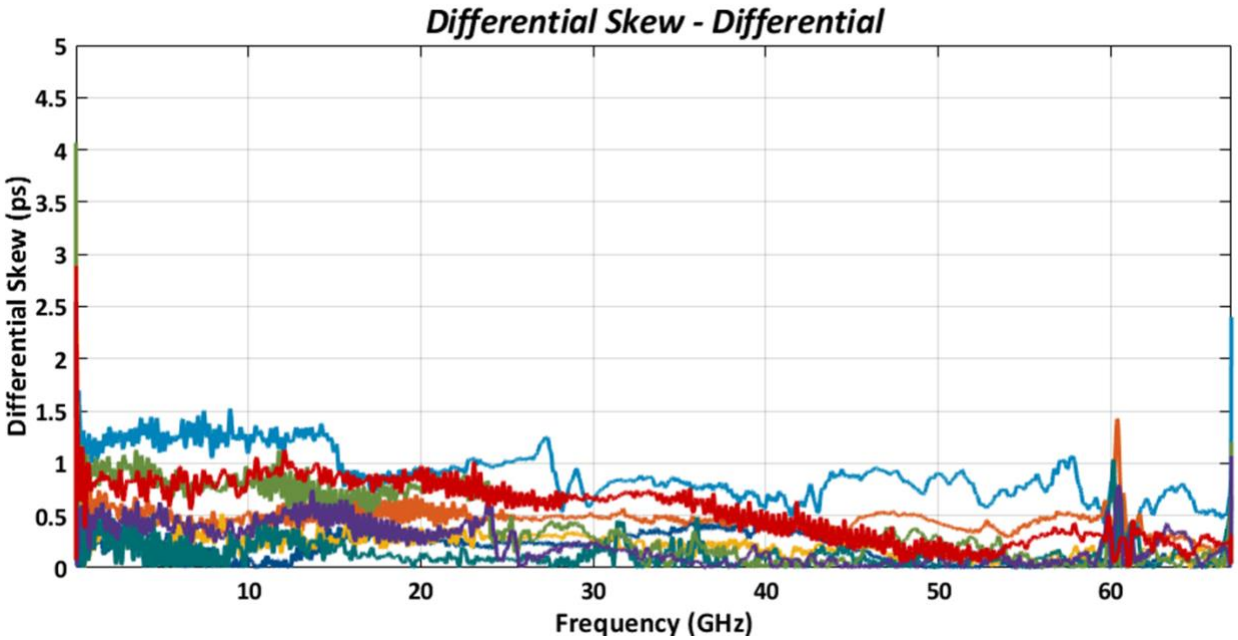



*Figure 7: Complete cable assembly differential skew (Si-Fly HD + Flyover® Twinax + Si-Fly HD)*

Samtec has engaged in significant R&D as regards to the impact of skew, comparing the effect in both Flyover® twinax and PCB traces [5],[9]. Fortunately, tightly coupled, co-extruded twinax cable has superior skew (as well as impedance and insertion loss stability) even under realistic bending conditions that allows skew to be completely under the implementer's control. This is in stark contrast to other twinax cable constructions.

For 224 Gbps PAM4 systems, controlling skew is critical to predictable performance, particularly because one unit interval (the width of a single bit) is approximately 9 ps at 224 Gbps PAM4. CPX and near-chip Flyover cable can be used by system designers to reduce interconnect skew to manageable levels.

## Achieving 224 Gbps with Samtec

For 224 Gbps designs, Samtec offers a suite of interconnect solutions, including the flagship Si-Fly HD high-density 224 Gbps PAM4 co-packaged (SFCC/SFCM) and near-chip (SFNC/SFNM) cable systems.

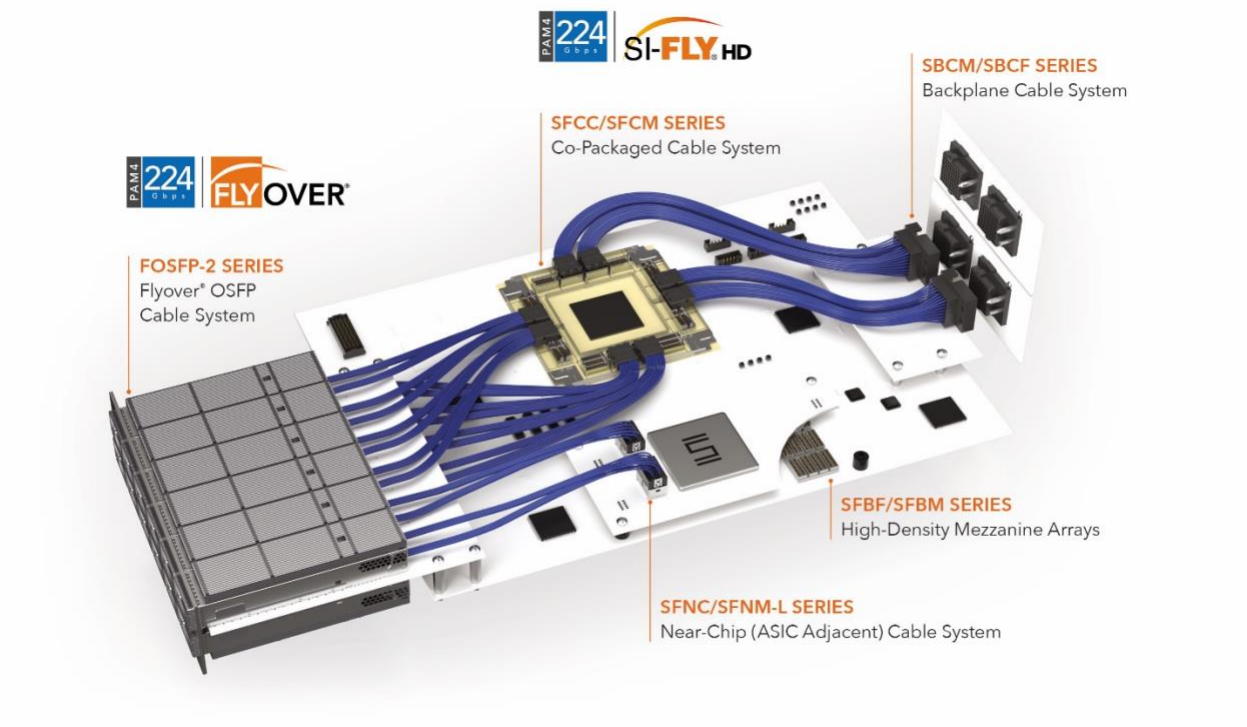


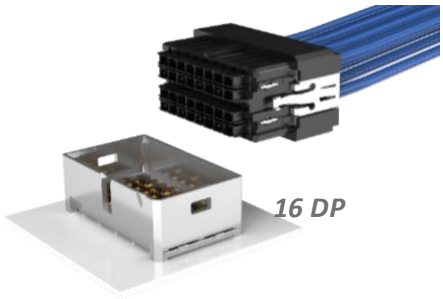

*Figure 8: Samtec cable and connector solutions for 224 Gbps PAM4 designs.*

Co-packaged cabled systems such as those in Figure 8 offer the lowest loss signal transmission from the package to the front panel or backplane while providing the highest signal density. The Si-Fly HD system allows system architects to interchange copper for short distances/scale-up and optics for extended reach/scale-out using the same electrical substrate connector.

Co-packaged copper (CPC) connectivity eliminates insertion losses in the BGA breakout and the PCB. This technology makes a complete 224G passive DAC 224G channel possible, enabling a low-power linear pluggable optics front panel solution that could have immense potential for connectivity in some emerging AI architectures.

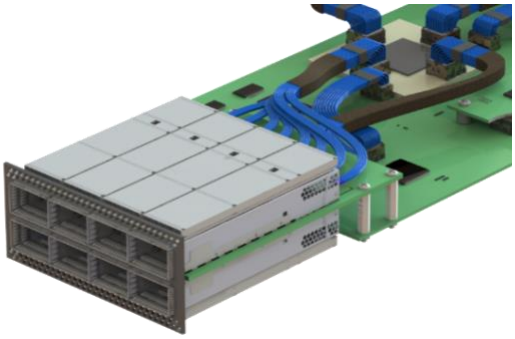
The Si-Fly HD co-packaged solution (CPX) uses the same connector for electrically pluggable co-packaged copper and/or co-packaged optical high-density, high-performance interconnects on a 95 mm x 95 mm or smaller substrate (SFCM, SFCC, Optics). It supports up to 170 differential pairs per square inch and is specifically designed for high density interconnect (HDI) and package substrates. Si-Fly HD is well suited for use in a switch module (card, slot, or blade) in a system that expects a bandwidth bottleneck at 224 Gbps.

Si-Fly HD incorporates Samtec's Eye Speed Hyper Low Skew cable, which features foamed dielectric twinax and the industry's best signal integrity performance (1.75 ps/m max intra-pair) at 224 Gbps PAM4.

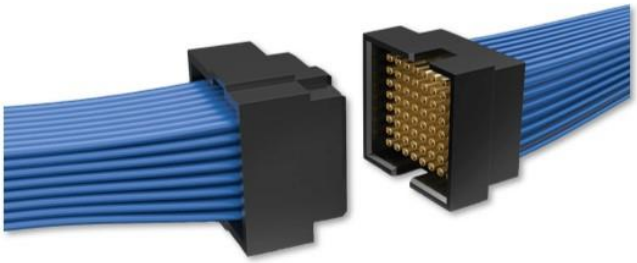



The Samtec Si-Fly HD near-chip solution (SFNC/SFNM) features a signal density of 60 differential pairs per square inch and is designed for use with traditional PCB substrates. The connector length is 15.90 mm and depth is 21.65 mm (for 32 DP). The near-chip Si-Fly HD offers the system architect the signal integrity benefits of ultra-high density Flyover solutions while preserving legacy system configuration items through a PCB compatible footprint.

The Samtec FOSFP-2 224 Gbps PAM4 Flyover panel assembly supports up to 1.6 Tbps PAM4 aggregate data rate using Samtec Flyover cable technology and features direct attach contacts for optimized signal integrity. Designers can also choose Samtec's FOFSP 1600 pluggable optics front panel connector. The FOSFP front panel solution connects to either the Si-Fly HD co-packaged interconnect (SFCC/SFCM) or near-chip interconnect (SFNC/SFNM).



The Si-Fly HD family also includes the Si-Fly HD Board-to-Board Mezzanine System (SFBF/SFBM) that supports 60 differential pairs per square inch. It can be used for full differential pairs, or a mixed configuration of differential, single-ended, and power. Si-Fly HD Board-to-Board Mezzanine System is well suited for use between the PCB and a GPU, such as in blade-level networks.



The Si-Fly HD Backplane (SBCM/SBCF) can be equipped with 32 AWG or 28 AWG Eye Speed Hyper Low Skew Thinax™ for 64 differential pairs (8 pairs per row X 8 rows).

Designers of 224 Gbps PAM4 systems are also using the Samtec Bulls Eye® High-Performance Test System (BE90A or BE71A), which is designed to test chips and systems with 200+ Gbps data rates and is currently being used to characterize up to 448 Gbps signals [10].

Samtec continues to develop high-speed, high-performance interconnects in alignment with evolving models from standards bodies. Enabling technologies, such as advanced solder paste technology [4], will be critical to achieve the next level of signal speeds. Contact Samtec today to find interconnect solutions that are ready for your next-generation design needs [11,12].

## Resources


[1] Gore, Brandon. Next-Generation PCB Loss Analysis | Signal Integrity Journal, June 2023.
[2] Josephson, Andrew, et. al. Selecting a Backplane: PCB vs. Cable for High-Speed Designs | Signal Integrity Journal. May 2023.
[3] Samtec - Direct Connect to IC Package on Vimeo
[4] Huffman, Robbie & David Decker. Improved Solder Joint Connectivity for High-Density Interconnect Applications. May 2023.
[5] D'Silva, Hansel, Richard Mellitz, Steve Krooswyk, Adam Gregory, Beomtaek Lee, Amit Kumar, & Howard Heck, "Comparing the Different Metrics of Intra-Pair Skew in Tracking Channel Performance." DesignCon 2024.
[6] OIF-FD-CEI-224G-01.0.pdf (oiforum.com), p. 18.
[7] Skew … The Rest of the Story SCMR (signal to common mode ratio) for Channel (2023, December) IEEE P802.3dj 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force
[8] SCMR (signal to common mode ratio) for Channels (2025, June) IEEE P802.3dj Ad Hoc.
[9] Gore, B., McMorrow, S. (2017, Sept). Vehicle for Insitu Glass Fabric Characterization, [Invited Talk]. EDI CON USA 2017, Boston, Ma
[10] Gore, Brandon et al. Beyond 200G: Brick Walls of 400G Links Per Lane; DesignCon 2025
[11] Samtec 224 Gbps Products
[12] Twinax Cables, Samtec Flyover® Cable Systems | System Optimization | Samtec