# Analog Differential Signal Transmission across Open-Pin-Field Array Connectors: NovaRay® NVAX 7 mm Stack Height

**September 2026**

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## Abstract

System on chip (SoC) implementations with integrated data converters and RF front-end subsystems are being deployed in 5G/6G, phased array radar, SATCOM, FPGA cards, and test & measurement architectures. This paper describes the research, development, and simulations performed to design the optimal breakout region (BOR) for array connectors that simultaneously carry analog, digital, and/or power signals in an RF environment, as a replacement for traditional compression mount and threaded PCB connectors for RF signals.

## Integration leads to Innovation

Samtec is structured like no other company in the interconnect industry:  we work in a fully integrated capacity that enables true collaboration. The result is innovative solutions and effective strategies supporting optimization of the entire signal channel.

For more information contact SIG@samtec.com

## Introduction

Single-chip baseband system on chip (SoC) products with integrated data converters and RF front-end subsystems are being deployed in 5G/6G, phased array radar, SATCOM, FPGA cards, and test and measurement antennas-to-bits architectures. The development of these RFSoC devices challenges the traditional approach of using compression mount and threaded PCB connectors and cable assemblies to handle the RF signals. A simple alternative, using multiple-ganged connectors, still puts strain on form factors, weight, and financial budgets, especially as high frequency RF channel counts increase in these SoC-based systems.

One approach is to take existing technology that was originally designed for high-performance, high-speed digital signaling and adapt it: array connectors. These connectors make it possible to route high frequency, high-isolation RF signals as well as digital and power signals through a single connector. While these connectors are already proven in high-speed digital systems, using them for RF applications requires the development of specific PCB stack-ups and launch optimizations in order to achieve the differential crosstalk and return loss performance required for frequencies up to 8 GHz and beyond. This paper describes the research, development, and simulation performed to design the optimal breakout region (BOR) for the successful use of array connectors in an RF environment.

## Background

In pursuit of the latest applications, mixed-signal designers have taken FPGA technology to the next level, adding RF sampling data converter functionality on the chip. Traditionally, RF design is a discrete approach, including, for instance, a baseband processor, ADC, DAC, and IF/RF signal chain devices. An RFSoC brings the ADC/DAC and some of the RF signal chain processing into the same package as the FPGA. Examples of these types of devices are the AMD Xilinx Zynq® and Intel® Agilex™ Direct RF-Series, with frequencies up to nearly 8 GHz.

One of the fundamental differences of these new SoC designs is that instead of one or two antennas pathing into a processor, a single chip is now supporting dozens of RF signal chains. This enables new technologies such as 5G MIMO, which also requires beamforming, as well as phased array systems, with a typical phased array having 64 to 128 antenna paths with discrete antennas.

Fortunately, the latest RFSoCs can handle differential RF signals, so this paper will focus on a connector BOR design using differential RF signals. The industry is moving towards differential RF signaling to achieve the necessary noise performance at higher frequencies. Since differential signals are out of phase with each other, they have a natural noise rejection that single-ended designs do not have, essentially cancelling each other's unwanted EM fields [1].

In addition, designers using these SoCs with integrated RF functionality are also looking for array connectors throughout their full system designs, such as LEO satellites. This has generated an extensive research project providing reference design toolkits and characterization reports for a wide range of array connectors that were originally developed for digital applications. Ultimately this project has focused on redesigning the launch optimization for the RF signals, the break outs/pin outs throughout the connector, and then the stack ups and the laminates used.

## General Information on Samtec Array Products

Samtec offers a variety of array connectors (Figure 1), initially designed and utilized in high-speed digital applications, which feature a range of pitches, stack heights, and configurations for maximum routing, grounding, and design flexibility. With these attributes, the array connectors are considered a great candidate for analog applications, which can require dozens, if not hundreds, of RF signal chains.

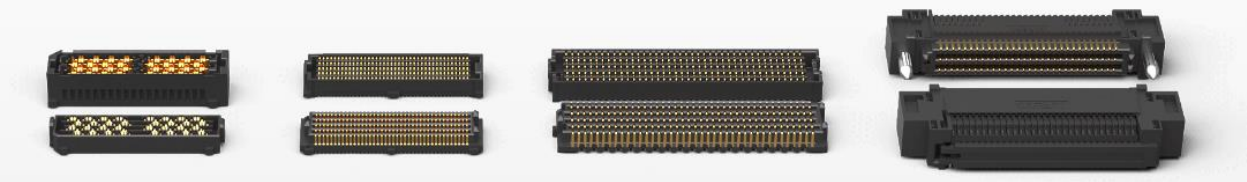

*Figure 1: Samtec Arrays Sample (left to right: NVAX, SEAX, ADX6, SEAX8-RA)*

The interconnects chosen for this application are intended to give customers flexibility with their design in both board real estate and stacking height. Please note that only specific stacking heights were examined and stacks not shown would require additional vetting per application.

## Performance Goals

The design targets identified for this mixed-signal connector array project included:

- Maximize bandwidth for each product
- 100-ohm differential is the target unless otherwise stated
- Differential return loss of -12 dB up to 20 GHz; -15 dB up to max frequency
- Differential crosstalk isolation between channels: -70 dBc to max frequency

These performance requirements were based on the specifications from existing RFSoCs, such as the AMD Xilinx Zynq [2].

## Design Details

In a design optimized for best analog performance, Samtec's NOVARAY (NVAX-7mm) interconnects sit on a 0.8 mm pitch in a vertical mate configuration using pins in-row (Figure 2). The breakout region uses via-in-pad to transition to stripline traces on layer 2, with backdrilling leaving behind an 8-mil stub. ANI I-TERA MT40 is used for core and prepreg fills. The reference plane for the simulation results is 1.2 mm beyond the via transition on layer 2 (Figure 3). In Figure 4, return loss and VSWR plots extracted from the design are shown, where <=–15dB return loss, and <=1.4 VSWR, are observed up to 20 GHz. RF pairs are isolated from each other by predetermined wider ground blade pins and are, therefore, staggered by column. Better isolation can be obtained by terminating neighboring pairs if desired and as shown in Figure 5. Recommended BOR available by request.

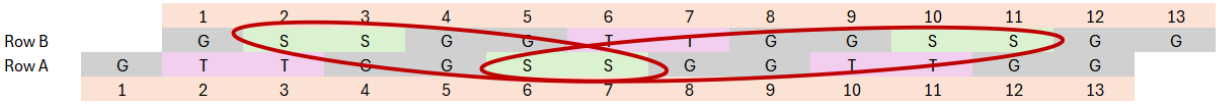


*Figure 2: Signal pin mapping definition. Differential pair 1 (A6 & A7) is used as an observation; all other pairs are aggressors*

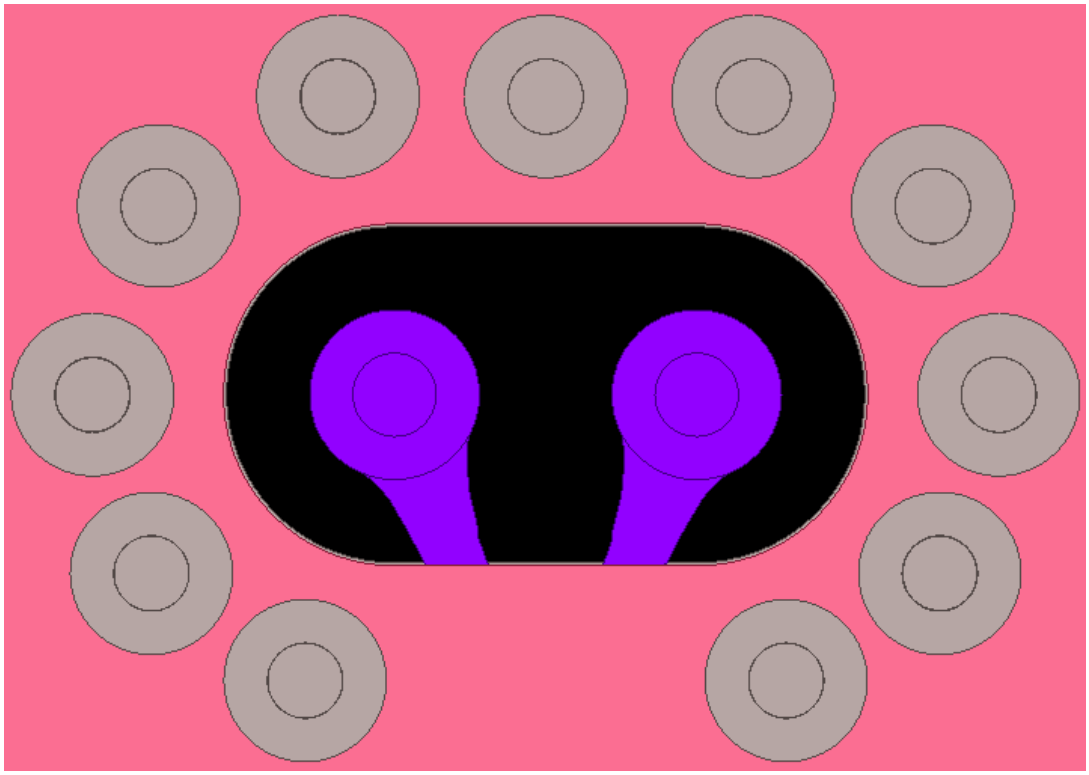

*Figure 3: Optimized BOR design including 1.2 mm trace.*

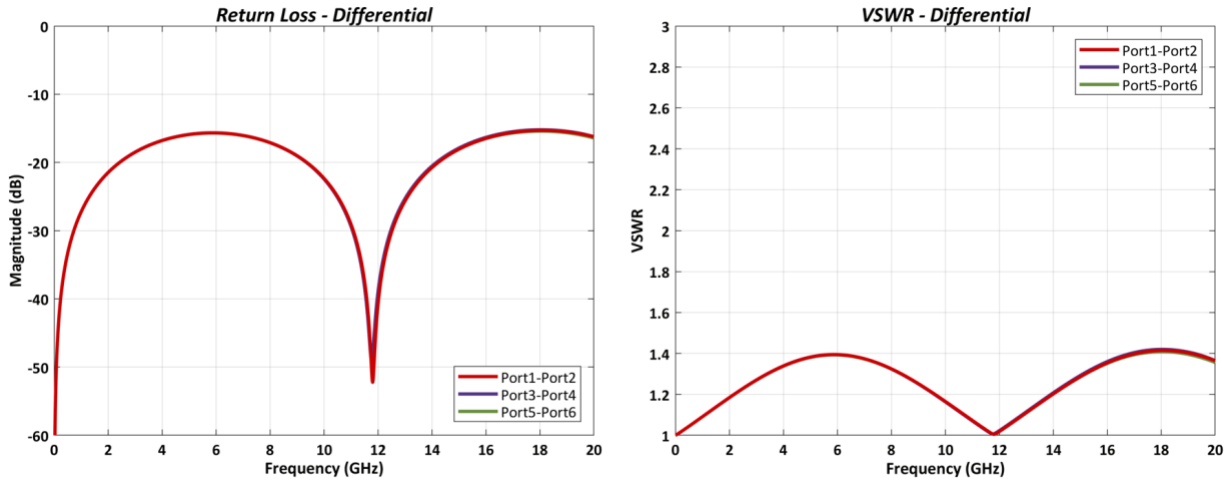


*Figure 4: Differential return loss and VSWR plots of simulated configuration for NVAX-7mm.*

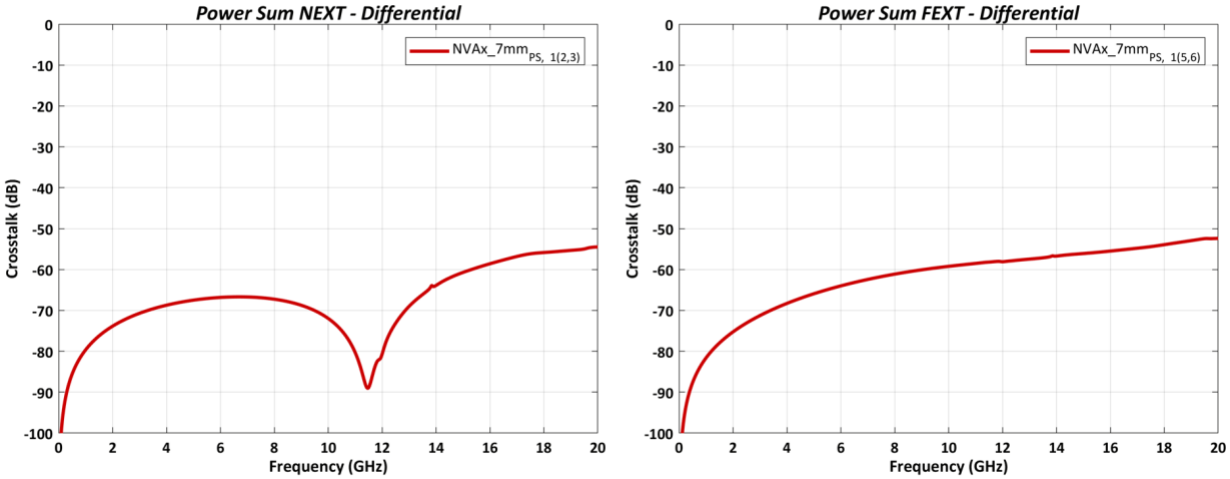


*Figure 5: Differential PowerSum NEXT and FEXT plots of simulated configuration of NVAX-7mm.*

## Resources

[1] 1. M. Zhao. Differential Interfaces Improve Performance in RF Transceiver Designs Analog Dialogue 45-07, July (2011).

[2]. Xilinx Zynq Data Sheet, p. 93.