Array Connectors for Mixed-Signal Multi-Channel RFSOCs up to 8 GHz

White Paper

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Abstract

System on Chip (SoC) implementations with integrated data converters and RF front-end subsystems are being deployed in 5G/6G, phased array radar, SATCOM, FPGA cards, and test & measurement architectures. This paper describes the research, development, simulation, and measurements performed in a project to design the optimal breakout region (BOR) for the use of array connectors that simultaneously carry analog, digital, and/or power signals in an RF environment, as a replacement for traditional compression mount and threaded PCB connectors for RF signals.

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Introduction

Single-chip baseband system on chip (SoC) products with integrated data converters and RF front-end subsystems are being deployed in 5G/6G, phased array radar, SATCOM, FPGA cards, and test and measurement antennas-to-bits architectures. The development of these RFSoC devices challenges the traditional approach of using compression mount and threaded PCB connectors and cable assemblies to handle the RF signals. A simple alternative, using multiple ganged connectors, still puts strain on form factor, weight, and financial budgets, especially as high-frequency RF channel counts increase in these SoC-based systems.

One approach is to take existing technology that was originally designed for high-performance, high-speed digital signaling and adapt it: array connectors. These connectors make it possible to route high-frequency, high-isolation RF signals as well as digital and power signals through a single connector. While these connectors are already proven in high-speed digital systems, using them for RF applications required the development of specific PCB stack ups and launch optimizations in order to achieve the differential crosstalk and return loss performance required for frequencies up to 8 GHz and beyond. This paper describes the research, development, simulation, and measurements performed to design the optimal breakout region (BOR) for the successful use of array connectors in an RF environment.

Background

In pursuit of the latest applications, mixed-signal designers have taken FPGA technology to the next level, adding RF sampling data converter functionality on chip. Traditionally, RF design is a discrete approach, including, for instance, a baseband processor, ADC, DAC, and IF/RF signal chain devices. An RFSoC brings the ADC/DAC and some of the RF signal chain processing into the same package as the FPGA. Examples of these types of devices are the AMD Xilinx Zynq® and Intel® AgilexTM Direct RF-Series, with frequencies up to nearly 8 GHz.

One of the fundamental differences of these new SoC designs is that instead of one or two antennas pathing into a processor, a single chip is now supporting dozens of RF signal chains. This enables new technologies such as 5G MIMO, which also requires beamforming, as well as phased array systems, with a typical phased array having 64 to 128 antenna paths with discrete antennas.

Each of these antennas needs a signal path, which could include an RF interconnect, a switching function (which determines Tx or Rx), up/down converters, IF circuitry, beamforming, etc. Traditionally, designs use simple compression RF connectors which offer excellent performance but do not scale well. They take up valuable PCB space, add cost, and are prone to misalignment in an array form factor. A solution for some simpler designs is ganged RF connectors, offering, for example, a 1x8 or 1x6

configuration. While this is proving to be a very good solution in many applications, it is still too bulky to support RFSoC designs. For instance, a 5G MIMO or phased radar array design could require dozens or hundreds of RF connectors. As a result, the industry requires smaller, denser, high-frequency connectors. Ideally these connectors handle RF, digital, and power simultaneously, linking the motherboard to daughter cards and beyond.

Fortunately, the latest RFSoCs can handle differential RF signals, so this paper will focus on a connector BOR design using differential RF signals. (Single-ended signals were also part of the overall project, and they are mentioned in the future work section.) The industry is moving towards differential RF signaling to achieve the necessary noise performance at higher frequencies. Since differential signals are out of phase with each other, they have a natural noise rejection that single-ended designs do not have, essentially cancelling each other's unwanted EM fields [1].

As compared to single compression-mount RF SMA connectors or ganged ones, an array connector offers a better solution in terms of performance, cost, and real estate for designs using RFSoCs, as long as its pinouts and BOR are optimized for use with RF signals. To date, our work on this array project has supported 4 GHz, 6 GHz, and now 8 GHz mixed-signal FPGA designs.

In addition, designers using these SoCs with integrated RF functionality are also looking for array connectors throughout their full system designs, such as LEO satellites. This has generated an extensive research project providing reference design toolkits and characterization reports for a wide range of array connectors that were originally developed for digital applications. Ultimately this project has focused on redesigning the launch optimization for the RF signals, the break outs/pin outs throughout the connector, and then the stack ups and the laminates used.

Performance Requirements

The design targets identified for this mixed-signal connector array project included:

- 8 GHz bandwidth
- 50 ohm system impedance for single-ended; 100 ohm for differential
- Return loss of -12 dB up to 4 GHz; -10 dB up to 8 GHz;
- Crosstalk isolation between channels: -69 dBc to 4 GHz, -63 dBc to 8 GHz

These performance requirements were based on the specifications from existing RFSoCs, such as the AMD Xilinx Zynq [2].

Design Choices

The major technical challenge facing this project was to successfully send differential RF signals through a digital connector and meet the very high crosstalk isolation requirements of -63 dBc (referred to in this document as "isolation"). All design decisions were made with this benchmark in mind.

FPGAs in RFSoCs are now able to handle differential signals. Therefore, this project proceeded with a differential signal scheme to achieve the -63 dBc target. (One would need many more grounds to use single-ended RF signaling and achieve the targeted crosstalk isolation.)

The first step was to optimize the PCB material for the launch, and experiments were conducted on different laminates to find the best balance of isolation and cost. Although multiple materials were suitable, the team selected Rogers 3003 because it kept the dielectric loss tangent low and was not exotic (or expensive). The typical dielectric constant of RO3003 is 3.00 with excellent stability over temperature and over frequency out past 10 GHz [3].

Once the material characteristics were determined, the next step was to determine the ground fencing (stitching). The challenge was to find the lowest number of grounds that still achieved the isolation specification. A series of experiments were conducted to determine how many grounds were enough to achieve high isolation, and what mapping pattern would keep the signals well isolated while being as dense as possible.

Most RF launches are single ended and mimic a coaxial structure with a via fence. Differential signals need to fit within the via fence. When the ground fences are asymmetrical, it is possible to get better isolation between the differential pairs, particularly at lower frequencies.

We analyzed the near-end (NEXT) and far-end (FEXT) crosstalk between three approaches to determine the best ground fencing configuration in an optimized launch design (Figure 1). All the configurations have similar performance at higher frequency, particularly our frequency of interest of 8 GHz. Applications with lower frequency but higher crosstalk requirements can benefit most from the third ground fencing configuration, which is asymmetrical.

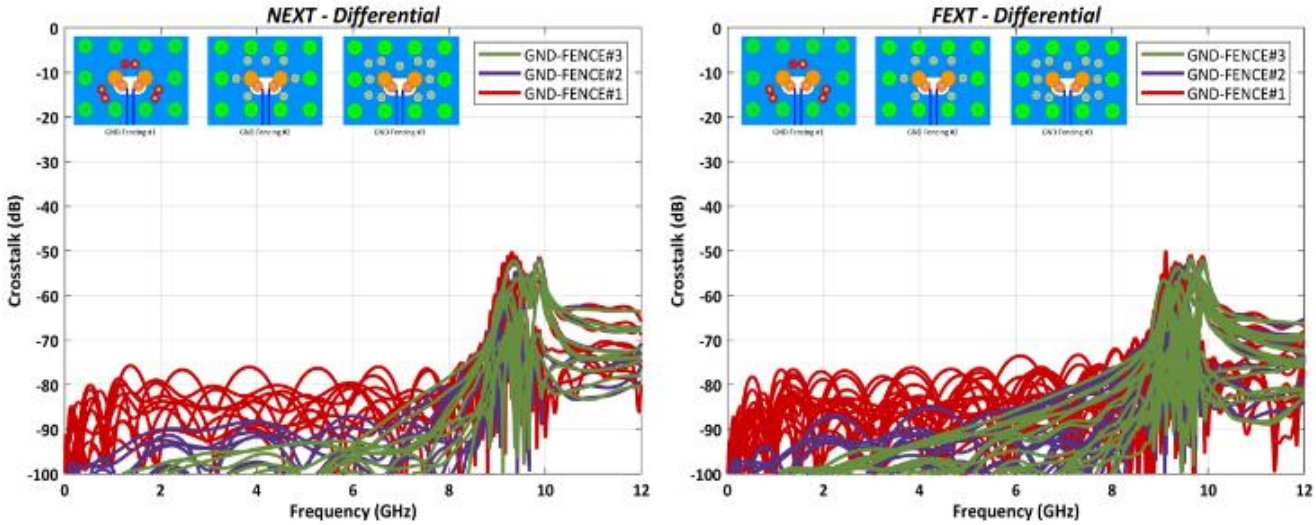


Figure 1: Near-end crosstalk between three ground fencing approaches shows comparable performance at frequencies at or above 8 GHz.

Designing the launch also required a decision between microstrip or stripline [4]. Our work in signal integrity analysis has long shown that stripline is better at isolating signals. (Microstrip adds air and plastic, which can be detrimental to isolation performance.) The challenge here was to get directly down to stripline in this mixed-signal project. The work began with considering previous design wins for digital signals (Figure 2 left), such as a “dogbone” approach (instead of a via that goes directly down through the contact pad, a bit of microstrip trace leads away and then down into the board).

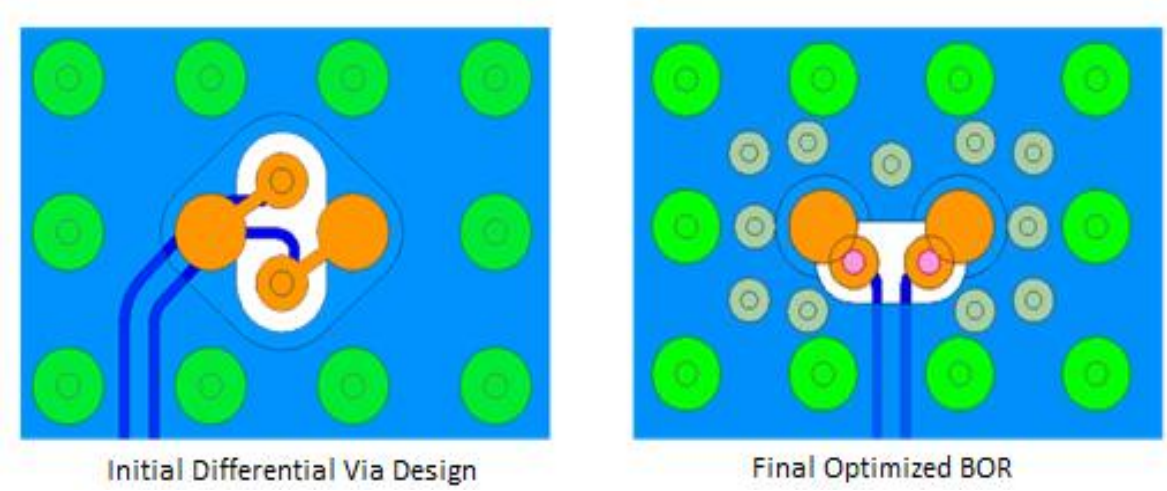


Figure 2: Optimized differential via launch for digital applications (left) vs optimized differential via launch for analog applications (right).

Unfortunately, the microstrip trace collects noise, and in an analog application, it is important to reduce the amount of noise as much as possible. So, the signal needs to get into the board as soon as possible. This led to pulling the signal via in tight to the signal pad, resulting in a “snowman” shaped escape from the solder ball into the board (Figure 2 right).

In an array connector, pin mapping needs to be optimized based on the application. Experimentation in pin mapping revealed that based on natural pin geometry, the signals at the frequencies of note for this project experience more coupling in the vertical position than in the horizontal one.

The vertical position indicates broadside coupling between the signal pin pairs while horizontal position indicates edge coupling between signal pairs (Figures 3 and 4). As a result, for best-case isolation, we resolved to have four grounds in the vertical position and three in the horizontal one. Figure 5 shows side-by-side layout definition in our DUT for those six middle differential RF launches with a pin mapping selection sample for the most optimal solution.

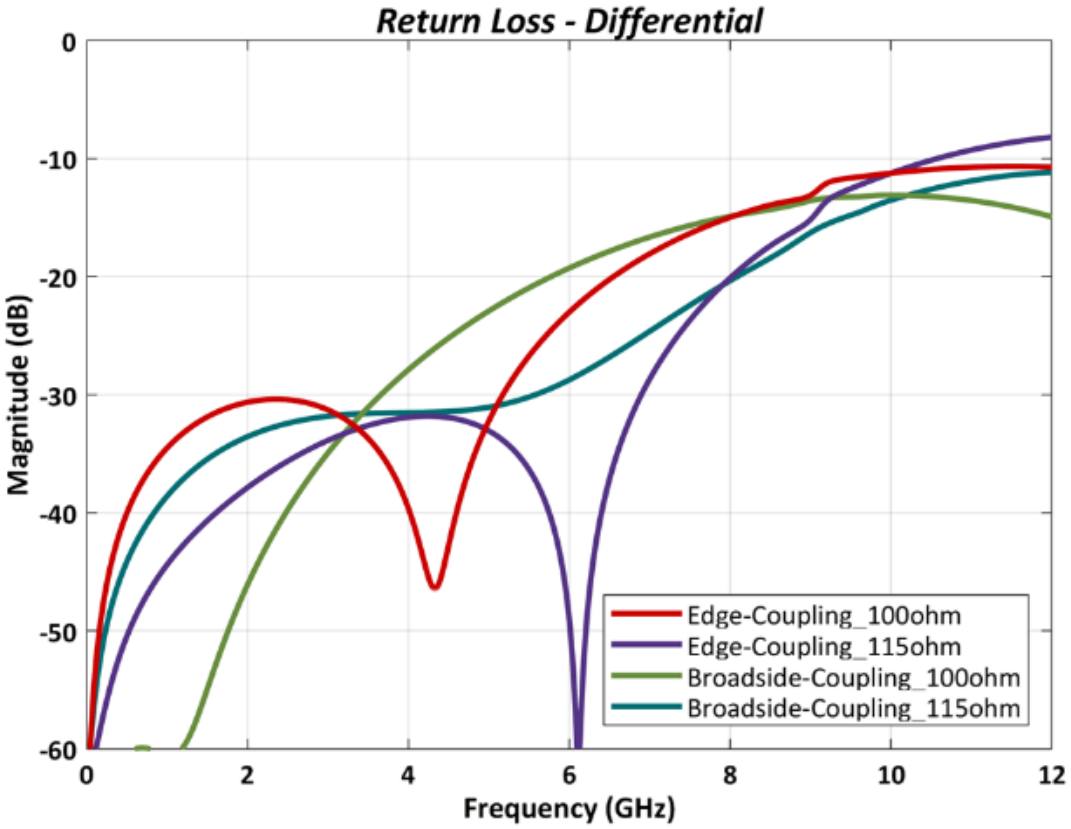


Figure 3: Return loss performance between edge coupling (optimal horizontal: OPTH) and broad side coupling (optimal vertical: OPTV) with 115 ohm and 100-ohm transition trace.

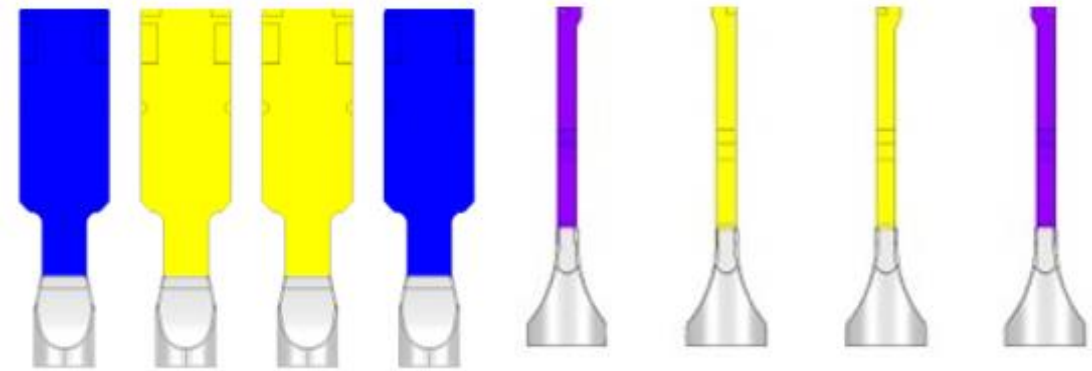


Figure 4: Edge coupling between the signal pair shows optimal horizontal configuration (left) as compared to broadside coupling between the signal pair which shows optimal vertical configuration (right).

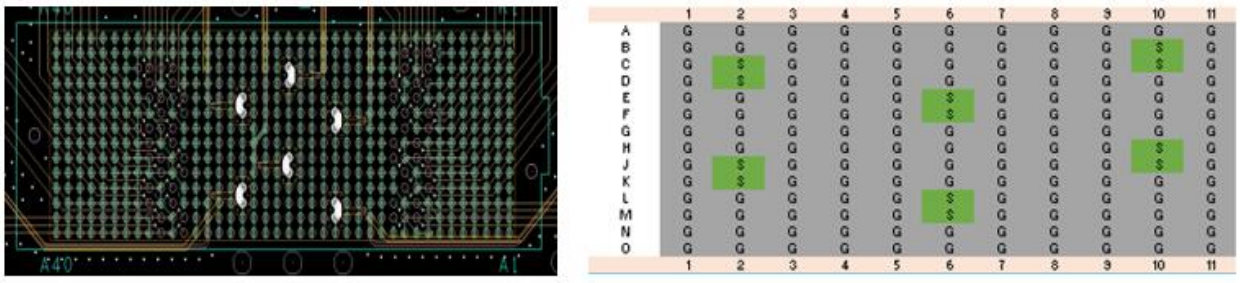


Figure 5: Layout definition artwork (left) and pin mapping selection (right) highlighting ground isolation.

The final design choice in this project had to do with impedance. Traditionally, when a signal is routed into a transition area, it comes in at the targeted system impedance of the transmission path. In most instances for differential signals, this is 100 ohms.

However, when a signal reaches a board transition, that area is very capacitive and can lead to higher reflection due to poor impedance control. So, to offset the capacitance, we increased the impedance to 115 ohms by tapering the traces just before the via. The inductive spike going into a capacitive region causes the changes to balance each other out. As a result, the system shows better return loss because of that “up and down” motion instead of just heading into the transition at 100 ohms and then taking a capacitive dip [5] (Figure 6).

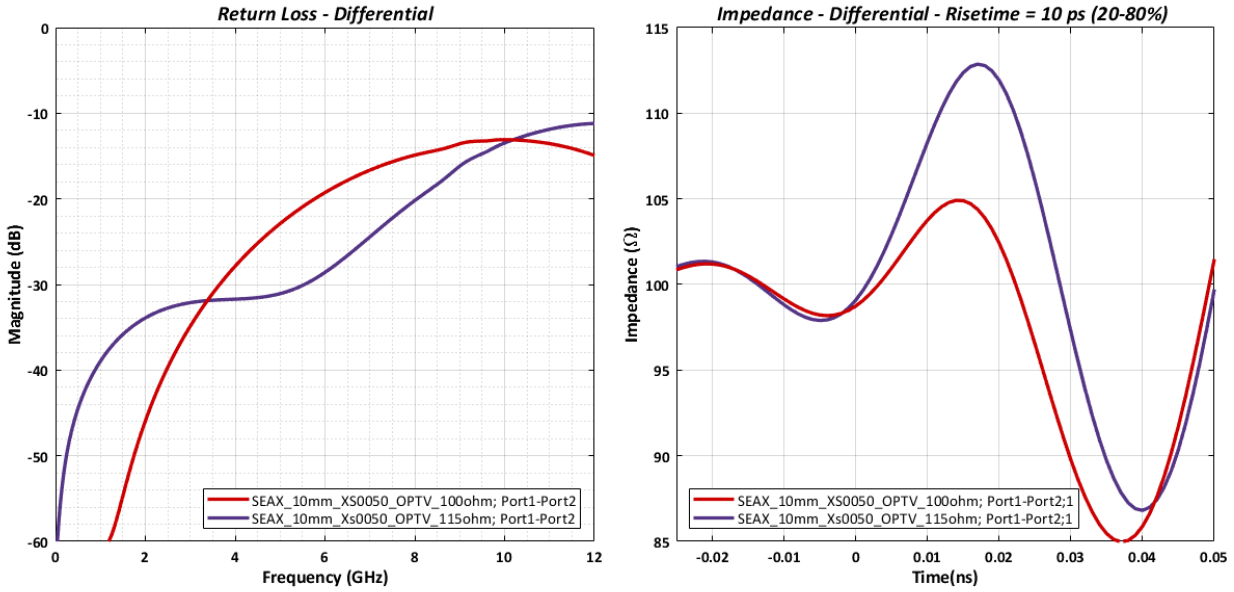


Figure 6: Return loss and impedance plots showing the impact of the 115 ohm lead-in trace, improving return loss from 4-8 GHz.

Analysis and Results

Three key areas of performance indicators for this project were crosstalk isolation, return loss, and VSWR. These characteristics were simulated using ANSYS HFSS and measured using Keysight PNA-L N5225B, 32-port network analyzer, with a test fixture composed of the same board panel of six-layer combo material of Rogers R3003 C and

370HR. All traces on these test boards were length-matched to 56.34 mm (measured from the edge of the pad to the 2.4 mm Samtec connector). The AFR calibration effectively removes 52.87 mm of the test board effects, leaving 3.47 mm of test board trace length effect on both sides of the test boards in the measurement, as shown in Figure 7.

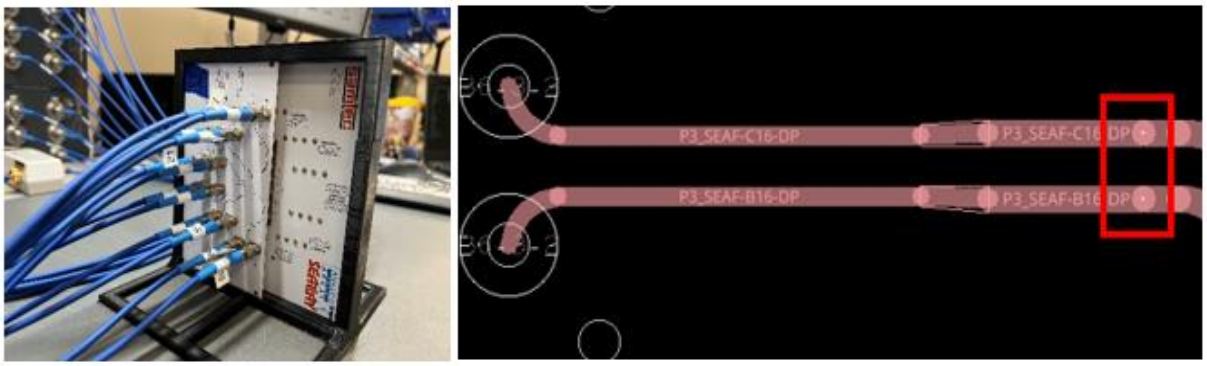
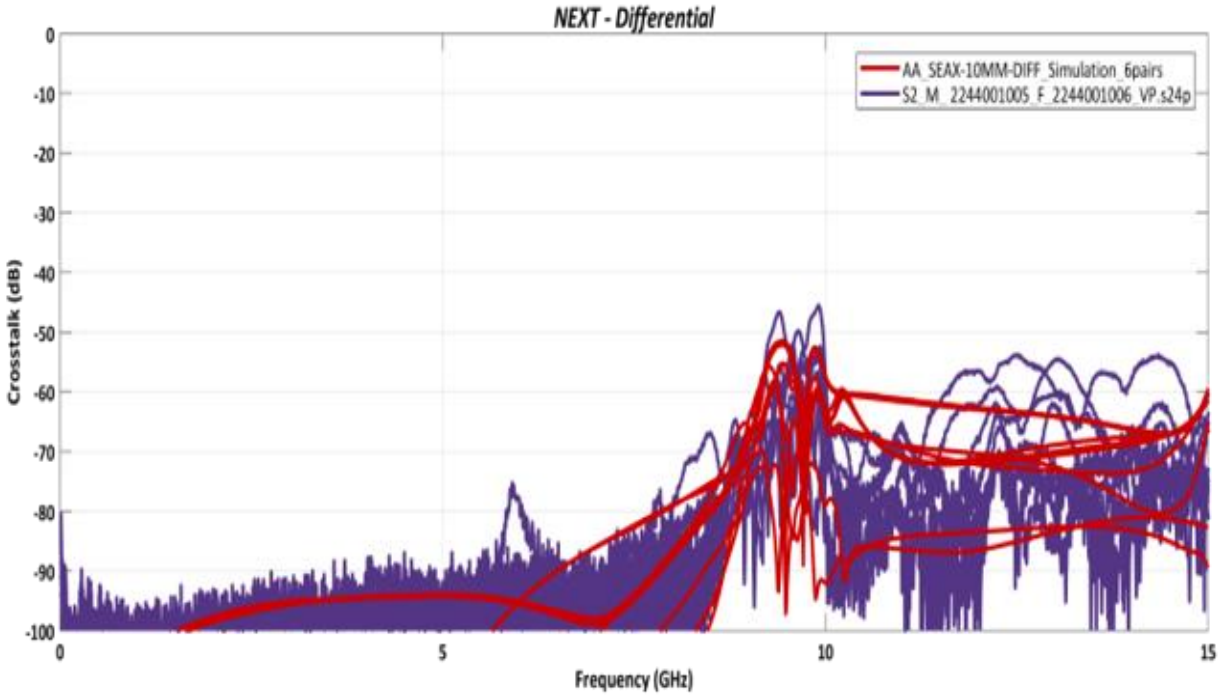


Figure 7: Measurement setup and plane of reference.

Differential crosstalk data for corresponding pin mapping definition from Figure 5 is calculated as a ratio of the input line voltage, also known as active or aggressor to the couple line voltage (sometimes described as quiet victim line) where all measurements are made at both the near-end and far end of the DUT. In Figure 8, we analyzed all six differential pairs for crosstalk, where we maintain -70 dB of isolation up to 8.5 GHz (which is better than our defined performance requirement). This figure shows good correlation between measurement and simulation.



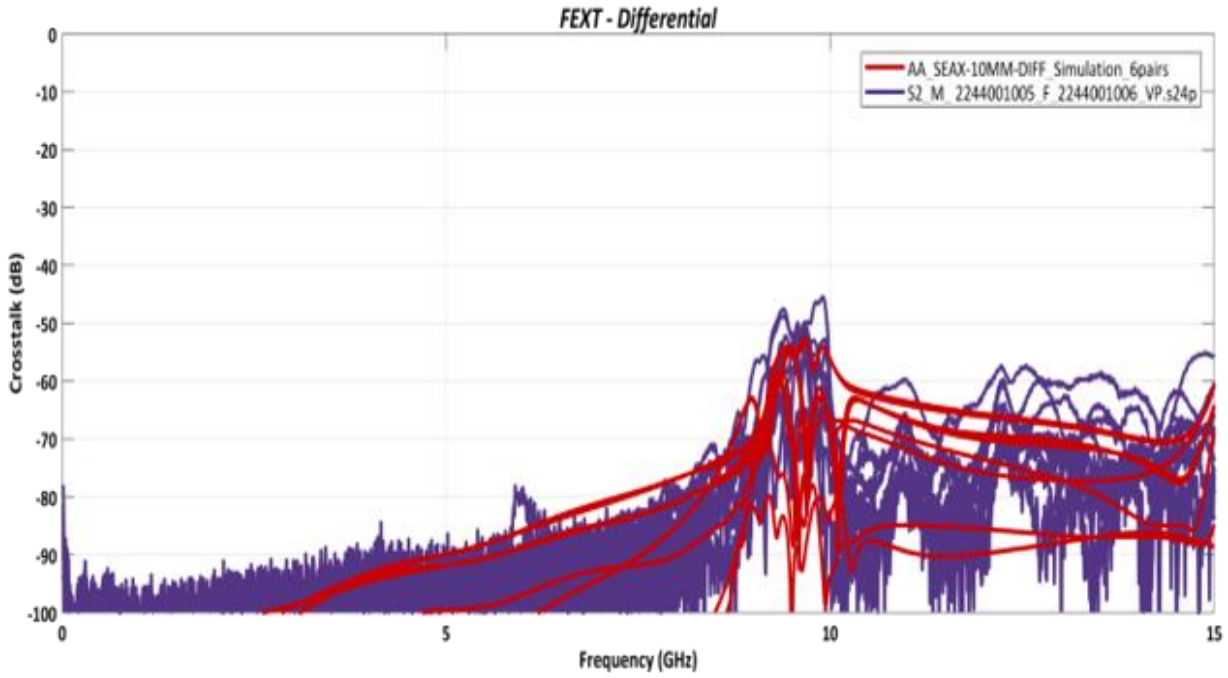


Figure 8: NEXT (top) and FEXT (bottom) measurement over simulation shows good isolation of 70 dB up to 8.5 GHz, satisfying the specification.

Reflection coefficient in our differential linear passive DUT measures the power return "reflected" as a positive value from power incident over power return [6] as seen in (1). By implementing our BOR optimization, we were able to reduce this reflected noise successfully as seen in Figure 9 to satisfy the specification: -10 dB from 0-15 GHz.

$$RL = 10log_{10}\left(\frac{Pincident}{Preturned}\right) \qquad (1)$$

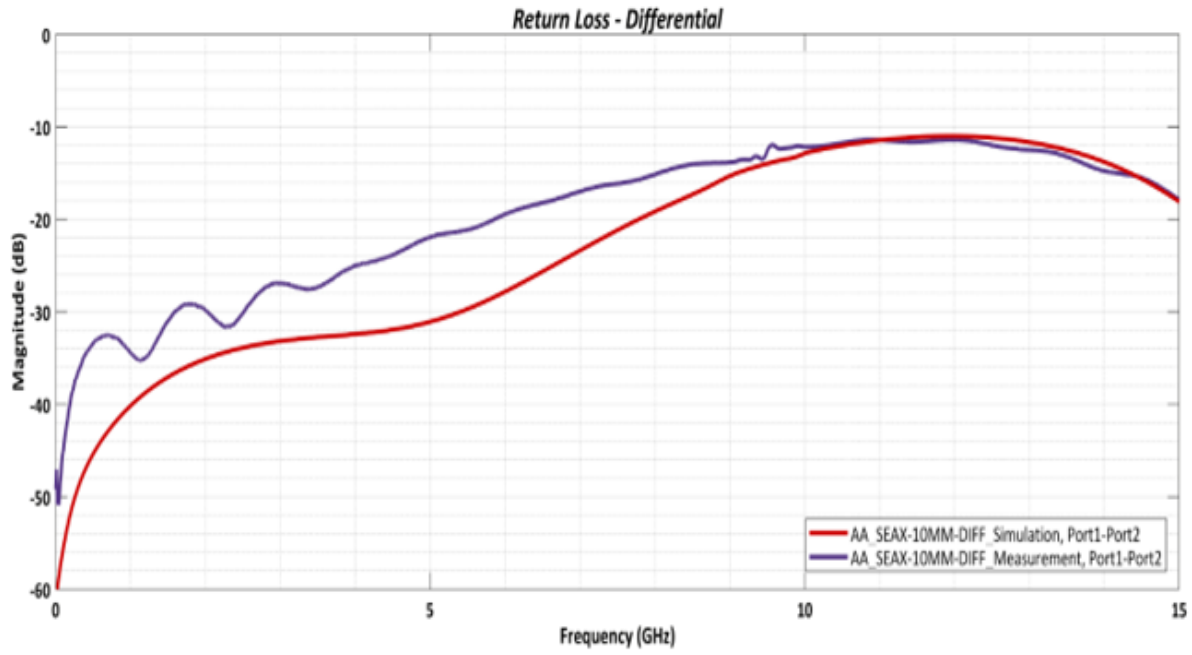


Figure 9. Return loss differential measurement over simulation satisfies the target specification (using a Samtec SEARAY™ connector).

Looking at our DUT as our transmission line, we measured and simulated both incident and reflected waves in our differential RF system to determine the efficiency of power transmission from source to load [7]. In Figure 10, we can determine that a VSWR of 1.45 at 8 GHz, which translates to 0.18 ρ reflection coefficient, 0.15 mismatch due to loss (ML), matching to our Figure 9, a return loss magnitude of 14.72 dB. Values can be determined following (2-4) [6].

$$\rho = \left(\frac{VSWR-1}{VSWR+1}\right) \quad (2)$$

$$\text{ML} = -10log_{10}(1-\rho^2) \quad (3)$$

$$\text{RL} = -20log_{10}(\rho) \quad (4)$$

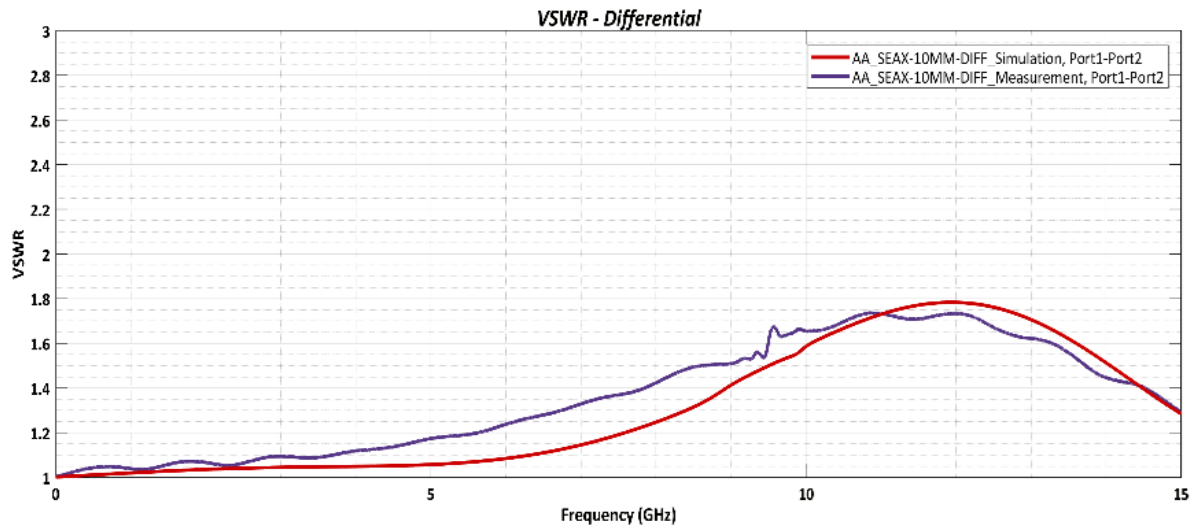


Figure 10: VSWR differential measurement over simulation shows good power transmission efficiency.

Conclusion

The development of RFSoCs has led to a new opportunity to use differential RF signals and achieve greater performance for next-generation applications. There is real value to using an array connector with open-pin-field versatility for these applications because it allows designers to path digital, analog, and power signals through a single connector while achieving excellent isolation and return loss performance. This work took an unconventional approach to an optimized breakout design in terms of materials, launch, connector pin field, and differential ground pattern. Because of that, a currently available 560-pin single array connector can support up to 26 differential RF signals. Another implementation example is a 560-pin single array connector with six differential RF signals plus digital I/O and power [8].

Future Work

The differential signal part of this project has been designed, fabricated, tested, and is now available in a reference design toolkit (including a characterization report). Looking ahead, the roadmap includes development of a single-ended version to provide versatility as well as support for other array connectors in the company catalog. Future work in this area also includes developing a solution to support higher frequencies as the market demands. Analog over Array reference design kits are in development for Samtec SEARAY™, NovaRay®, AcceleRate® HP, LP Array™, and SUPERNOVA™ connectors.

Acknowledgements

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Resources

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