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Design Case Study and Experimental Validation for a 100 Gb/s Per Lane C2M Link Using Channel Operating Margin

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Abstract

The Chip-to-Module (C2M) interface as specified by the IEEE 802.3 Standard Working Group, and currently being updated for higher data rates, implements links that must perform up to 800 Gb/s (8 × 100 Gb/s) within the internet infrastructure physical layer. The design of these channels require multiple engineering disciplines that fused together to create a comprehensive workflow. The standard measurements and specifications such as insertion loss, return loss, crosstalk, impedance profile and eye diagram may no longer be sufficient to ensure compliance as well as interoperability. The Channel Operating Margin (COM) is an emerging Figure of Merit (FOM) that incorporates all active and passive components within the channel to allow performance trade-offs to be made by designers.

While COM is a voltage signal to noise ratio, the C2M uses another related figure of merit, the Voltage Eye Closure (VEC), which is the ratio of eye opening to the amplitude of the electrical output. Since the eye opening is the complement to noise, VEC is directly computable from COM and vice versa as follows.

$$VEC = -20 * log10\left(1 - 10^{\frac{-COM}{20}}\right)$$

$$COM = -20 * log10\left(10^{\frac{-VEC}{20}} - 1\right)$$

Moving to higher and higher in the data rate poses challenges to the applicability of COM/VEC computation for a channel performance design and interoperability compliance evaluation. This paper will characterize a C2M link using advanced simulation and measurement tools to validate the applicability of the design solution explored by COM algorithm. This will confirm its effectiveness without the need to continuously rely on complex, time consuming and expensive measurements, whenever approaching a new C2M channel design.

A typical physical layer channel design, including simulation, measurements and debugging, identifies specific challenges with its subsequent potential solutions evaluated by COM.

Author(s) Biography

Mike Resso is the Signal Integrity Application Scientist in the Internet Infrastructure Solution Group of Keysight Technologies and has over thirty years of experience in the test and measurement industry. His background includes the design and development of electro-optic test instrumentation for aerospace and commercial applications. His most recent activity has focused on the complete multiport characterization of high speed digital interconnects using Time Domain Reflectometry and Vector Network Analysis. He has authored over 30 professional publications including two books on signal integrity. Mike has been awarded one US patent and has twice received the Agilent "Spark of Insight" Award for his contribution to the company. He received a Bachelor of Science degree in Electrical and Computer Engineering from University of California.

Luis Boluña is a Senior Application Engineer for Keysight Technologies. He has extensive experience in both the measurement and simulation of high speed SerDes architectures and backplane designs. His background is Signal Integrity and Mixed Signal Circuit Design. He has worked in Silicon Valley almost 28 years with Agilent, Cisco Systems, Rambus, Microsoft, and National Semiconductor. His research interests are in system design, testability, simulation, and validation of high speed designs.

O.J. Danzy is a Senior RF and Microwave Application Engineer at Keysight Technologies specializing in areas surrounding physical layer test, network analysis, test system design and automation. Most recently he has focused on fixture removal techniques, standards compliance measurement systems and techniques for multiport network analysis applications. He received a Bachelor of Science in Electrical Engineering from Tennessee State University and a Master of Electrical Engineering from Cornell University

Francesco de Paulis was born in L'Aquila, Italy in 1981. He received a Specialist degree (summa cum laude) in Electronic Engineering from University of L'Aquila, L'Aquila, Italy, in 2006, a M.S. degree in Electrical Engineering in May 2008 from Missouri University of Science and Technology (formerly University of Missouri-Rolla), USA, and a PhD degree in Electrical and Information Engineering in 2012 from the University of L'Aquila, L'Aquila, Italy. He is currently a Senior Researcher at the Electromagnetic and Signal Integrity Laboratory, UAq EMC Laboratory, University of L'Aquila, Italy. His main research interests are in SI/PI design on PCB, packages interposers and chips, high speed channel characterization and design, composite materials for shielding and absorption, RF interference in mixed-signal system, TSVs in silicon chips and interposers, EMI and EMC measurement techniques and field transformation, remote fault detection in transmission lines, design of T/R modules and electronic systems for space applications.

Richard Mellitz is presently a Distinguished Engineer at Samtec, supporting interconnect signal integrity and industry standards. Prior to this, he was a Principal Engineer in the Platform Engineering Group at Intel. Richard was a principal member of various Intel processor and I/O bus teams including Itanium®, Pentium®, PCI Express®, SAS®, and Fabric (Ethernet, IB, and proprietary). Additionally, he has been a key

contributor for the channel sections IEEE802.3 backplane and cabling standards, and for the time domain ISI and return loss standards for IEEE802.3 Ethernet, known as COM (Channel Operating Margin) and ERL (Effective Return Loss), which are now an integral part of Ethernet standards due to Rich's leadership. He founded and chaired an IPC (Association Connecting Electronics Industries) committee delivering IPC's first PCB loss test method. Prior to this, Rich led industry efforts at IPC to deliver the first TDR (time domain reflectometry) standard which is presently used throughout the PCB industry. Richard holds many patents in interconnect, signal integrity, design, and test. He has delivered numerous signal integrity papers at electronic industry design conferences.

Antonio Orlandi was born in Milan, Italy in 1963. He received the Laurea degree in electrical engineering from the University of Rome La Sapienza, Rome, Italy, in 1988, and the Ph.D. degree in biomedical engineering from the University Campus Biomedico, Italy, in 2012. He was with the Department of Electrical Engineering, University of Rome La Sapienza from 1988 to 1990. Since 1990, he has been with the Department of Electrical Engineering, University of L'Aquila, L'Aquila, Italy, where he is currently a Full Professor and Chair of the UAq EMC Laboratory. He is the author of more than 350 technical papers. and one book on EBGs. He has published in the field of electromagnetic compatibility in lightning protection systems and power drive systems. His research interests include the field of numerical methods for analysis, modeling and optimization techniques to approach signal/power integrity, EMC/EMI issues in high speed digital systems. In 2017 received the IEEE EMC SOCIETY R.R. STODDART AWARD for outstanding technical contributions on EBG. In 2018 has been awarded with the GOOGLE FACULTY RESEARCH AWARD on "Advanced Machine Learning for PDN Design".

Rick Rabinovich, IEEE802.3 Ethernet voter member, is a Distinguished Engineer at Keysight Technologies, specializing in 3D modeling of electromagnetic structures and PCB stackup optimization for 10G/25G/50G/100G/200G/400 GbE. Former IEEE Communication Society member, Rick was a Senior Principal Design Engineer at Alcatel-Lucent and an Alcatel-Lucent Bell Labs Distinguished Member of the Technical Staff. He has authored several technical articles in the IEEE Communications and EDN magazines and holds two US patents in communications. Rick's previous positions include Hardware Technology Director and Fellow Associate at Spirent Communications, and senior position at Northrop. Rick holds a BS from the Buenos Aires University Engineering College and attended computer post-graduate courses at Cal State Los Angeles, UCLA, and UCI.

Chun-ting "Tim" Wang Lee is a Signal Integrity Application Scientist in the PathWave Software and Solutions group of Keysight Technologies. Tim received his Ph.D in Electrical Engineering from the University of Colorado at Boulder in 2020. His work focuses on understanding the printed circuit board fabrication process and how it impacts the on-board Signal Integrity. Lately, he has been presenting ways to improve simulation and measurement correlation. Recently, he has involved himself in advancing DDR5 and COM analysis

Introduction

The modern internet infrastructure requires an ever-increasing data rate; thus, the standards defined by the IEEE 802.3® and OIF Working Groups are continuously being updated to track the increasing bandwidth demand at all levels of the electrical system design for internetworking products. Different specifications are set by the IEEE 802.3® standard body depending on the interconnect (chip, package, backplane, copper/optical cables) and terminals (chip, optical modules) and length of the channel [1]. The IEEE802.3bs® 2017 standard specifies the Chip-to-Module (C2M) interface that operates at 50 Gbps (Gigabits per second) [2]. The next generation of communication products will operate at 100 Gbps; thus, the definition of the corresponding specifications is underway in the P802.3ck project [3].

The C2M electrical link between a host board and the optical module consists of copper traces or fly over cabling on the host PCB, a high-speed connector, and a short copper trace within the optical module. This link type , the Device Under Test (DUT), will be analyzed in the analysis carried out in this paper.

The link requirements are traditionally characterized in the frequency domain, such as insertion loss and return loss, or time domain such as electrical output eye opening, common mode noise, etc. to achieve the required bit error ratio (BER) prior to the application of the Forward Error Correction (FEC). The transmitter Finite Impulse Filter (FIR) at the transmitter, and the Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalization (DFE) will be used to meet the standard specifications. The design of 100 Gb/s PAM4 (4 level pulse amplitude modulation) C2M channels will require tighter specifications, where an inherent larger degradation of the transmitted signal is expected at double bandwidth, especially in terms of return loss and Insertion Loss Deviation (ILD). A side note, the 100 Gbps rate becomes 106.25 Gbps after the Forward Error Correction (FEC) is included. The Channel Operation Margin (COM) has been demonstrated to be a powerful tool to predict and optimize the pad-to-pad electrical channel performances and has been adopted since the IEEE Std 802.3bj®-2014 for all the latest link standardization at the highest data rate [4]-[6]. An exception is that the testing for a “chip to optical-module” host uses eye diagram parameters such as eye height and eye width.

The evaluation and pass/fail requirement for the channel performance of a 100 Gbps C2M link utilizes the complement to COM called Voltage Eye Closure (VEC) and Vertical Eye Opening (VEO); COM algorithm statistical methods compute VEC and VEO which may also be called Eye Height (EH). The difference between COM and VEC is that the COM computation is at single sampling point whereas the VEC is a statistic measure over a window around the sample point. The purpose of this paper is to provide a practical methodology for design engineers to effectively use COM/VEC algorithms, and reliably confirm the VEC performance by experimental measurements. As a third term of comparison, a channel simulation setup is also built based on the settings extracted from the experimental measurements. In such a way, the quick and effective statistical approach offered by COM through VEC is validated by time domain measurements and full channel simulations. It will also be shown how to reliably derive

the best transmitter/receiver configuration parameters by combining the passive link features with the corresponding optimum equalization settings.

1. The C2M Channel

The C2M DUT considered in this analysis is a Samtec evaluation kit that includes two PCBs interconnected with a Flyover® Twin-Axial cable system. Figure 1 shows the DUT comprised of the two PCBs, and an interconnect cable which is terminated with a NovaRay® connector on the left side and a QSFP-DD connector on the right side [7]-[8]. The flyover cable length is 12". Although several channels were analyzed within a given cable length, this paper will focus only one channel on the 12" cable, since their performances are all similar to each other. The channel s-parameters are measured with a VNA (Keysight P5028A) by setting the calibration planes at the DUT coaxial access points TP0 and TP1a which are highlighted in Fig. 2. The setup in Fig. 2 is used for time domain measurements based on a M8040A BERT source and a sampling oscilloscope. It is worth mentioning that the connection of the C2M DUT to the source and the scope is made possible via additional set of differentially configured instrument grade coax cables; these cables have been selected for its low loss to minimize their impact on the DUT characterization. The differential insertion loss is shown in Fig. 3, after embedding the two sets of cables on both sides of the DUT.

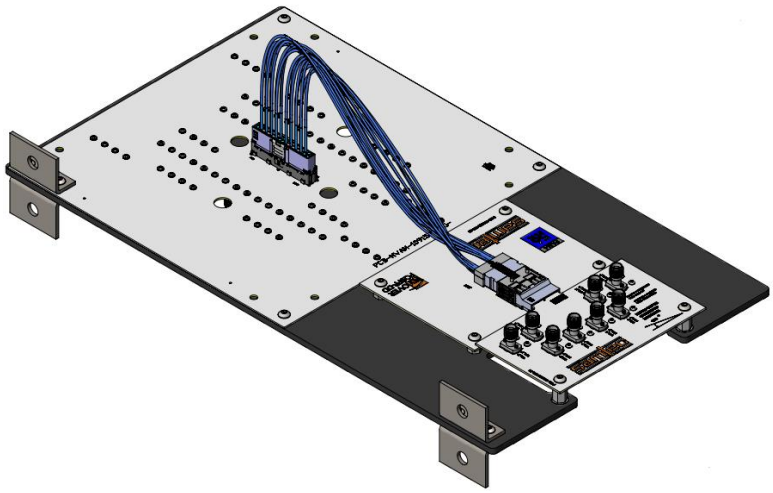


Figure 1. C2M assembly for COM analysis

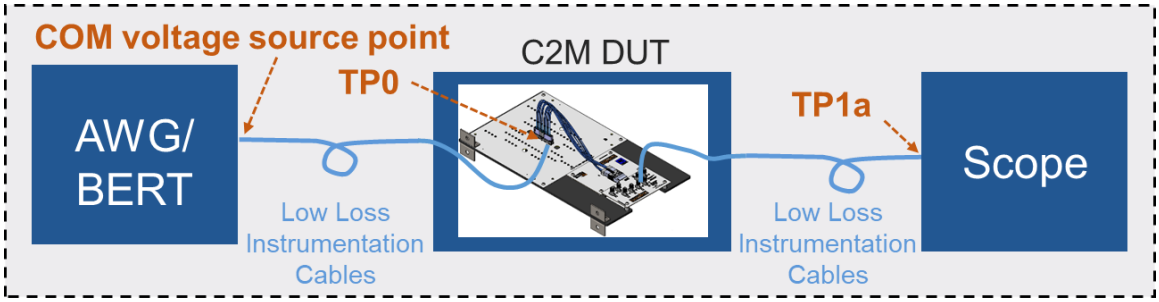


Figure 2. Setup for the time domain measurements

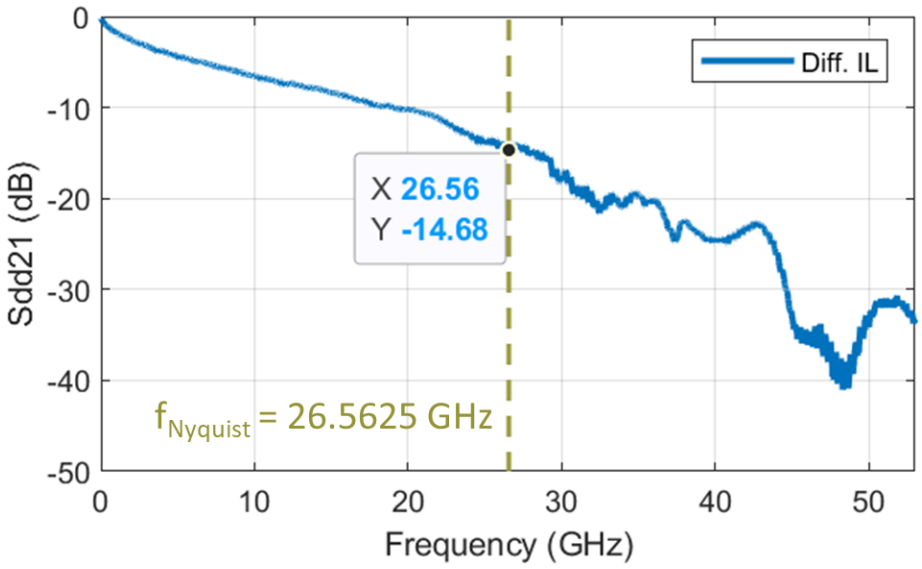


Figure 3. Differential insertion loss of the Cable – DUT (12") – Cable assembly.

2. Measurement Setup to obtain COM parameters

The COM algorithm runs based on a set of input parameters included into a configuration spreadsheet file. Some of these parameters are defined by the IEEE802.3® for the specific interface to which the COM is applied. Other parameters, detailed below, are required to be extracted for the specific transmitter (Tx) host compliance. The direct or indirect measurements of such parameters is discussed in this Section.

2.1 TP0 Setup and Measurements

The M8057B remoted head of the pattern generator output of the M8040A BERT system is attached to an oscilloscope running FlexDCA firmware. The oscilloscope module used is the the N1060A Precision Waveform Analyzer (CDR)module in a N1000A mainframe. One set of the instrumentation cables (0.15 m in length) shown in Fig. 2, interconnects the source-oscilloscope system running at a symbol rate of 53.125 GBd based on a digitally modulated PAM-4 signal. An overview of the setup for the characterization of the TX source at TP0 is shown in Figure 4.

The pattern generator is set to transmit PRBS13Q at 53.125 GBd; the waveform at TP0 acquired by the oscilloscope is processed by the FlexDCA to obtain the pulse response of the TX waveform at TP0. The source at TP0 is calibrated for the best impulse response obtained after an equalization run within the oscilloscope. This is the equivalent to a host signal with no equalization or PRESET1. The N1091CKCA Electrical TX Test Software within the FlexDCA can extract the parameters to be used for the COM analysis. However, the COM algorithm uses an exhaustive search to determine desirable transmitter and receiver equalization. Thus, the expectation, at the time of this paper, is that the VEC/EH from COM may yield a more iteratively optimized result than what is offered in the N1091CKCA application.

The extraction of the TX signal amplitude A_v and rise time t_r is achieved by tuning such factors from a parametric COM analysis aiming at matching the pulse response from

COM and the pulse response extracted from the measured waveform at TP0. The obtained best comparison is reported in Fig. 5 based on A_v = 548.5 mV and t_r = 7.5 ps. Figure 2 illustrates the pulse source injection,

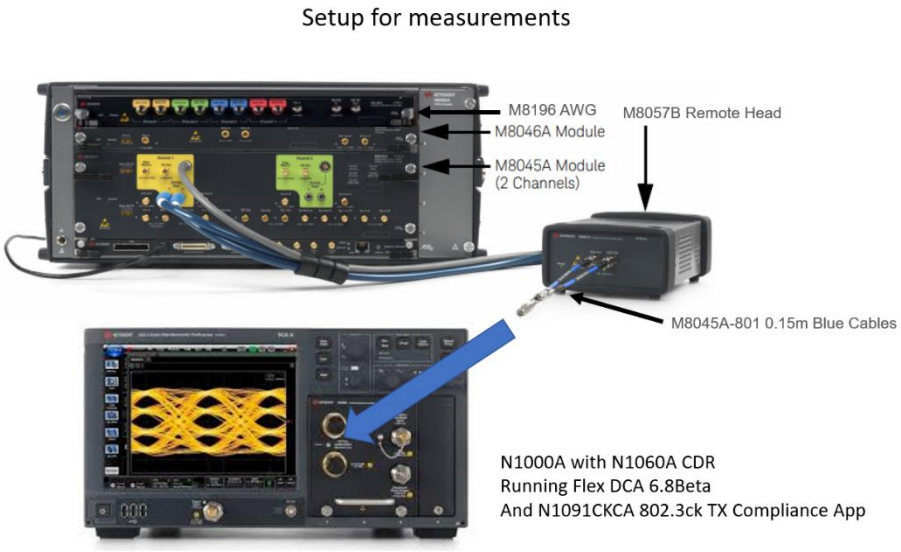


Figure 4. Setup TX characterization at TP0.

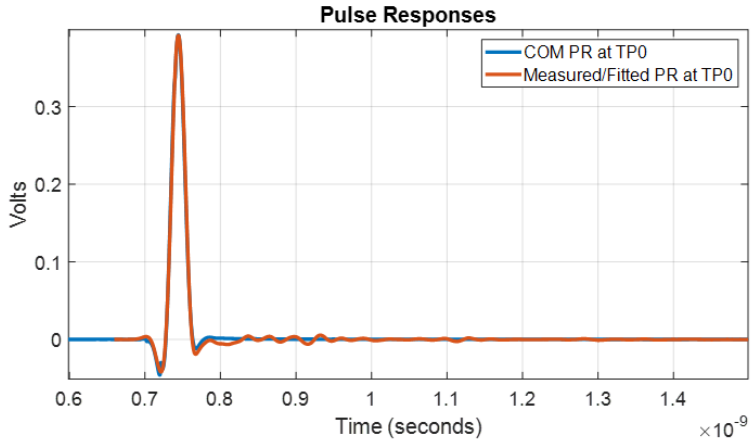


Figure 5. Comparison between pulse response measured at TP0 and the one optimized by the COM algorithm for A_v and t_r.

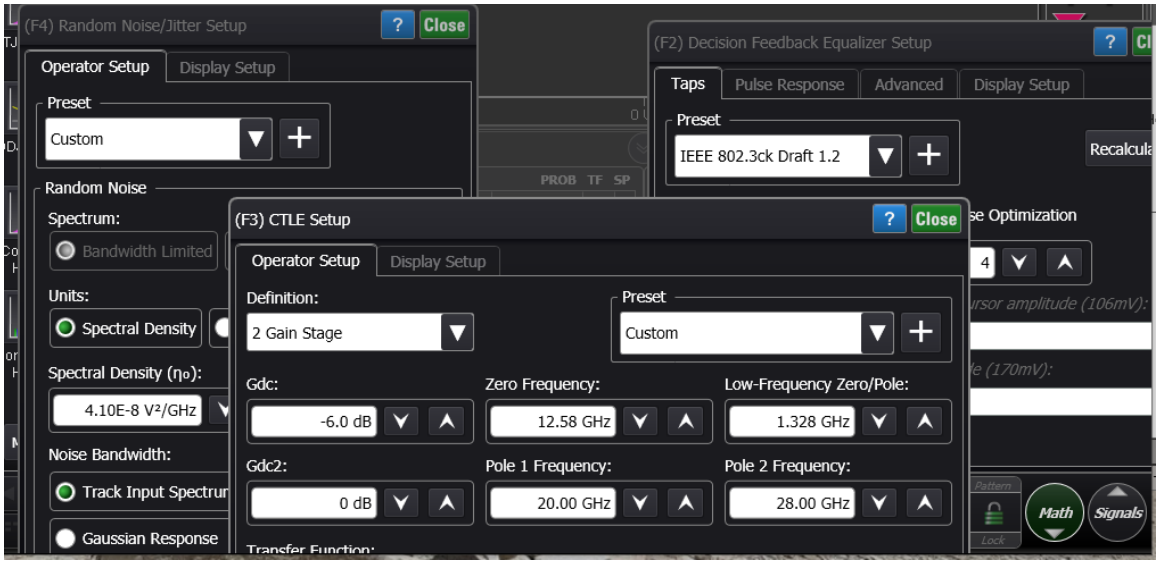
The jitter parameters J3u and J_{RMS} that characterize the TX at TP0 are directly extracted from the measured waveform. These values are used as input to the expressions defined by the 802.3cd Standard (equations136-8 and 136-9) [9], which are being revised according to the current revision 802.3ck, to derive the parameters dual-dirac jitter A_{DD} = 8.4 mUI and random jitter σ_{RJ}= 3.4 mUI. The TX Application N1091CKCA also extracted parameters needed to run COM such as the signal-to-noise distortion ratio (SNDR = 30.55 dB) and the level mismatch ratio (R_LM = 0.95).
Finally, the raw waveform at TP0 is stored for a later usage discussed in Section 3 within the Keysight ADS simulation environment.

2.2 TP1a Setup and Measurements

The second setup consisted of the TP1a configuration as shown in the image below.

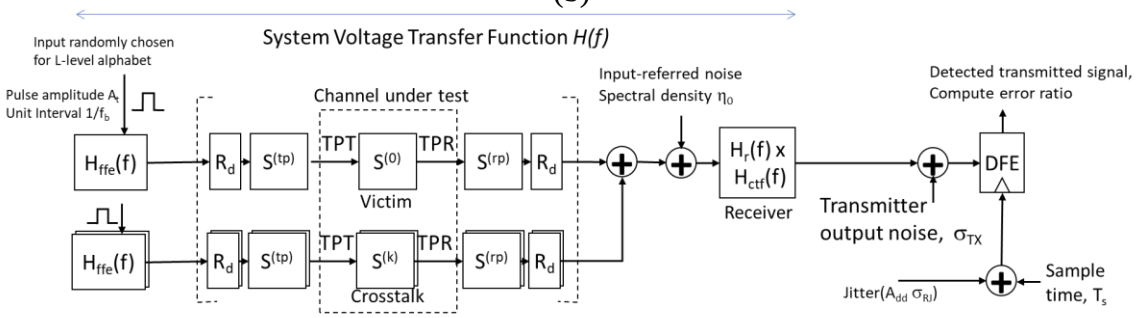
Figure 6. Measurement setup at TP1a: BERT remote Head – 0.15 m instrumentation cable – DUT (based on 12” flyover cable) - 0.15 m instrumentation cable – Oscilloscope.

The reference receiver model is set up based on the mentioned TX Application. A combination of python code controlling the N1091CKCA TX app and the FlexDCA firmware is used to obtain the needed measurements and the corresponding receiver metrics such as VEC and Eye Height (EH). The reference receiver for the measurement consists of setting the system to a Fourth Order Butterworth response with a -3dB cutoff at 40 GHz using the FlexDCA System Impulse Correction (SIRC). The screenshot in Fig. 7a depicts the standard math layout in FlexDCA used by the N0191CKCA TX Application



(a)

(b)



(c)

Figure 7. (a) Setup of the receiver filter. (b) Setup of the noise injection and equalization scheme. (c) Architecture of the COM algorithm

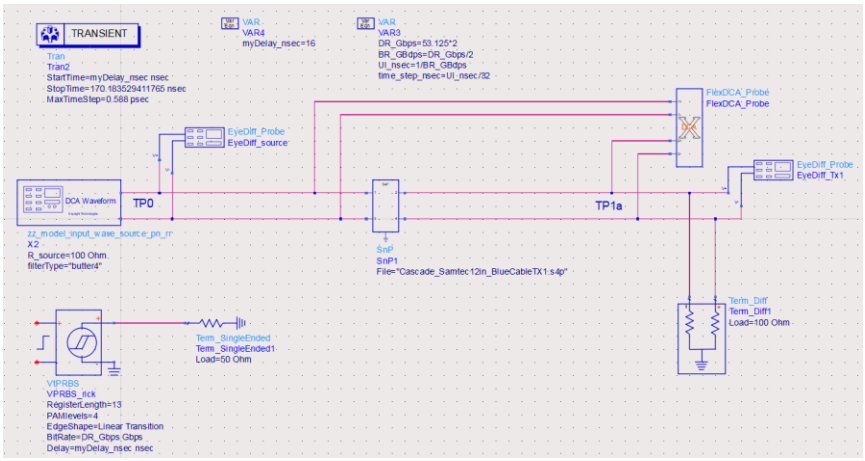
The measurements based on this setup consisted of recording the best vertical eye closure (VEC) while not violating the eye height (EH) requirements as a function of best CTLE settings (g_{DC} and g_{DC2} as defined by Equation 93A-22 in the Standard 802.3bs [2]). A value EH ≥ 15 mV is considered as a reasonable value for minimum EH. A sweep of CTLE (g_{DC}, g_{DC2}) values around those obtained by the COM algorithm, as reported in Section 4, is done according to the RX setup in Fig. 7b. The architecture of the COM algorithm is also shown in Fig. 7c to show the noise η_0 being injected at the receiver before the CTLE and the DFE, as defined in Figure 7b within FlexDCA.

3. Channel Setup in Simulation

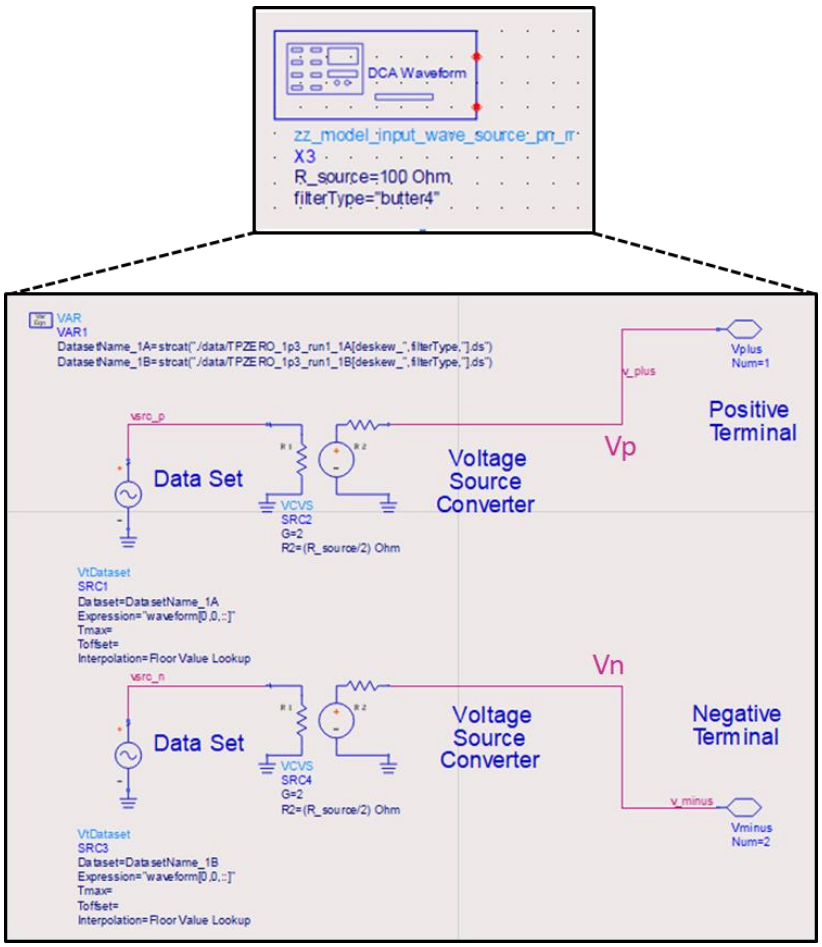
The simulation virtual prototype was created in the Keysight PathWave Advanced Design System (ADS) 2021 environment. The full channel consists of a signal generator model, the DUT, and the FlexDCA probe component. The FlexDCA probe component enables the communication between ADS and Keysight's sampling scope software, FlexDCA. The FlexDCA software used is identical to the one in the scope in Section 2 for the TP1 measurements. Additional termination and a couple of differential probes are also in place. A pseudo-random bit sequence generator was included to synchronize and communicate with the FlexDCA instance. The overall schematic is shown in Figure 8.

There were a couple of options on how to implement the signal generator. The chosen method was to directly import the measured signal out of the pattern generator in the form of single-ended dataset (*.ds) files. This method provides results that could have better correlation to the lab results and COM. However, in a typical project, the designer could use the manufacturer's provided IBIS-AMI Tx/Rx models to run a system simulation. In that case, an IBIS-AMI instance would have been required to create a "super clean" signal coming out of the pattern generator and re-creating the required noise configuration at the IBIS-AMI model to match the COM configuration.

The raw waveforms measured at TP0 made by the positive (Vp) and negative (Vn) single-ended branches of the differential signal from the BERT, as discussed in Section 2, are used within the signal generator circuitry as detailed in Figure 8b. The output waveform corresponds to TP0 in Figure 2. Because the instrumentation cables are already embedded into the TX source, the DUT channel in Figure 8a is made by the assembly S-parameter datasets of the C2M device in Figure 1 and one set of the 0.15 m instrumentation cable to reach TP1a in Figure 2. The signal generator is a hierarchical structure organized as shown in Figure 8b. There are two voltage sources. The Time Domain Waveform Defined in Dataset (VtDataset) instances imported the measured single-ended data set files. Two Linear Voltage-Controlled Voltage Source (VCVS) instances amplified the signal by two to compensate for the voltage divider once they are connected to the load. The VCVSs also function as a source impedance terminator, offering a tunable source impedance. The source termination was 100 Ω. The output of this signal generator is a balanced differential output that will go in the DUT.



(a)



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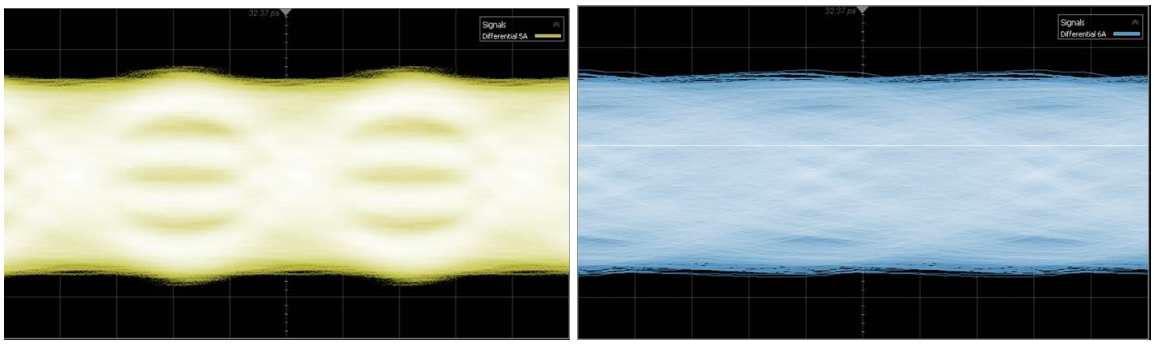


(c) (d)

Figure 8. (a) Overview of the complete channel simulation schematic. (b) Detail of the signal generator for accurately importing the measured waveforms at TP0. (c) Eye diagram at TP0, (d) eye diagram at TP1a.

The simulation period is selected to define the overall run time equal to 8191 clock periods, corresponding to the PRBSQ13 pattern length used in the measurement.
The waveform after the DUT is fed into the FlexDCA probe. This allows us to access the same measurements and waveform processing done by the N1091CKCA TX app within the oscilloscope.
The Time-Domain Pseudo-Random Bit Sequence Voltage Source (VtPRBS) is an auxiliary device that provides the register length and modulation to configure the FlexDCA instance for proper simulation setup. This element would not be necessary in a typical design application since the IBIS-AMI model would include this function.
The eye diagrams at TP0 and TP1a are also reported in Fig. 8c,d; they are completely closed, as expected due to the high data rate; moreover, the TP0 eye diagram is also affected by the mismatch that occurs between the source impedance and the DUT, whereas the worse eye diagram at TP1a is due to the channel losses.

3.1 FlexDCA Scope Instance Configuration

Similar to the actual scope, the FlexDCA TX Application is configured to apply the COM settings (noise and equalization) at the signal reaching TP1a. Settings for the math layout are the same as discussed in section 2.2. The reference RX model is reported in Fig. 9; this configuration is exactly the same as the one in Figure 7b. Each one of the blocks, the Random Noise/Jitter, CTLE, and DFE, was configured to match the instrument setup. The FlexDCA Jitter/Noise configuration window was also configured to match its lab counterpart.

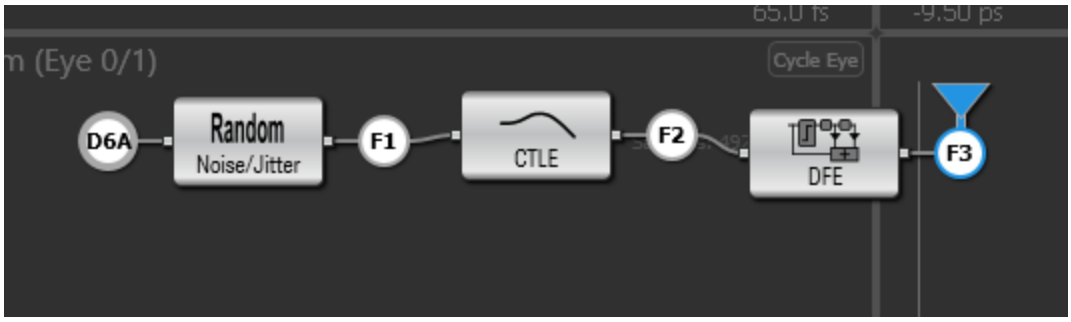


Figure 9. RX configuration within FlexDCA for noise injection and CTLE and DFE equalization.

4. Eye Metrics Validation

This Section describes all results obtained by the direct measurement at TP1a and the subsequent waveform processing according to the receiver defined in Section 2.2. These measurement results are directly compared to the corresponding values coming from the COM algorithm whose configuration file is populated by the parameters directly measured at TP0, and from the channel simulation detailed in Section 3. The version of COM employed herein is the most updated one (v3.1) publicly available and continuously being updated by the 802.3ck Working Group [3].

4.1 VEC and EH: COM vs. Measurements vs. Channel Simulation

The optimization of CTLE and FFE settings at TP1a are implemented in accordance to the RX setup in Figure 7b.The overall measurement system in Figure 6 led to the VEC results in Fig. 10, shown as function of the tested pairs (g_{DC}, g_{DC2}). The best solution in terms of VEC/EH is obtained by the combination reported in Table I. The units of g_{DC}, g_{DC2}, and VEC are in dB, whereas EH is in mV.

The final comparison among the three methodologies for evaluating the channel performances is reported in the subsequent rows of Table I.

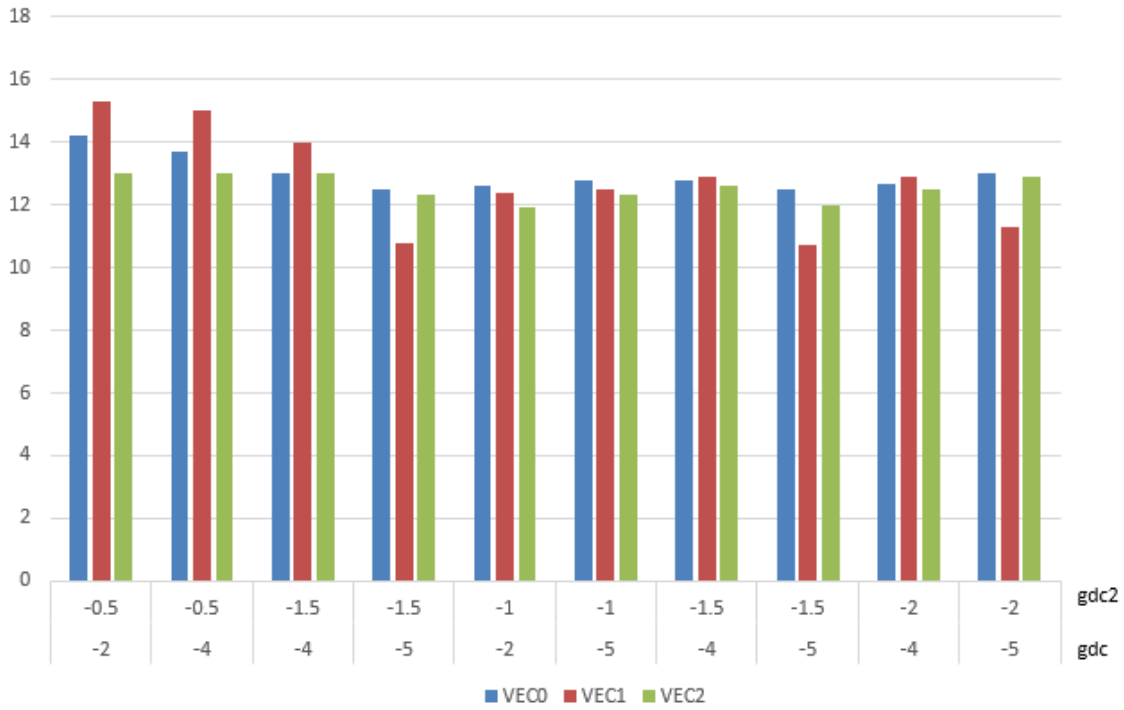


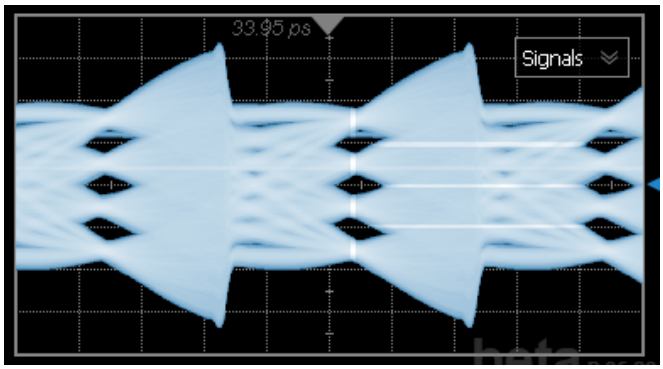
Figure 10. Analysis subset of VEC results while changing the variable CTLE settings (g_{DC} and g_{DC2}) during the measurements at TP1.

Table I

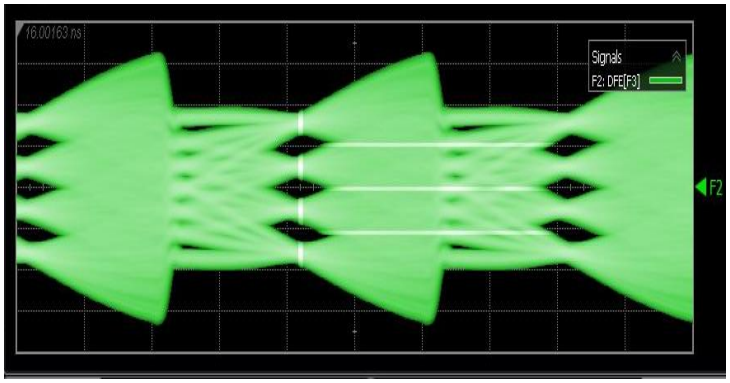
	g_{DC}	g_{DC2}	VEC0	VEC1	VEC2	EH0	EH1	EH2
Measurement 1	-5	-1	12.5	10.7	12.0	19	23.6	20.2
Measurement 2	-4	-2	12.7	12.9	12.5	18.8	18.7	19.4
ADS Simulation	-4	-2	11.2	10.5	10.4	22.8	24.7	25.0
COM [#]	-6	-2	9.43*			24.71*		

[#] The COM calculation is based on the COM script version 3.1 available at [3]
* COM only reports worst VEC and EH values

Differently from COM, both the channel simulation and the measurement setup are able to output the waveforms after the DFE. They are shown in Fig. 11.



(a)



(b)

Figure 11. (a) output eye diagram after DFE from (a) the ADS channel simulation, (b) the measurement and oscilloscope processing by the FlexDCA.

Discussion and Conclusions

One advantage of a figure-of-merit like COM is that thousands of variable combinations within a working TX-interconnect-Rx channel can be considered and datamined for performance insights. This is very difficult to do within a single domain analysis such as frequency or time domains. By creating a foundation for SERDES, connector, and PCB interconnect designers to have a common test strategy based on COM and related figures of merits, the overall ecosystem design team can make the margin trade-offs necessary in order to optimize each subsystem to achieve the best channel cost-performance.

This paper presents experimental work to show the scope and complexity related to developing this much needed compliance metrics. There are many moving parts within the measurement and simulation tools to achieve complete hardware/software correlation, as one can see from the detail inside this manuscript. However, the practical work carried out in this paper demonstrates a framework for experimentally testing compliance of transmitters for the IEEE® 100 Gbps PAM-4 C2M interface as being developed in IEEE® P802.3ck task force or, equivalently, in similar 112 Gbps PAM-4 OIF VSR specification work. The authors successfully displayed one potential path to achieve a comprehensive workflow to assure compliance as well as interoperability to be applied at both experimental and channel simulation levels. This included identification of proper test points, the methods for determining the parameters for COM simulation like

SNR_Tx, R_LM, jitter, voltage drive, and transition time, and to highlight how the various equalization techniques need to be handled for targeting a C2M compliance. The work described in this paper assumes the DCA Waveform generator as TX source for the C2M interface, thus making readily available the test point TP0. This may not be the case for a practical TX host design that may be characterized only at TP1a. However, the practical guidelines highlighted herein for extracting A_v, t_r, A_DD, sigma_RJ, R_LM, and SNDR can be readily applied either at TP0 or at TP1a, depending on which one is suitable for testing. The outcome of this framework is highlighted by the comparisons in Table I and in Figure 11, where good agreement is obtained in terms of VEC/EH, for the measured and simulated eye diagrams Minor differences in the configuration of the CTLE between these two methods is related to the limited frequency bandwidth of the DUT model. Since COM performs an extensive equalization search slightly better VEC/EH are expected with respect to the corresponding values obtained experimentally.

The authors recognize that much more work is required to fully implement the Channel Operating Margin test process as defined by IEEE 802.3 Working Group. However, the authors are confident that many insights can be gained by following the workflow as depicted in this manuscript. Is our work finished? It is definitely not. Have we encouraged and peaked at least one signal integrity engineer to pursue and contribute to this overall industry test and measurement challenge? We certainly hope so.

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