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Specification-based IBIS-AMI model PCIe 5.0 32GT/s

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Abstract

We will demonstrate how to convert electrical specification documents for PCI Express (PCIe) 5.0 and generate an equivalent IBIS-AMI model to represent the significant electrical signaling behaviors. Key signaling behaviors on transmitter is the 3-tap feed-forward equalization (FFE). On receiver, the key specification behaviors are continuous-time linear equalizer (CTLE), decision-feedback equalizer (DFE) and clock-data recovery (CDR). The conversion from specification jitter referenced at transmitter to separate transmitter & receiver components will be shown. The IBIS-AMI model will be setup in end-to-end channel simulation to demonstrate the system-level performance and how it matches with specification assumptions.

Author(s) Biography

Todd Bermensolo is an Application Engineer at Keysight Technologies, in their Customer Success Acceleration service team. Prior experience at Intel Corporation in the Enterprise Platform Signal Integrity team. He received his BS degree in EE from University of Idaho in 1998 and his MS degree in EE from University of Illinois in 2005.

Hansel Desmond Dsilva is a Staff Signal Integrity Engineer at Achronix Semiconductor Corporation. He received a Master of Science degree (with thesis) in Electrical Engineering from San Diego State University in 2015 and a Bachelor of Engineering degree in Electronics and Telecommunication Engineering from Don Bosco Institute of Technology, Mumbai (Bombay) University in 2013. He believes in innovating through collaboration and never shies from listening to another's thought process in challenging his own.

Adam Gregory is a Signal Integrity Engineer at Samtec. He is involved in modeling and analysis of high-speed differential signaling channels. He received a BSEE and MSEE at the University of South Carolina.

Michael Mirmak is a Platform Applications Engineer with Intel's Data Center Group, supporting signal integrity (SI) modeling and analysis. He has been involved with SI since 1996. He is a past chair of the IBIS Open Forum, the organization that manages the I/O Buffer Information Specification and the Touchstone specification.

Background

With mainstream interface specifications in the 5th generation, the challenges have never been greater for implementing standards like PCIe 5.0 [1] at 32 GT/s. Form factors in datacenters and high-performance computing are unchanged but supporting same platform topologies at faster data rates demands more design complexity with smaller margins. Translating electrical specification documents to system-level simulations is not easy and requires combinations of models for silicon, interconnect and jitter assessment. Behavioral modeling standards like IBIS-AMI [2] provides an interoperable format to capture specification assumptions for silicon that allows platform developers to get a first look at their system-level simulations before silicon vendor IP models are available, or to compare those silicon vendor IP models to electrical specifications.

Utilizing IBIS-AMI model format to support a top-down, behavioral design methodology, the static electrical specification documents can be converted to executable behavioral models for end-to-end system level simulation. First, the hundreds of pages in electrical specification will be narrowed down to the relevant material for IBIS-AMI modeling. Next, the key transmitter (Tx), receiver (Rx) and jitter components will be captured. For Tx in PCIe 5.0, there is the 3-tap feed-forward equalizer (FFE). For Rx in PCIe 5.0, there are continuous-time linear equalizer (CTLE), decision-feedback equalizer (DFE) and clock-data recovery (CDR). To optimize the Rx equalization, the system pulse response is used to minimize post-cursor ISI strength to near zero value (while staying positive). PCIe 5.0 jitter referenced at Tx, which will be separated into Tx & Rx components to support IBIS-AMI simulation analysis flow.

The result will be Tx & Rx IBIS-AMI models that can support low bit error ratio (BER) simulation analysis. Equalization values and channel conditions are varied to show performance vs. specification limits. The results are a simulation-based approach to utilize electrical specification details. Insights can be gained in platform-level simulation results before vendor-based models are available.

PCIe 5.0 Specification Overview

PCI Express a high performance, general purpose I/O interconnect. The 5th generation, or PCIe 5.0, operates at a signal transfer rate of 32 GT/s. To support backward compatibility, it shares many similarities to with prior generations like same connector pinout, Tx EQ presets, Tx Voltage and Jitter parameters and same approach to Tx and Rx testing. Some key updates moving to PCIe 5.0 are updated Rx characteristics to support 32 GT/s such as CTLE frequency tables, 3-tap DFE and CDR frequency behavior. The informative insertion loss budget is -36 dB at 16 GHz.

Overview of simulation with IBIS-AMI

The IBIS standard was first released in 1993 through the IBIS Open Forum. The core functionality focused on analog electrical modeling of Tx, Rx and packages. With IBIS Version 5.0 in 2008, the algorithmic modeling interface (AMI) support was added which expanded the modeling capability to include discrete time processing behaviors or

algorithmic modeling. Examples of types of AMI modeling are transmitter equalization, receiver equalization and clock recovery circuits. There are two fundamental simulation flows supported by IBIS-AMI: a statistical simulation flow for models with LTI equalization algorithms; and a time-domain flow which permits nonlinear or time-variant equalization characteristics [3]. See Figure 1 for reference flow.

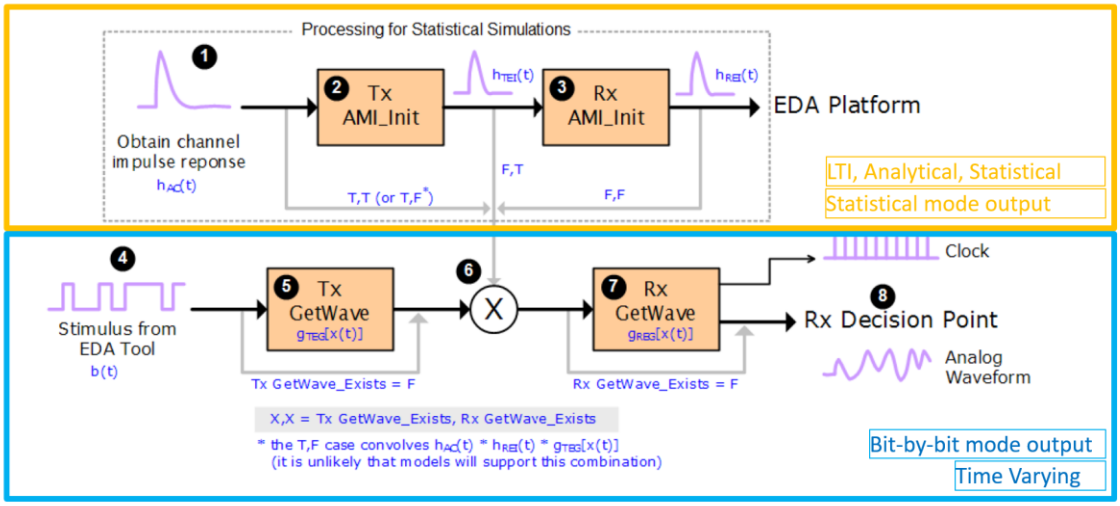

Figure 1. The IBIS-AMI statistical and time-domain reference flow [3]

IBIS-AMI Models: eesof_pcie5_tx/rx_adapt

The following is a description of the PCIe 5.0 specification-based IBIS-AMI models.

The Tx IBIS-AMI is an LTI model (Init_Returns_Impulse=True). Tx input parameters are transmitter jitter components (Tx_Rj, Tx_Dj, Tx_DCD) and the 10 Tx EQ presets as defined by specification (tx_preset).

The Rx IBIS-AMI is a NTV model (GetWave_Exists=True). Rx input parameters are Ignore bits (In bit-by-bit mode, defines how many bits to use for Rx adaption phase before eye-margin data is captured), receiver jitter components (Rx_Rj, Rx_Dj, Rx_DCD) and equalization controls for CTLE and DFE:

- rx_ctle_adapt_enable. Set to 1 for Rx CTLE adaptation. Set to 0 for manual control.
- rx_ctle_dcgain. DC Gain parameter for CTLE. As defined by spec, can vary from -5dB to -15dB in 1dB increments. Used only when rx_ctle_adapt_enable=0 (adaptation disabled).

Also available from Rx IBIS-AMI model is output parameters that provide visibility into the CTLE and DFE automatic adaptation:

- rx_dfe_tap1_limit. View dfe tap1 limit measurement as it complies with h1/h0 < 0.8 spec requirement.
- rx_dfe_tapN_value. View DFE coefficients as they adapt during the simulation.
- rx_ctle_dcgain_value. View CTLE DC Gain value, either final adaptation or what was manually selected.

As a performance benchmark, running a Tx IBIS-AMI connected to S-parameter channel in followed by Rx IBIS-AMI in a single CPU laptop runs 100k bits in 50 seconds. See Figure 2 for simulation for when Tx is LTI and Rx is NTV. The highlights paths show how AMI_Init processing is used for Tx and AMI_Getwave for Rx.

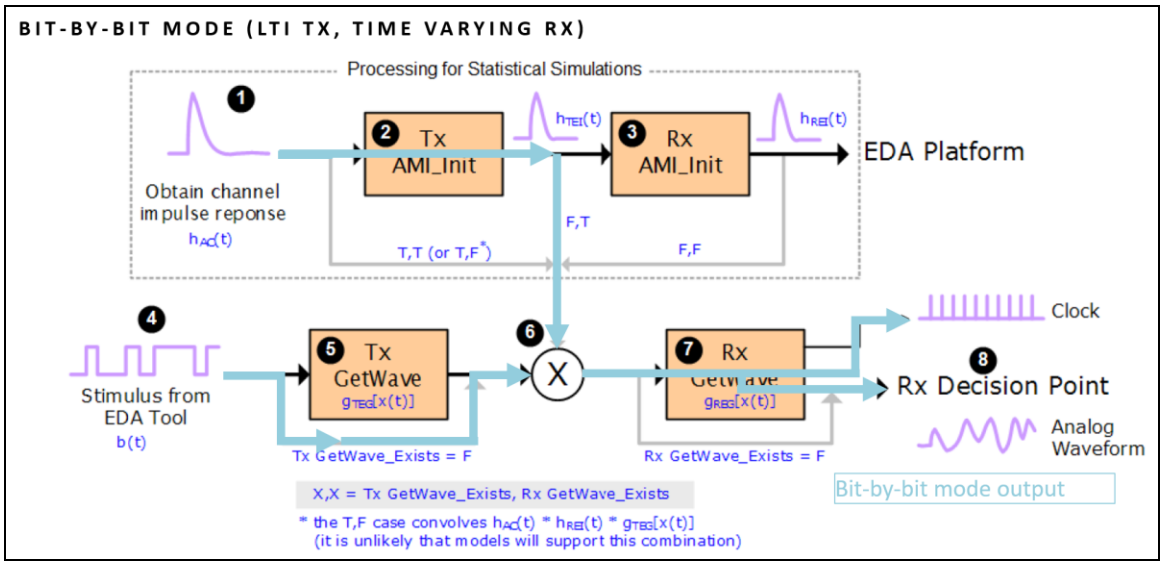

Figure 2. The PCIe 5.0 IBIS-AMI Tx and Rx simulation flow.

PCIe 5.0 Collateral Used for IBIS-AMI Model

The PCIe 5.0 electrical base specification is a 1299-page document [1]. Out of that material, only 30-50 pages are pertinent for AMI model building. As I list out the electrical signaling collateral used for AMI modeling, I'll reference page numbers to PCIe 5.0 base electrical specification document to allow for more in-depth review of the material.

Tx EQ behavior vs spec

1) Using PCI Express Base Spec Revision 5.0, Version 1.0 - PCI-SIG (page 1005)

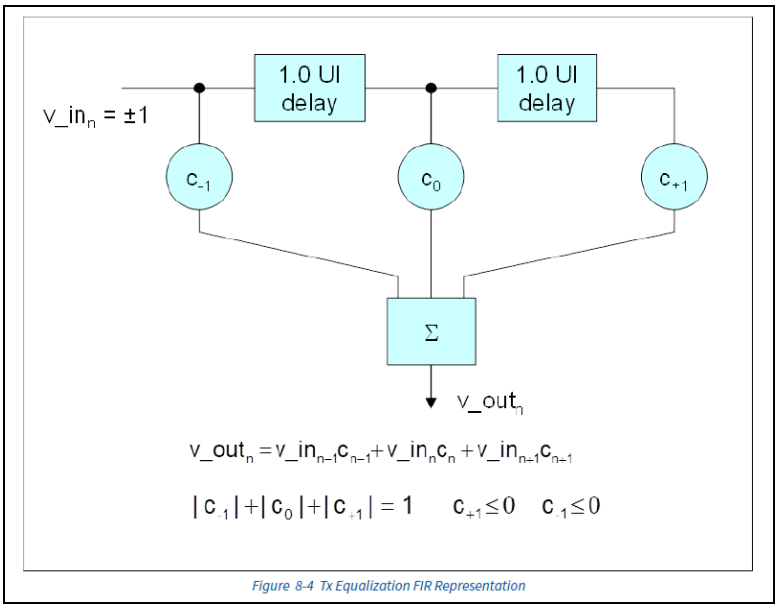

Figure 8-4 Tx Equalization FIR Representation

Figure 3. Tx Equalization FFE

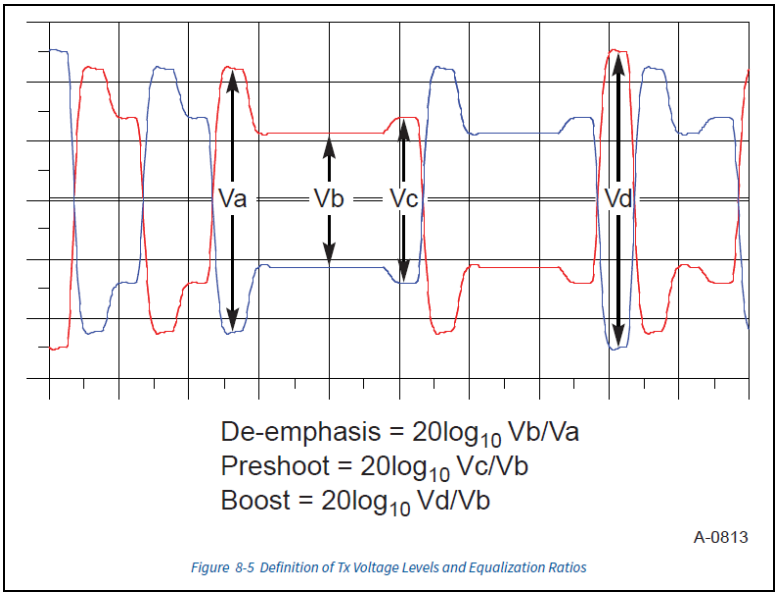

Figure 8-5 Definition of Tx Voltage Levels and Equalization Ratios

Figure 4. Definition of Tx Voltage Levels and Equalization Ratios

Table 1. Tx Preset Rations and Coefficient Values

Table 8-1 Tx Preset Ratios and Corresponding Coefficient Values

Preset #	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000

Preset #	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	Note 2.	0.000	Note 2.	1.000	Note 2.	Note 2.

Notes:

1. Reduced swing signaling must implement presets P4, P1, P9, P5, P6, and P3. Full swing signaling must implement all the above presets.
2. P10 boost limits are not fixed, since its de-emphasis level is a function of the LF level that the Tx advertises during training. P10 is used for testing the boost limit of Transmitter at full swing. P1 is used for testing the boost limit of Transmitter at reduced swing.

2) Pulse Response sweep of Tx Presets

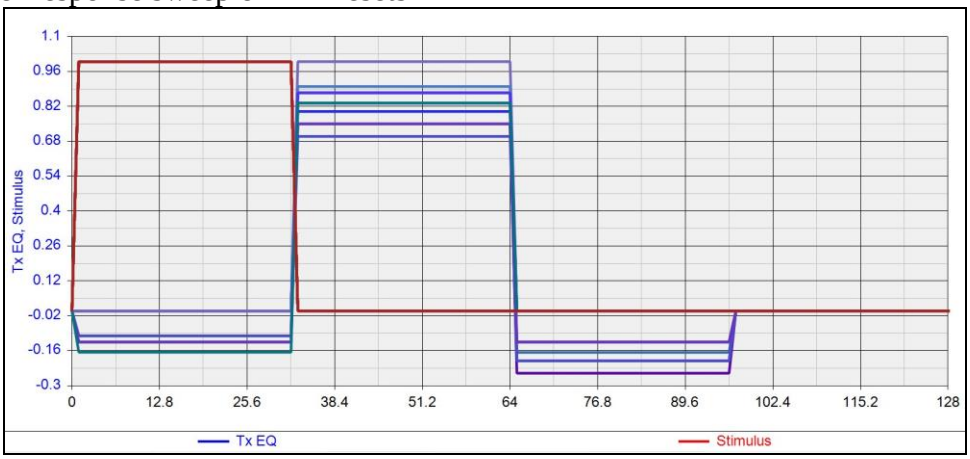

Figure 5. Single-bit pulse response of Tx Presets in Table 1

Rx CTLE frequency behavior vs spec

1) Using PCI Express Base Spec Revision 5.0, Version 1.0 - PCI-SIG (page 1046)

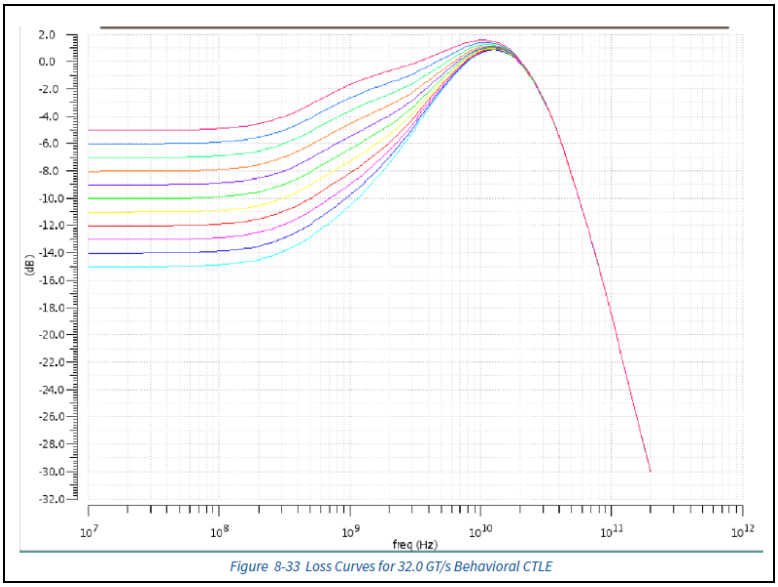

Figure 6. Gain vs Frequency curves for 32 GT/s Behavioral CTLE

Equation 1. S-domain Transfer function for Behavioral CTLE at 32 GT/s

$$H(s) = \frac{\omega_{P1} \times \omega_{P3} \times \omega_{P4}}{\omega_{Z1}} \times \frac{(s + \omega_{Z1})(s + \omega_{P2} \times A_{DC})}{(s + \omega_{P1})(s + \omega_{P2})(s + \omega_{P3})(s + \omega_{P4})}$$

$\omega_x = 2\pi \times F_x$

$F_{P1} = 1.65 \times F_{Z1}$

$F_{P2} = 9.5$ GHz

$F_{P3} = 28$ GHz

$F_{P4} = 28$ GHz

$F_{Z1} = 450$ MHz

$F_{Z2} = \text{mag(DC gain)} \times F_{P2}$

Equation 8-7 Behavioral CTLE at 32.0 GT/s

2) Pulse response of CTLE curves

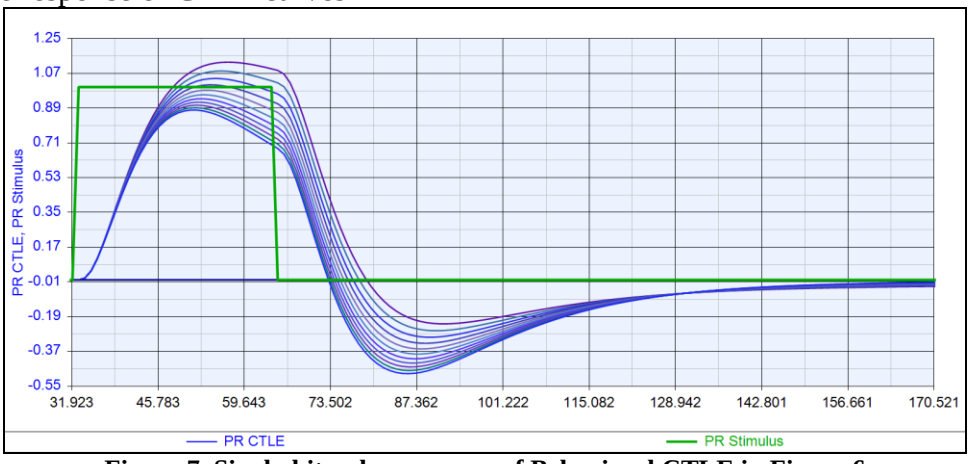

Figure 7. Single-bit pulse response of Behavioral CTLE in Figure 6

Rx CDR behavior vs spec

1) Using PCI Express Base Spec Revision 5.0, Version 1.0 - PCI-SIG (page 1019)

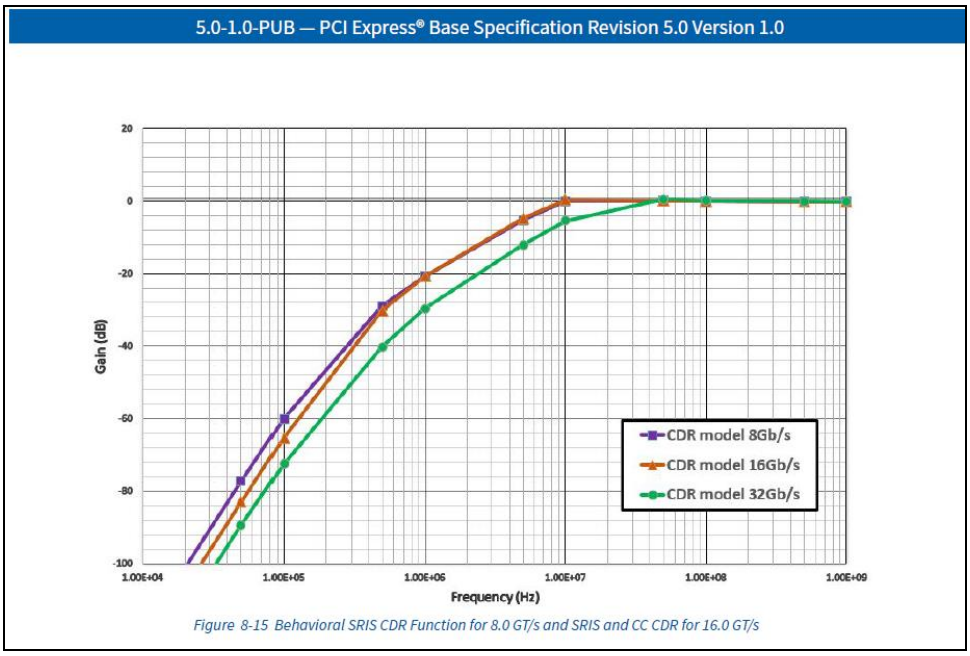

Figure 8. Behavioral CDR frequency response at 32 GT/s

2) Build IBIS-AMI model with CDR adjustments
Using linear phase detector with VCO to implement CDR. VCO input sensitivity is adjusted by following equation:

Equation 2. VCO input gain sensitivity with rx_cdr_adjust parameter control

vco_sensitivity = (1.0/sampleinterval) * (1.0/(2.0*3.1415926)) * (1.0/rx_cdr_adjust)

3) Setup simulation to sweep 0.1UI of periodic jitter (PJ) at different frequencies. Plot the jitter transfer gain. Characterize CDR performance in time-domain simulation.

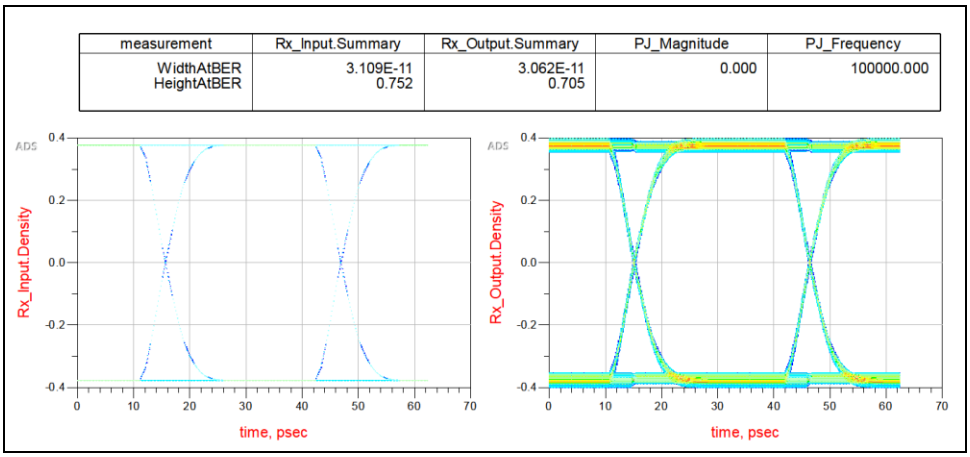

Figure 9. Baseline - no PJ (periodic/sinusoidal jitter)

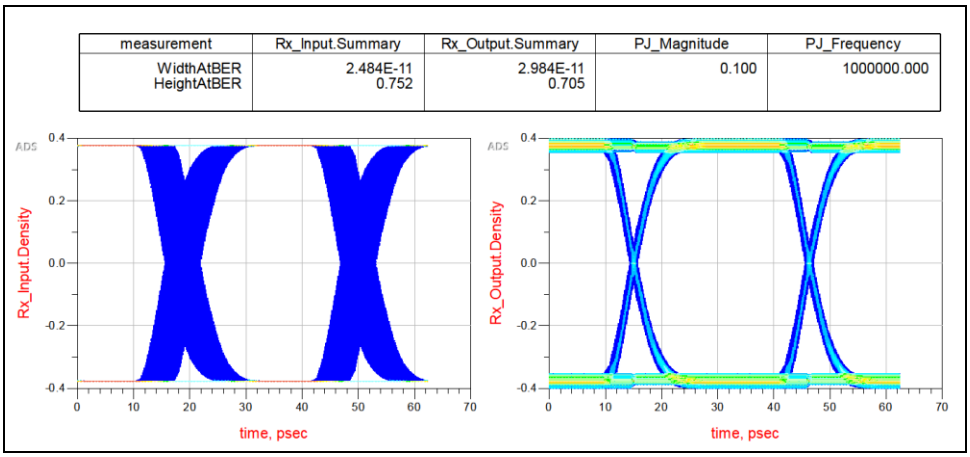

Figure 10. PJ=0.1 UI, Frequency=1e6 Hz (jittery input and stable output clock…CDR is tracking)

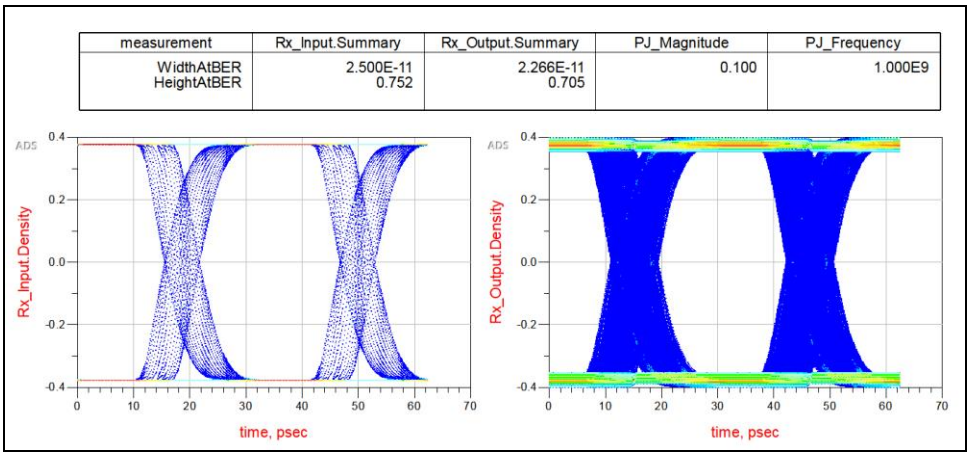

Figure 11. PJ=0.1 UI, Frequency=1e9 Hz (jittery input and jittery output clock…CDR is now pass-thru)

Simulation results - sweeping pj_freq, pj_value, cdr_adjust

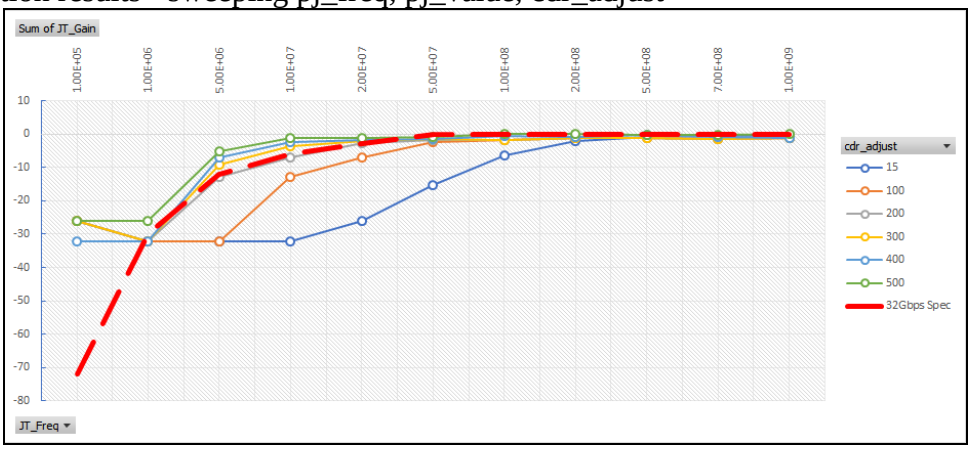

Figure 12. PJ frequency vs. PJ value vs. cdr_adjust parameter variation (graph)

Table 2. PJ Frequency vs. PJ Value vs. cdr_adjust parameter variation (data)

Freq	15	100	200	300	400	500	32Gbps Spec
1.00E+05	-26	-26	-26	-26	-32	-26	-72
1.00E+06	-32	-32	-32	-32	-32	-26	-30
5.00E+06	-32	-32	-13	-9	-7	-5	-12
1.00E+07	-32	-13	-7	-4	-2	-1	-6
2.00E+07	-26	-7	-3	-2	-2	-1	-3
5.00E+07	-15	-2	-2	-1	-1	-1	0
1.00E+08	-6	-2	-2	-2	0	0	0
2.00E+08	-2	-1	-1	-1	-1	0	0
5.00E+08	-1	-1	-1	-1	0	0	0
7.00E+08	0	-1	-1	-1	-1	0	0
1.00E+09	0	-1	-1	-1	-1	0	0

Results:

- Lower cdr_adjust increases frequency tracking.
- To meet 32GT/s PCIe spec, use setting cdr_adjust = 200.

Rx DFE behavior vs spec

1) Using PCI Express Base Spec Revision 5.0, Version 1.0 - PCI-SIG (page 1048). For 32 GT/s the limit on d1 is defined a ration of the tap magnitude (h1) to the cursor strength (h0). The h1/h0 ration must be less than or equal to 0.8.

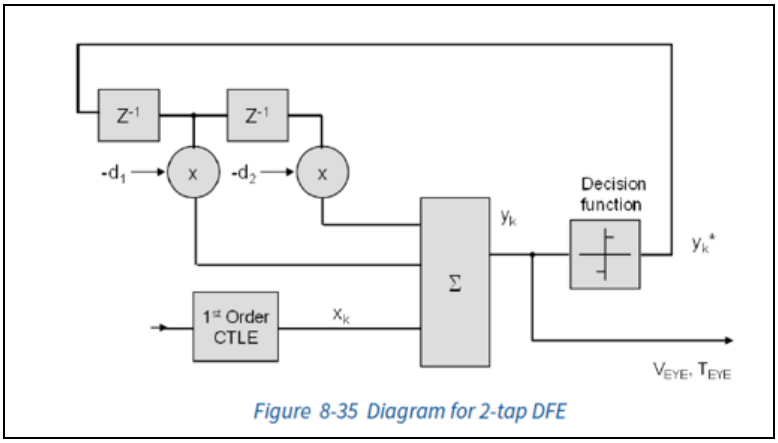

Figure 13. Diagram for DFE

2) Defining h1/h0 ratio. h1 tap strength is coefficient d1 * (-1, +1) from slicer, so mag(h1) = d1. Therefore, h1/h0 < 0.8 constraint converts to d1 < 0.8*h0. Inside the Rx model, implement a d1 measurement circuit.

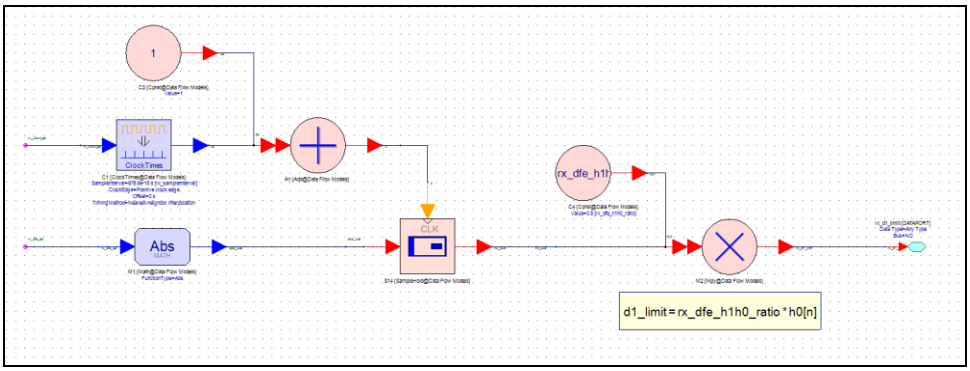

Figure 14. DFE d1 limit measurement circuit for IBIS-AMI model

Example IBIS-AMI Rx Parameter out of "rx_dfe_tap1_limit". It provides a bounding limit for d1 that meets h1/h0<0.8 spec requirement.

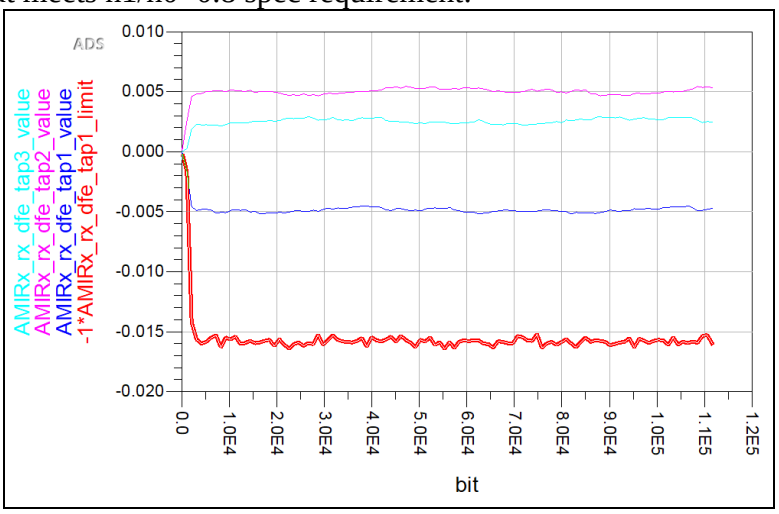

Figure 15. Rx IBIS-AMI parameter out for DFE tap1 limit calculation

PCIe spec jitter vs AMI jitter components; Eye-margin table

Table 3. Summary of PCIe jitter from 2.5 GT/s to 32 GT/s

Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
T-TX UTJ	Tx uncorrelated total jitter	100	50	27.55	11.8	6.25	ps PP at 10^-12 BER
T-TX UTJ SRIS	Tx uncorrelated total jitter when testing for the IR clock mode with SSC	100	66.51	33.83	15.85	7.15	ps PP at 10^-12 BER
T-TX UDJDD	Tx uncorrelated Dj for non embedded Refclk	100	30	12	6.25	3.125	ps PP
T-TX UPW TJ	Total uncorrelated pulse width jitter	N/A	40	24	12.5	6.25	ps PP at 10^-12 BER
T-TX UPWDJDD	Deterministic DjDD uncorrelated pulse width jitter	N/A	40	10	5	2.5	ps PP
T-REFCLK-RMS		86	3.1	1	0.7	0.25	ps RMS

2) Derived jitter parameters (per page 1080 formulas)

Table 4. Converting jitter parameters to high-frequency and low-frequency components.

Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
jit_hfrj_nui	Tx Rj (HF+LF) edge	0.000	1.422	1.105	0.394	0.222	ps
T-TX UDJDD	Tx Dj (HF+LF) edge	100.000	30.000	12.000	6.250	3.125	ps
TTX-CH-URJ	Tx Rj (LF) + Clk Rj edge	3.450	3.450	1.314	0.710	0.276	ps
TTX-CH-UDJDD	Tx Dj (LF) edge	20.000	20.000	7.000	3.750	1.875	ps
TTX-CH-UPW-RJ	Tx Rj (HF) PW	1.420	1.420	0.995	0.533	0.267	ps
TTX-CH-UPW-DJ	Tx Dj (HF) PW	80.000	40.000	10.000	5.000	2.500	ps
Total Jitter	T-TX UTJ + Clk Rj		93.614	41.619	21.648	9.767	

Table 5. Formulas used to convert jitter in Table 3 to Table 4

Label	Jitter Parameter	Formula
jit_hfrj_nui	Tx Rj (HF+LF) edge	'=(T_TX_UTJ-T_TX_UDJDD)/14.069
T-TX UDJDD	Tx Dj (HF+LF) edge	'=T_TX_UDJDD
TTX-CH-URJ	Tx Rj (LF) + Clk Rj edge	=SQRT(jit_hfrj_nui^2 - (TTX_CH_UPW_RJ/SQRT(2))^2 + (T_REFCLK_RMS)^2)
TTX-CH-UDJDD	Tx Dj (LF) edge	'=T_TX_UDJDD-T_TX_UPWDJDD/2
TTX-CH-UPW-RJ	Tx Rj (HF) PW	'=(T_TX_UPW_TJ-T_TX_UPWDJDD)/14.069
TTX-CH-UPW-DJ	Tx Dj (HF) PW	'=TTX_CH_UDJDD
Total Jitter	T-TX UTJ + Clk Rj	'=T_TX_UTJ+((T_REFCLK_RMS*14.069))

3) Resulting AMI jitter parameters. Converting all the pulse-width (PW) jitter to edge jitter. Allocating high-frequency (HF) jitter to Tx and low-frequency (LF) jitter to Rx.

Table 6. Jitter parameters for use in IBIS-AMI model

Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
Tx_Rj	Tx Rj (HF) edge			0.704	0.377	0.188	ps
Tx_Dj	Tx Dj (HF) edge			5.000	2.500	1.250	ps
Tx_DCD							
Rx_Rj	Tx Rj (LF) + Clk Rj edge			1.314	0.710	0.276	ps
Rx_Dj	Tx Dj (LF) edge			7.000	3.750	1.875	ps
Rx_DCD							
Rx_Noise							
Tx Total Jitter	Tx Dj + Tx Rj			14.90	7.80	3.90	ps
Rx Total Jitter	Rx Dj + Rx Rj			25.49	13.73	5.76	ps
Total Jitter	Tx + Rx			40.39	21.54	9.66	ps
T_TX_UTJ + T_REFCLK_RMS	Total Jitter check (over-est)			41.62	21.65	9.77	ps

Table 7. Formulas used to convert jitter in Table 4 to Table 6

Label	Jitter Parameter	Formula
Tx_Rj	Tx Rj (HF) edge	'=TTX_CH_UPW_RJ/SQRT(2)
Tx_Dj	Tx Dj (HF) edge	'=(T_TX_UPWDJDD/2)
Tx_DCD		
Rx_Rj	Tx Rj (LF) + Clk Rj edge	=TTX_CH_URJ
Rx_Dj	Tx Dj (LF) edge	'=T_TX_UDJDD-Tx_Dj
Rx_DCD		
Rx_Noise		
Tx Total Jitter	Tx Dj + Tx Rj	'=(Tx_Rj*14.069)+Tx_Dj+Tx_DCD
Rx Total Jitter	Rx Dj + Rx Rj	'=(Rx_Rj*14.069)+Rx_Dj+Rx_DCD
Total Jitter	Tx + Rx	'=Tx_Total_Jitter+Rx_Total_Jitter
T_TX_UTJ + T_REFCLK_RMS	Total Jitter check (over-est)	'=T_TX_UTJ+14.069*T_REFCLK_RMS

- Note on conversion relationship:
  - Deterministic edge jitter = (1/2) Deterministic pulse width jitter
  - Random edge jitter = (1/sqrt(2)) Random pulse width jitter

Table 8. Visual summary of converting jitter in Table 4 to Table 6

Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
jit_hfrj_nui	Tx Rj (HF+LF) edge	0.000	1.422	1.105	0.394	0.222	ps
T-TX UDJDD	Tx Dj (HF+LF) edge	100.000	30.000	12.000	6.250	3.125	ps
TTX-CH-URJ	Tx Rj (LF) + Clk Rj edge	3.450	3.450	1.314	0.710	0.276	ps
TTX-CH-UDJDD	Tx Dj (LF) edge	20.000	20.000	7.000	3.750	1.875	ps
TTX-CH-UPW-RJ	Tx Rj (HF) PW	1.420	1.420	0.995	0.533	0.267	ps
TTX-CH-UPW-DJ	Tx Dj (HF) PW	80.000	40.000	10.000	5.000	2.500	ps
Total Jitter	T-TX UTJ + Clk Rj		93.614	41.619	21.648	9.767	

1/2

1/sqrt(2)

Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
Tx_Rj	Tx Rj (HF) edge			0.704	0.377	0.188	ps
Tx_Dj	Tx Dj (HF) edge			5.000	2.500	1.250	ps
Tx_DCD							
Rx_Rj	Tx Rj (LF) + Clk Rj edge			1.314	0.710	0.276	ps
Rx_Dj	Tx Dj (LF) edge			7.000	3.750	1.875	ps
Rx_DCD							
Rx_Noise							
Tx Total Jitter	Tx Dj + Tx Rj			14.90	7.80	3.90	ps
Rx Total Jitter	Rx Dj + Rx Rj			25.49	13.73	5.76	ps
Total Jitter	Tx + Rx			40.39	21.54	9.66	ps
T_TX_UTJ + T_REFCLK_RMS	Total Jitter check (over-est)			41.62	21.65	9.77	ps

Calculation Checks - Different ways to calculate total Rj. To verify previous jitter conversion calculations, 3 checks were put together to verify Rj separation agrees among the different methods. Since all the calculations give same Total Rj, then there is confidence the formulas are correct.

Table 9. Rj checks to confirm separation results in same total Rj

Label	Jitter Parameter	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
Rj check 1	Tx Rj + Rx Rj			1.491	0.804	0.334	ps
Rj check 2	Tx Rj (HF+LF) + Clk Rj			1.491	0.804	0.334	ps
Rj check 3	Tx Rj (HF) + Tx Rj (LF) + Clk Rj			1.491	0.804	0.334	ps

Table 10. Formulas used in Table 9

Label	Jitter Parameter	Formula
Rj check 1	Tx Rj + Rx Rj	'=SQRT(Tx_Rj^2+Rx_Rj^2)
Rj check 2	Tx Rj (HF+LF) + Clk Rj	'=SQRT(jit_hfrj_nui^2+T_REFCLK_RMS^2)
Rj check 3	Tx Rj (HF) + Tx Rj (LF) + Clk Rj	'=SQRT(((TTX_CH_UPW_RJ/SQRT(2))^2)+TTX_CH_URJ^2)

4) Eye mask table

Table 11. Eye mask eye-height and eye-width requirements

	2.5 GT/s	5.0 GT/s	8.0 GT/s	16.0 GT/s	32.0 GT/s	Units
EH @ BER	130	85	25	15	15	mV
EW @ BER	140	60	37.5	18.75	9.375	pS

5) Pass/Fail Eye Characteristics

8.5.1.4.3 Pass/Fail Eye Characteristics

The output of the simulation tool shall be in the form of pass/fail characteristics as defined by an eye mask as shown in Figure 8-63 . EH and EW must meet respectively the voltage and jitter parameters defined in Table 8-14 . Eye margins are defined at the die pad of the Receiver after the appropriate Tx and Rx equalization algorithms have been applied. In the case where the channel is being designed for a specific pair of silicon devices and the package models of these silicon devices including cross-talk aggressors are known the actual device packages may be used instead of the reference packages in running the pad to pad channel pass/fail compliance simulations.

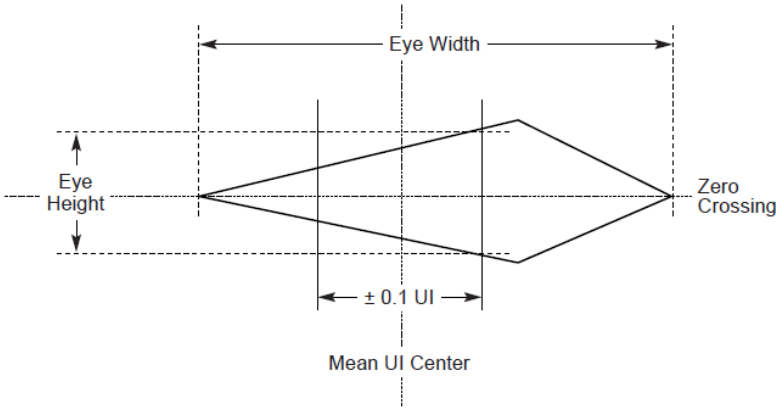

Figure 16. Pass/Fail Eye Characteristics

6) Eye mask for simulations. Eye height defined as maximum within +/-0.1 UI from mean UI center. Eye width at zero crossing. Eye mask for simulation setup in Figure 17. +/-7.5mV EH set for -0.1UI of UI Center .

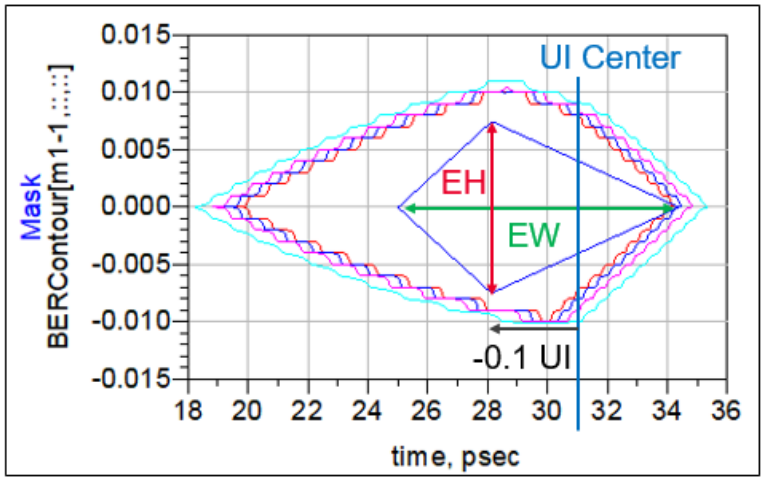

Figure 17. Simulation eye-mask derived from criteria in Figure 16

Correlation – Dataflow model building environment vs. IBIS-AMI simulation results under same channel & settings

PCIe 5.0 informative insertion loss limit is -36dB at 16GHz. Use that informative limit to compare with Tx, Rx and jitter assumptions. All specification assumptions plus maximum insertion loss should give close to at-margin performance. When building an IBIS-AMI model, it's convenient to use a data flow simulation environment to test the algorithmic methods before compiling into the C++ DLL wrapper for IBIS-AMI. When compiled to C++, you'll loose intermediate node visibility which is very helpful for the model development phase.

1) Short Channel (-12dB at 16GHz)
Leveraging 1x cascaded 4-port S-parameter files. Publicly available channel from Ethernet workgroup: "C2C_PCB_SYSVIA_18dB_thru.s4p" [4].

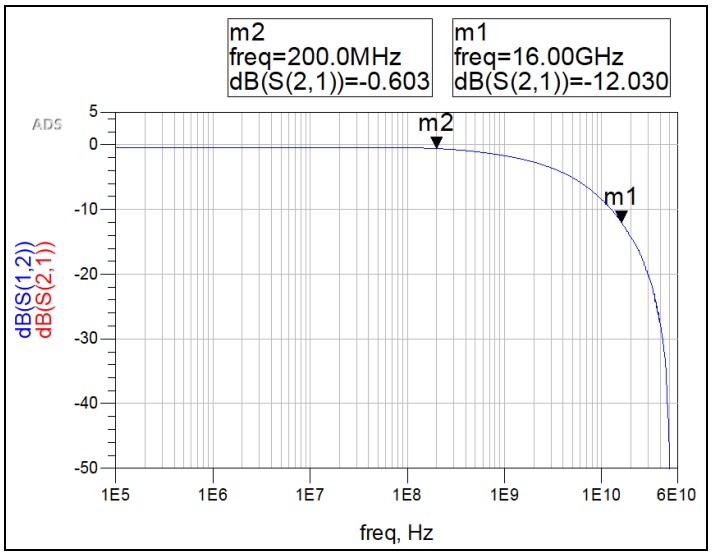

Figure 18. Differential insertion loss plot for Short Channel

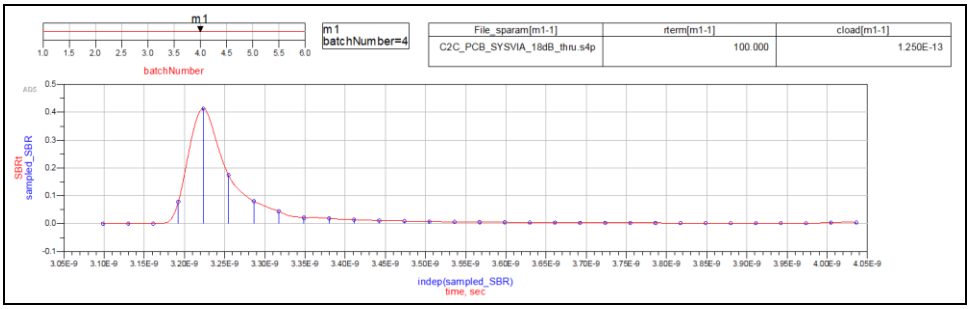

Figure 19. Single-bit pulse response for Short Channel

Results comparison:

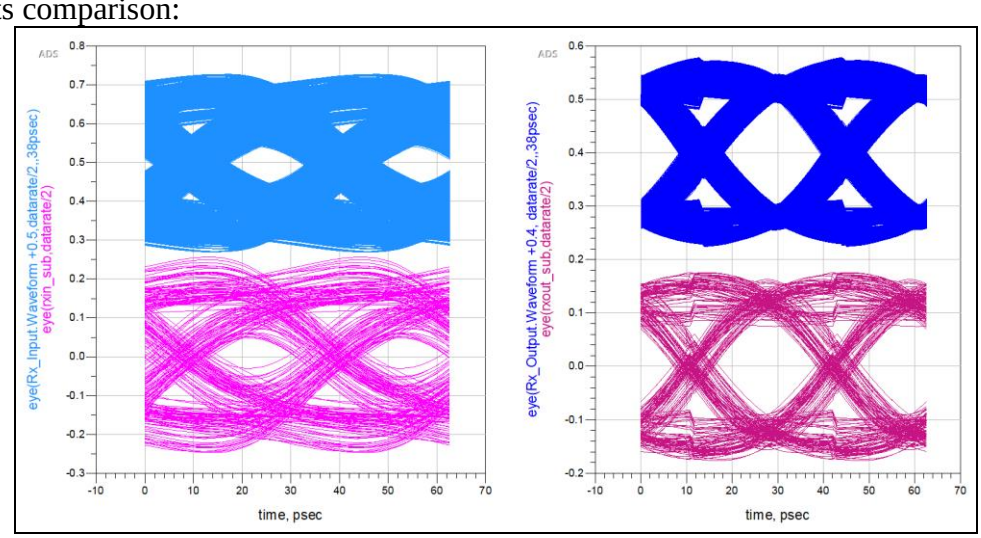

Figure 20. Short Channel Eye diagrams for Rx input & Rx output – IBIS-AMI (blue), dataflow (purple)

Optimized BER 1e-12 results: 226mV/18.125ps

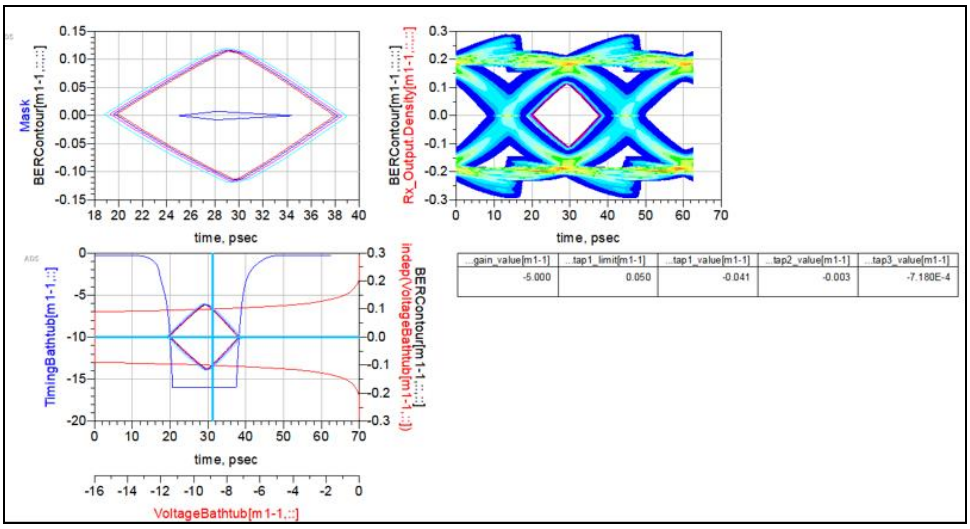

Figure 21. Short Channel BER results

2) Medium Channel (-28dB at 16GHz)
Leveraging 3x cascaded 4-port S-parameter files. Publicly available channel from Ethernet workgroup: "C2C_PCB_SYSVIA_14dB_thru.s4p" [4].

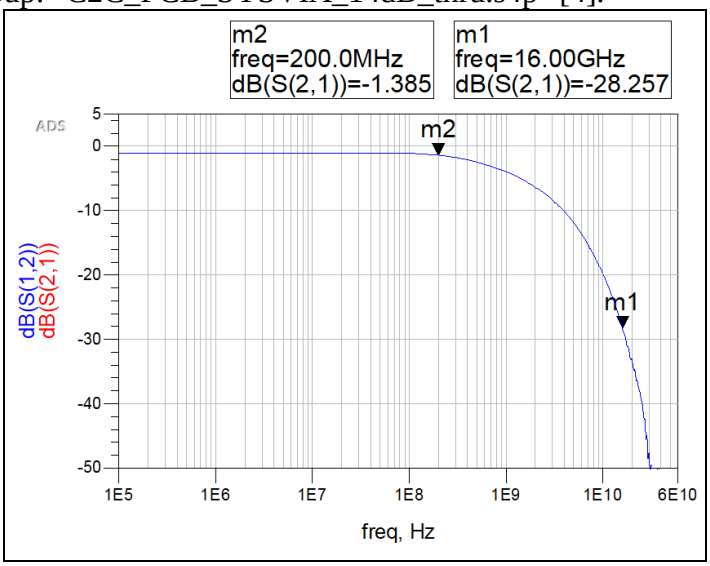

Figure 22. Differential insertion loss plot for Medium Channel

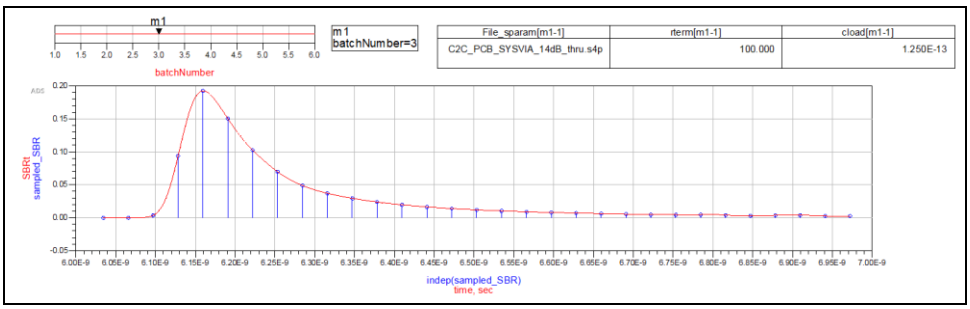

Figure 23. Single-bit pulse response for Medium Channel

Results comparison:

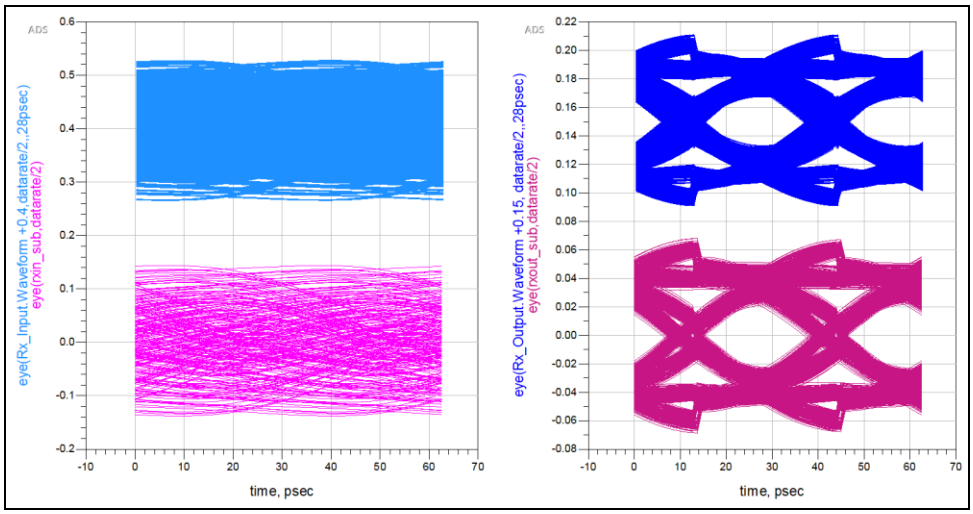

Figure 24. Medium Channel Eye diagrams for Rx input & Rx output – IBIS-AMI (blue), dataflow (purple)

Optimized BER 1e-12 results: 69mV/17.25ps

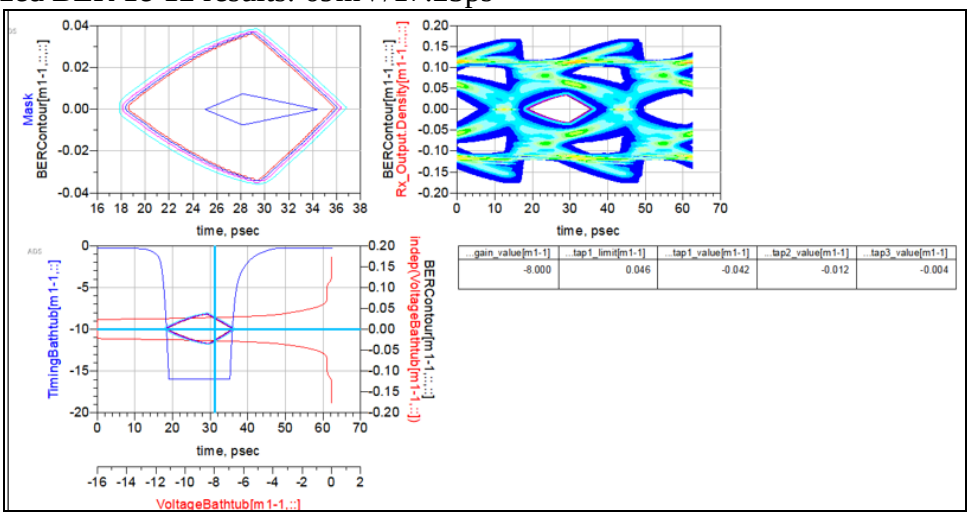

Figure 25. Medium Channel BER results

3) Long Channel (-36dB at 16GHz)
Leveraging 3x cascaded 4-port S-parameter files. Publicly available channel from Ethernet workgroup: "C2C_PCB_SYSVIA_18dB_thru.s4p" [4].

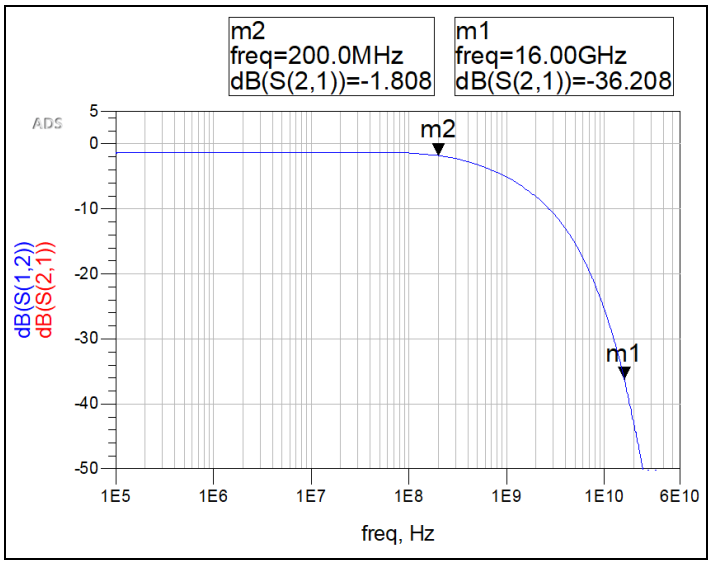

Figure 26. Differential insertion loss plot for Long Channel

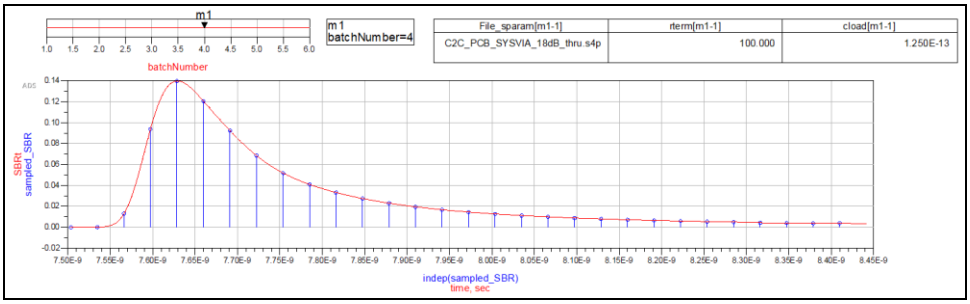

Figure 27. Single-bit pulse response for Long Channel

Results comparison:

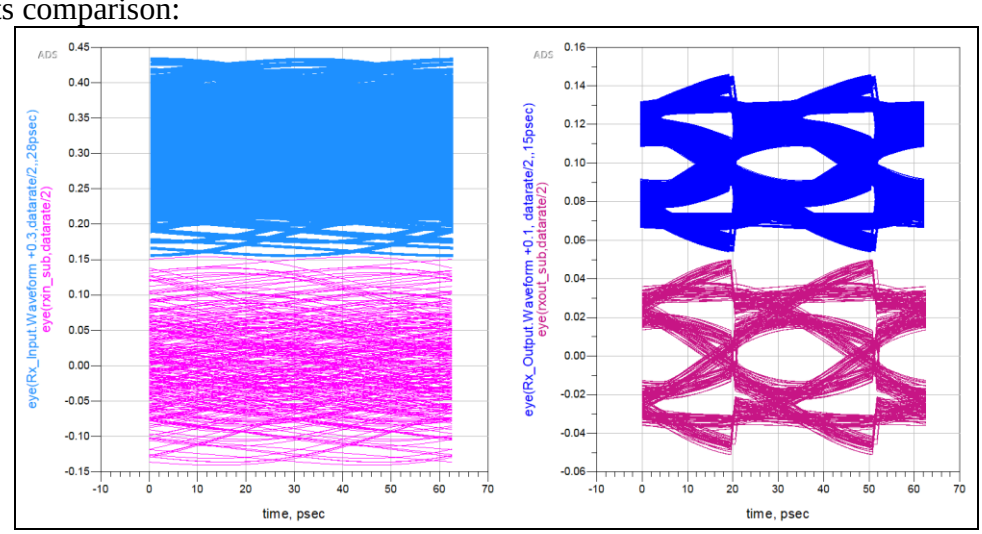

Figure 28. Long Channel Eye diagrams for Rx input & Rx output – IBIS-AMI (blue), dataflow (purple)

Optimized BER 1e-12 results: 19mV/14.813ps. Important note…at maximum insertion loss of -36dB at 16GHz, we do see very close to at-margin behavior. This is our loose confirmation that when capturing all the PCIe 5.0 specification elements the resulting IBIS-AMI model analysis is providing expected results.

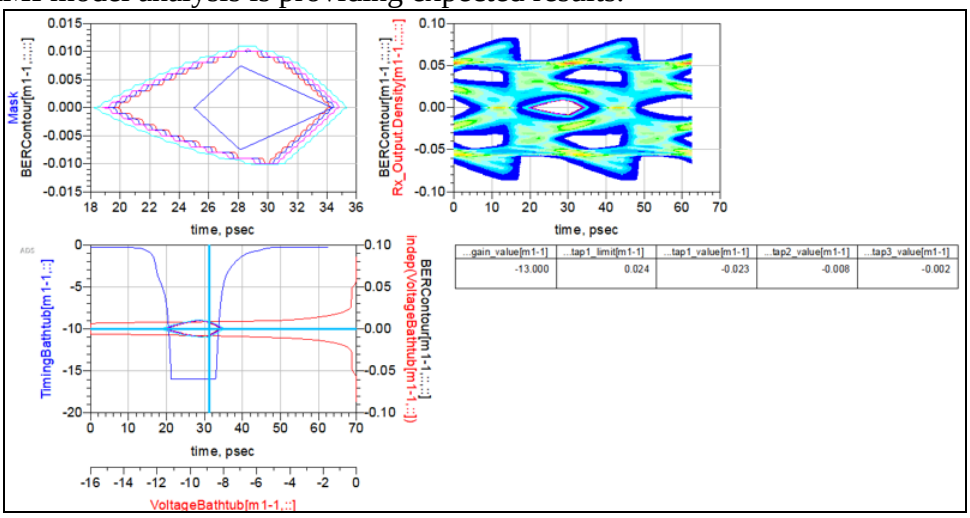

Figure 29. Long Channel BER results

IBIS-AMI Simulation: Verifying Rx CTLE adaptation

Batch simulation sweep:

- 100k bits analyzed
- Sweeping Tx Preset (10 settings)
- Sweeping Rx CTLE DC Gain (11 settings)
- Varying Rx CTLE adapt on/off
- Varying 4 Channels: -12dB, -24dB, -36dB & -36dB with reflections
- Total is 440 cases to test static mode
- Plus additional 40 cases to test adaptive mode

Simulation Performance:

- 480 simulation cases total
- Run on single laptop
- Simulation time of 24k sec total (or 6 hr 40 min)
- That's 50 sec per case!

Reference Table 12 for the results of the 480 case simulation sweep. To find the optimal value, 440 cases at static settings were varied to choose best CTLE DC gain setting. For adapted value, 40 cases were varied (where Rx CTLE would automatically adapt) and results were compared with optimal value to verify the adaptation behavior.

Table 12. 480 case Rx CTLE Adaptation Batch Mode Simulation Results

Channel	Tx Preset	EH Optimal	EH adapted	EW Optimal	EW adapted	DC Gain Optimal	DC Gain adapted
pcie5_test_m12db.s4p							
	0	168.215	168.215	16.25	16.25	-5	-5
	1	193.706	193.706	18.25	18.25	-5	-5
	2	182.367	182.367	17.375	17.375	-5	-5
	3	201.117	201.117	18.625	18.625	-5	-5
	4	219.76	219.76	18.75	18.75	-5	-5
	5	226.458	226.458	18.125	18.125	-5	-5
	6	218.134	218.134	17.688	17.688	-5	-5
	7	161.827	161.827	15.312	15.312	-5	-5
	8	176.405	176.405	16.313	16.313	-5	-5
	9	194.785	194.785	16.625	16.625	-5	-5
pcie5_test_m24db.s4p							
	0	60.001	57.001	17.625	16.938	-5	-6
	1	62.292	62.292	17.688	17.688	-7	-7
	2	59	59.053	17.375	17.25	-8	-7
	3	64.614	64.614	17.813	17.813	-8	-8
	4	70.002	69.079	17.75	17.25	-9	-8
	5	68.004	68.004	17.125	17.125	-8	-8
	6	67.064	67.064	17.313	17.313	-8	-8
	7	61	58.068	17.125	16.813	-5	-6
	8	61.757	61.001	16.063	16.688	-6	-7
	9	64.193	64.193	15.875	15.875	-8	-8
pcie5_test_m36db.s4p							
	0	15	12	14.5	11.5	-13	-10
	1	17	16	14.438	13.875	-13	-12
	2	16	13.004	15.25	12.375	-13	-11
	3	18	16	15.125	13.563	-13	-12
	4	19	19	14.813	14.813	-13	-13
	5	19	14	16	14.312	-14	-12
	6	18	13	16	14.375	-14	-12
	7	15.028	11	15.625	13.5	-12	-10
	8	16.034	11	15.188	13.938	-13	-11
	9	17	12	15.375	13.625	-14	-12
pcie5_test_m36db_reflections.s4p							
	0	8	8	9.5	9.5	-8	-8
	1	9	9	9.438	9.438	-9	-9
	2	8	8	10.188	10.188	-9	-9
	3	9.021	9.021	9.563	9.563	-10	-10
	4	4	-1	6.687	0	-12	-10
	5	14	13	12.313	12.188	-11	-10
	6	16	16	13.563	13.563	-10	-10
	7	12	12	13.625	12.937	-9	-8
	8	14	14	14.063	14.063	-9	-9
	9	15	15	13.188	13.188	-10	-10

The following is the Rx CTLE adaptation approach used in the IBIS-AMI model. See Figure 30 for illustration:

1. Per the IBIS specification [2], the Rx model will receive modified impulse response (IR) to AMI_Init. This modified impulse response will be (channel + Tx) IR.
2. (channel + Tx) IR information is combined with each of the eleven CTLE curves to select optimal DC Gain setting to use for simulations.
3. "optimal" CTLE DC Gain setting = strongest equalization the (channel + Tx) IR needs without over-equalizing. 3 tap DFE is last equalization step and will provide the "fine adjust" for the final waveform output

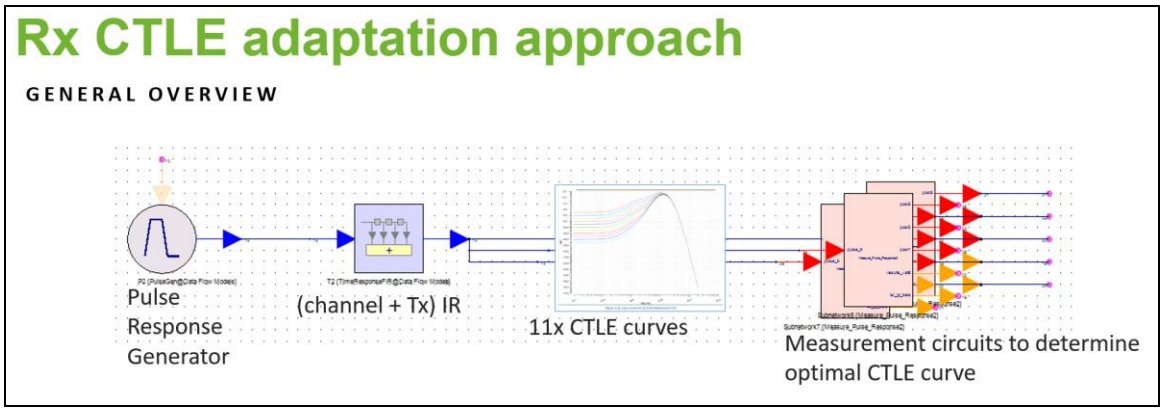

Figure 30. Rx CTLE adaptation approach used in the IBIS-AMI model

Conclusion

We've shown why you would want a PCIe 5.0 32GT/s specification-based IBIS-AMI model. It's allows you to take the 1000+ page specification document and convert it to something you can use in end-to-end signal integrity analysis. It's also portable among different EDA simulations tools, to support a diverse set of methodologies.

We've shown details of how the PCIe 5.0 32GT/s spec-based IBIS-AMI model work. Its capabilities being FFE, CTLE, DFE, CDR and jitter budget modeling. Current limitations are that it was verified to the -36dB informative limit.

The strategic value of PCIe 5.0 32GT/s spec-based IBIS-AMI model is that you can build your analysis flow early with industry standard PHY model. Later you can swap-in IP PHY model (when it's available) and perform A/B testing, but already have a good idea how your end-to-end channel performance is based on electrical specification. Lastly, spec-based IBIS-AMI model supports continuous development, in that you can provide incremental changes to the model to support next generation standards, like PCIe 6.0 64GT/s spec-based, for early simulation assessment.

References

[1] PCI Express Base Spec Revision 5.0, Version 1.0 - PCI-SIG

[2] IBIS (I/O Buffer Information Specification), Version 7.0, Ratified March 15, 2019, IBIS Open Forum 2019

[3] Bob Sullivan, Michael Rose, Jason Boh, Simulating High-Speed Serial Channels with IBIS-AMI Models, Keysight Technologies, Application Note, August 2014

[4] ieee802.org, 'IEEE P802.3ck 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force Public Area', 2019. [Online]. Available: http://www.ieee802.org/3/ck/public/index.html. [Accessed: 4- Nov-2019].