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A Novel Approach to 224 Gb/s Reference Receiver Design Using Raised Cosine Response for Noise Mitigation

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Abstract

Current work for Standardized Datacenter interconnect communication has led to the publication of IEEE 802.3ck supporting 100 Gb/s per lane. Ethernet line rates are 106 Gb/s using 4 level pulse amplitude modulation (PAM4) and similarly 112 Gb/s for Optical Internetworking Forum (OIF-CEI-05.0) specifications.

The next generation of high-speed interfaces are expected to operate at 212 Gb/s PAM4. Channel design and corresponding equalization schemes require novel solutions beyond those found in 106 Gb/s PAM4 designs. In the same way that the IEEE802.3ck required improvements in interconnect loss per unit length, reflections, crosstalk, filtering, and equalization, the jitter requirements for the sub-10 ps Unit Interval (UI) and noise parameters are expected to be more stringent for next generation semiconductor devices.

Since noise is integrated over the entire operating channel bandwidth, its impact must be mitigated by appropriate filtering at the receiver. The 80 GHz cut off frequency of the 4th order Butterworth filter extrapolated from IEEE802.3ck may no longer be sufficient. Discussion within this paper includes aspects of a novel Raised Cosine (RCos) filter, which has a steeper low pass roll-off that can be aligned with required measurement bandwidth.

Author(s) Biography

Luis Boluña is a Senior Application Engineer for Keysight Technologies. He has extensive experience in both the measurement and simulation of high speed SerDes architectures and backplane designs. His background is Signal Integrity and Mixed Signal Circuit Design. He has worked in Silicon Valley almost 29 years with Agilent, Cisco Systems, Rambus, Microsoft, and National Semiconductor. Luis has two US patents and has a Pioneer Award from Cisco Systems. His research interests are in system design, testability, simulation, and validation of high speed designs. Luis holds a BSEE from UC Santa Barbara with an emphasis in Solid State Physics.

John Calvin is a strategic planner and datacom technology lead for Keysight Technologies. John has been bridging the measurement science gaps of emerging Telecom and DataCom development efforts for 20 years. He has chaired multiple physical layer interoperability working groups and is currently serving as a contributing member to IEEE 802.3, OIF-CEI, InfiniBand, and PCIe development efforts. John holds a BSEE from Washington State University, and his graduate level studies are in signal processing from Stanford University.

Francesco de Paulis was born in L'Aquila, Italy in 1981. He received the M.S. degree in Electrical Engineering in May 2008 from Missouri University of Science and Technology (formerly University of Missouri-Rolla), USA, and the PhD degree in Electrical and Information Engineering in 2012 from the University of L'Aquila, L'Aquila, Italy. He is currently a Research Professor at the University of L'Aquila
His main research interests are in SI/PI design on PCB, packages, interposers and chips, high speed channel characterization and design, RF interference in mixed-signal system, EMI and EMC.

Richard Mellitz is presently a Distinguished Engineer at Samtec, supporting interconnect signal integrity and industry standards. Richard has been a key contributor to IEEE802.3 electrical standards for many years. He led efforts to develop radically new IEEE and OIF time domain specification methods called COM (Channel Operating Margin) and ERL (Effective Return Loss). Early in his career he founded and chaired an IPC committee authoring the industry's first TDR standard. Richard holds many patents in interconnect, signal integrity, design, and test. Richard received the IEEE Standards Association Medallion and the Intel Achievement Award (IAA) for spearheading the industry's first graduate signal integrity programs at the University of South Carolina. Recently, Richard was honored with the DesignCon 2022 Engineer of the Year Award.

Rick Rabinovich, IEEE802.3 Ethernet voter member, is a Distinguished Engineer at Keysight Technologies, specializing in 3D modeling of electromagnetic structures and PCB stackup optimization for 10G/25G/50G/100G/200G/400 GbE. Former IEEE Communication Society member, Rick was a Senior Principal Design Engineer at Alcatel-Lucent and an Alcatel-Lucent Bell Labs Distinguished Member of the Technical Staff. He has authored several technical articles in the IEEE Communications and EDN magazines and holds two US patents in communications. Rick's previous positions include Hardware Technology Director and Fellow Associate at Spirent Communications, and senior position at Northrop. Rick holds a BS from the Buenos Aires University Engineering College and attended computer post-graduate courses at Cal State Los Angeles, UCLA, and UCI.

Mike Resso is the Signal Integrity Application Scientist in the Internet Infrastructure Solution Group of Keysight Technologies and has over thirty years of experience in the test and measurement industry. His background includes the design and development of electro-optic test instrumentation for aerospace and commercial applications. His most recent activity has focused on the complete multiport characterization of high-speed digital interconnects using Time Domain Reflectometry and Vector Network Analysis. He has authored over 30 professional publications including two books on signal integrity. Mike has been awarded one US patent and has twice received the Agilent "Spark of Insight" Award for his contribution to the company. He received a Bachelor of Science degree in Electrical and Computer Engineering from University of California.

Introduction

There are significant technical challenges to achieve 212 Gb/s (or OIF 224 Gb/s) in the network and data center ecosystem [1]. Interface chips, DSP chips, packaging, connectors etc. and all physical layer components will need performance improvements for new designs to work at higher data rates [2]. There are already some corresponding standards in the industry that define 106 Gb/s PAM4 electrical ports [3]. This paper will provide direction for the design teams developing these new emerging datacenter communications standards, following and extending the preliminary work in [4].

The development of reliable guidelines for designing and testing high-speed interfaces running at 212 Gb/s will be provided based on a complete experimental setup. An instrumentation source (BERT), a channel representative of typical C2M interface (in terms of loss at Nyquist), and an equivalent time sampling oscilloscope fully equipped with data processing capabilities (filtering, noise injection, and equalization) are employed as an experimental benchmark. Source characterization in terms of noise, jitter, signal amplitude, rise time, and impedance matching is carried out to define the proper parameters necessary for the statistical channel analysis based on the COM algorithm. As a first step, a reference receiver filter and TX/RX equalization will be set for experimentally verifying the channel performances Eye Height (EH) and Vertical Eye Closure (VEC) as predicted by COM. Once this is completed, the impact of the receiver filtering will be investigated.

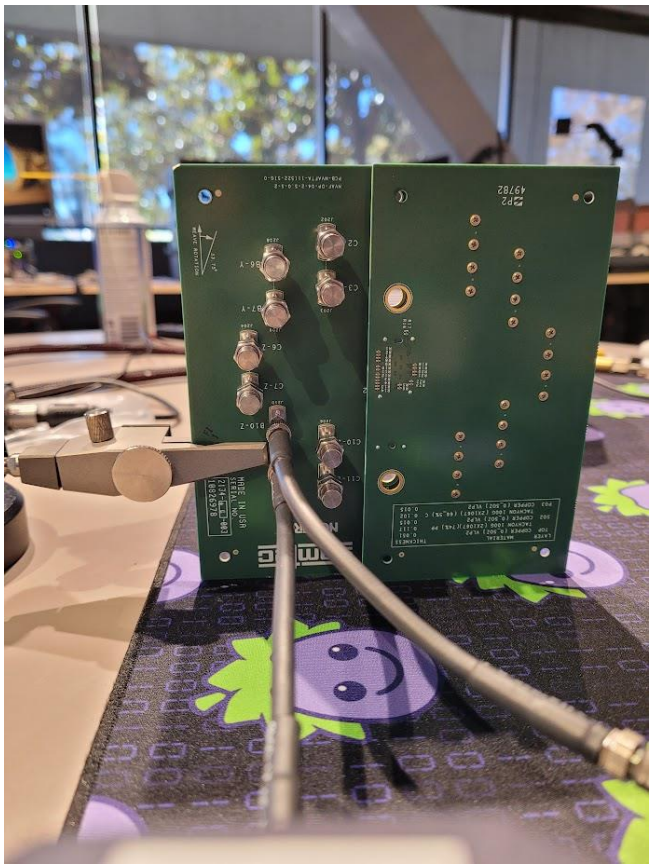
A specific analysis will be carried out by tuning the proposed filter parameters and then it will be compared with the reference Butterworth filter based on the physical channel under investigation. This task will involve the measured waveform at the pattern generator output of the BERT and the RX equalization on the scope will use a full experimental demonstration. A parametric analysis, aimed at understanding the filter design requirement, will be realized by varying the starting frequency of the Raised Cosine (RCos) filter roll-off and measuring its corresponding impact on the eye metrics (EH and VEC). This analysis will lead to the quantification of the advantages/disadvantages of the newly proposed Raised Cosine filter as shown below:

- The Raised Cosine filter will maximize Signal-to-Noise Ratio (SNR) while improving Eye Height (EH) and Vertical Eye Closure (VEC) compared to the standard Butterworth filter
- Higher frequency noise of a working channel at 112 Gb/s PAM4 will enable higher η_0 noise
- Practical aspects for the implementation of the complete measurement setup will be discussed

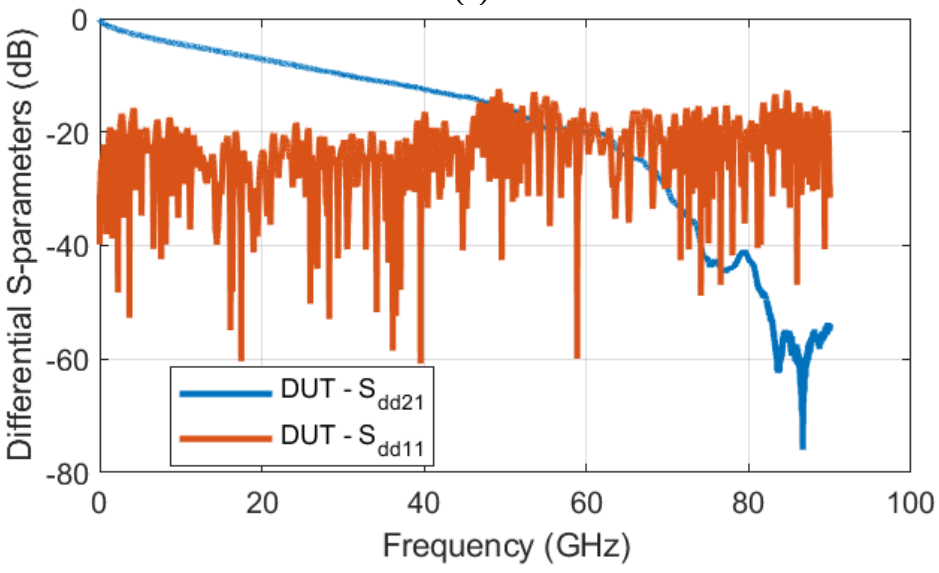
1. Device Under Test

The channel consists of a PCB-PCB assembly interconnected by a 224 Gbps NovaRay® Characterization Kit Male+Female mezzanine connector for high-speed and high-density applications as sketched in Fig. 1a [5]. This connector was designed for high-speed and

low crosstalk applications by fully shielding each differential pair. The connector itself is proven to be very reliable since each connection between the pins of the male and the female portions is ensured by two points of contact [6]. Also, the connection to the PCB is ensured by a BGA type of mounting technology, thus avoiding the need for vias. This allows minimizing the impedance discontinuities for a controlled impedance environment at the launch point. The PCBs are assembled with 1mm coaxial connectors for accessing the 32 differential pairs routed between the two PCBs, although only one differential channel is considered in the analysis carried out herein. An overview of the overall DUT is shown in Fig. 1b, whereas the differential insertion loss S_{dd21} and the differential return loss S_{dd11} of one of the pairs is shown in Fig. 1b. Assuming a bit rate of 212.5 Gb/s PAM4, it will render a 106.25 Gbaud and a Nyquist frequency of 53.125 GHz. For the channel under study, the S_{dd21} is about 14.1 dB at the Nyquist frequency The 212.5 Gb/s value corresponds to the bit rate of the signal propagating on each lane; such value lowers to the nominal 200 Gbps after applying the Forward Error Correction (FEC), also referred to as the post-FEC bit rate. The value of the S_{dd21} = 14.1 dB is a typical loss for a Chip-to-Module (C2M) type of interface as it is defined by the IEEE Project P802.3ck for Ethernet Communications [3]. Therefore, although an ad-hoc DUT for C2M verification at 200 Gbps is not yet available, the present analysis can be considered appropriate for representing the performances of a C2M interface. The physical DUT is measured up to 110 GHz with calibration performed using a mechanical calibration kit at all four ports. However, the dynamic range of the DUT at the upper frequency levels was not adequate to provide meaningful information throughout the complete bandwidth of the measurement. Therefore, the S-parameters were truncated at 90 GHz to input into the COM process characterization.



(a)



(c)

Fig. 1. Overview of the DUT (PCB – NovaRay®/Male – NovaRay®/Female - PCB). (b) S_{dd21} and S_{dd11} of one of the pairs of the DUT.

2. The Raised Cosine Filter

The use of noise mitigation techniques can be a key factor when dealing with very high data rate, as 212 Gbps, with a Nyquist frequency exceeding 50 GHz. Several aspects need to be considered, as discussed below

1. Simulations and equalization optimization by the Channel Operating Margin algorithm may require high bandwidth S-parameters. Such data needs to be measured up to a quite large limit, at least $1.3\times f_{Nyquist}$ as discussed in [4], but a larger limit may be preferable for starting with, and for evaluating the channel performances at a frequency as high as possible. However, achieving very high accuracy of VNA measurements exceeding 90 GHz may be very difficult and prone to errors, i.e. due to handling of calibration cables, small cable unbalances between the two single-ended channels. Therefore, having the possibility to cut the bandwidth where the S-parameter data starts to degrade can be very useful to avoid embedding into the simulation unwanted noise coming from the measurement setup.
2. The same issue discussed above is valid when using the channel S-parameters to analyze the channel by using simulation-based processing within the instrumentation, i.e. using the FlexDCA analyze the impact of equalization and receiver settings.
3. Small unbalances and manufacturing imperfections in the single-ended physical supports (cables, connectors, transmission lines) of the channel of interest may result in high frequency effects such as ISI and crosstalk. Such high frequency noise can be more effectively removed by a raised cosine filter at the receiver end rather than the much smoother roll-off of the 4th order Butterworth filter currently employed for lower data rates. Limiting bandwidth using the raised cosine filter is offers a degree of phase linearity as well as a high order cut-off capable of rejecting high frequency cross talk induced bounded uncorrelated noise (BUN).

The Raised Cosine (RCos) filter has a frequency response described by (1):

$$H(f)=\begin{cases}1, & |f|\le\frac{1-\beta}{2T}\\ \frac{1}{2}\left[1+cos\left(\frac{\pi T}{\beta}\left[|f|-\frac{1-\beta}{2T}\right]\right)\right], & \frac{1-\beta}{2T}<|f|\le\frac{1+\beta}{2T}\\ 0, & |f|>\frac{1+\beta}{2T}\end{cases} \quad (1)$$

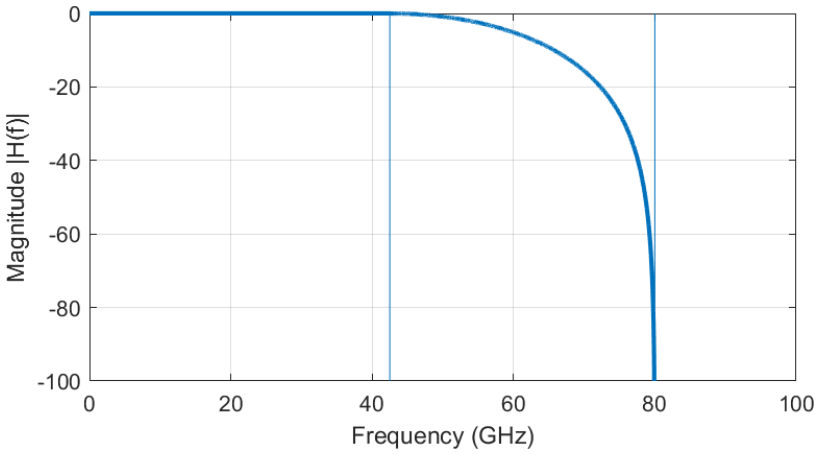
Where T is the symbol time, whereas β is the roll-off factor. Since the start f_{start} and end f_{end} frequencies are not necessarily tied to the baud rate f_b, as will be discussed in the parametric analysis in Sections 3.3 and 4, the roll-off limits f_{start} and end f_{end} can be set independently and converted into the limits in (1) by (2) and (3). This allows a more straightforward description of the RCos transfer function in (4) and is not directly dependent on the baud rate.

$$T=\frac{1}{f_{start}+f_{end}} \quad (2)$$

$$\beta = \frac{f_{end} - f_{start}}{f_{start} + f_{end}} \tag{3}$$

$$H(f) = \begin{cases} 1, & f < f_{start} \\ \frac{1}{2}\left(1 - cos\left(\frac{\pi(f_{end} - f)}{f_{end} - f_{start}}\right)\right), & f_{start} \leq f \leq f_{end} \\ 0, & f > f_{end} \end{cases} \tag{4}$$

An example of the RCos transfer function is given in Fig. 2a, with f_{start} = 42 GHz, f_{end} = 80 GHz. A comparison with the frequency response of the 4th order Butterworth filter is shown in Fig. 2b,c. Its direct impact on the channel under investigation described in Section 1 is shown in Fig. 3.



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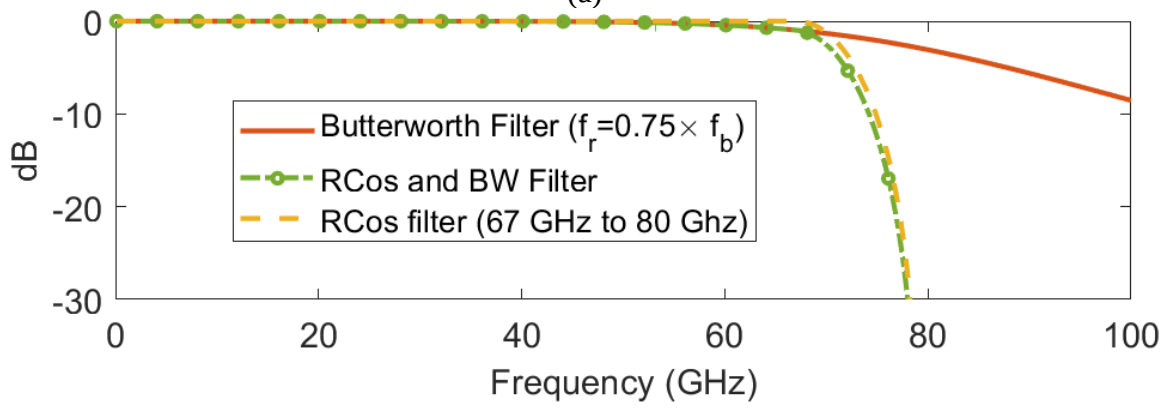
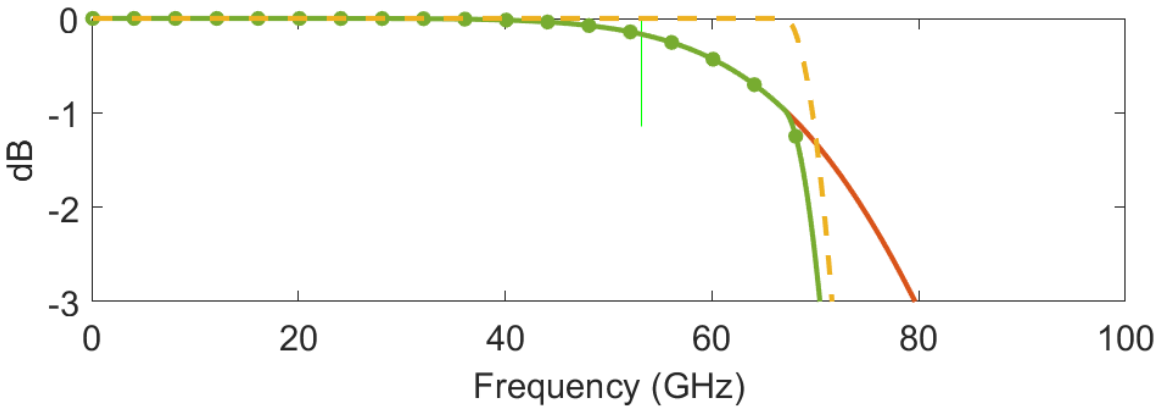


(b)



(c)

Fig. 2. Comparisons of the frequency responses of the RCos filter and the 4th order Butterworth filter.

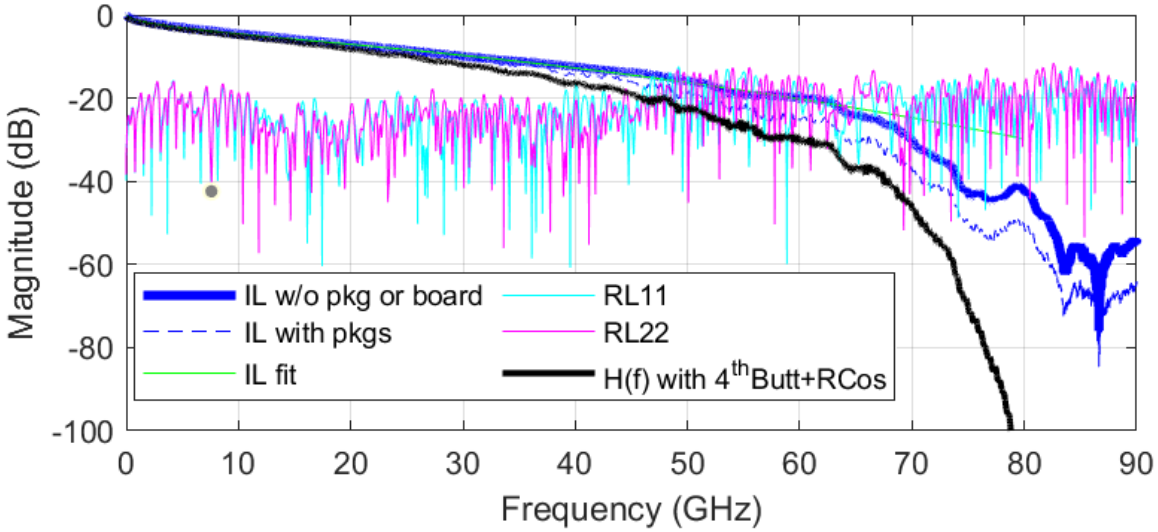


Fig 3. Impact of the RCos filter on the complete channel transfer function H(f) (no equalization is considered).

3. Time Domain (TD) Measurement Setup

Two Time-Domain (TD) measurement setups are required for the evaluation of the DUT performances through the COM algorithm. The TP0 setup is required to characterize the signal source consisting of the Keysight M8050A 120GBd High Performance BERT equipped with the M8059A 1.0mm Remote Head for an easier setup connection. The TP1a setup, in addition, includes the DUT for its performance evaluation by the scope. The receiving instrument (scope) used at both TP0 and TP1a the Keysight N1000A DCA-X Wide Bandwidth equivalent time sampling oscilloscope equipped with Keysight N1046A 100GHz Electrical Remote Sampling Head Modules- for a bandwidth of around 120GHz.

3.1 Source Characterization: TP0 Setup

The TP0 setup consists of a BERT and a Scope connected by 4 inches of low-loss instrumentation cable that is part of the source since they cannot be de-embedded from the measurements. A photo of the TP0 setup is shown in Fig. 4. The BERT generates a 106.25 Gbaud/s PAM4 PRBS13Q waveform. The scope, as required by [3], applies first a 4th order Butterworth filter with a -3dB bandwidth set at 80 GHz being ¾ of the baud-rate.

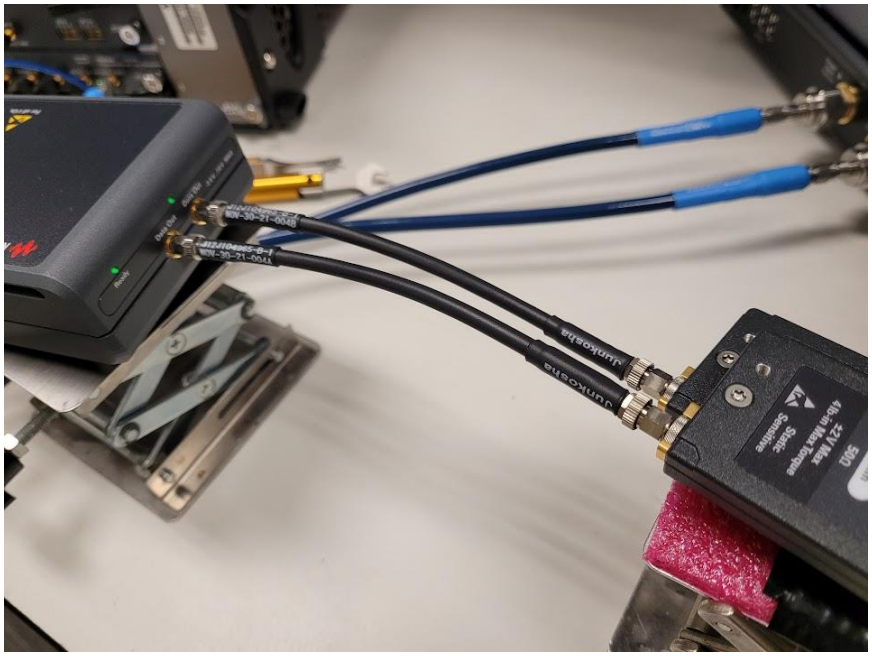


Fig.4. TP0 lab setup. The BERT remote heads are at the left side of the cable, whereas the right side of the cables are connected to the Scope remote heads.

The FlexDCA and Infiniium processing allows users to implement the math on the waveform at 106.25 Gbaud detailed into [4, 7] to extract several noise and jitter parameters, as listed below:

- Signal to noise distortion ratio SNDR = 32.8 dB
- Level mismatch ratio R_{LM} = 0.873 based on a nominal (default) level of the intermediate symbols at 33% and 66% of the signal amplitude.
- Direct extraction of the jitter amplitude based on the Dual-Dirac model A_{DD} = 270 fs that is equal to 0.029 UI.
- Measured random jitter associated to the waveform σ_{RJ} = 118 fs = 0.0122 UI

3.2 DUT Characterization: TP1a Setup

The TP1a setup includes the DUT assembly made by the PCB on one side, the multipin high-speed connector, and the PCB on the other side, with both PCBs equipped with 1 mm coaxial connectors for the source and scope connection, as described in Section 1.

An overview of the measurement setup is shown in Fig. 5, whereas the sketch of the setup with a more detailed insight is provided in Fig. 6. The 4th order Butterworth (BW) filter with a -3dB bandwidth set at 80 GHz, following the ¾ of the baud rate requirement for the 100 Gbps signaling [3] is added at the input of the scope.

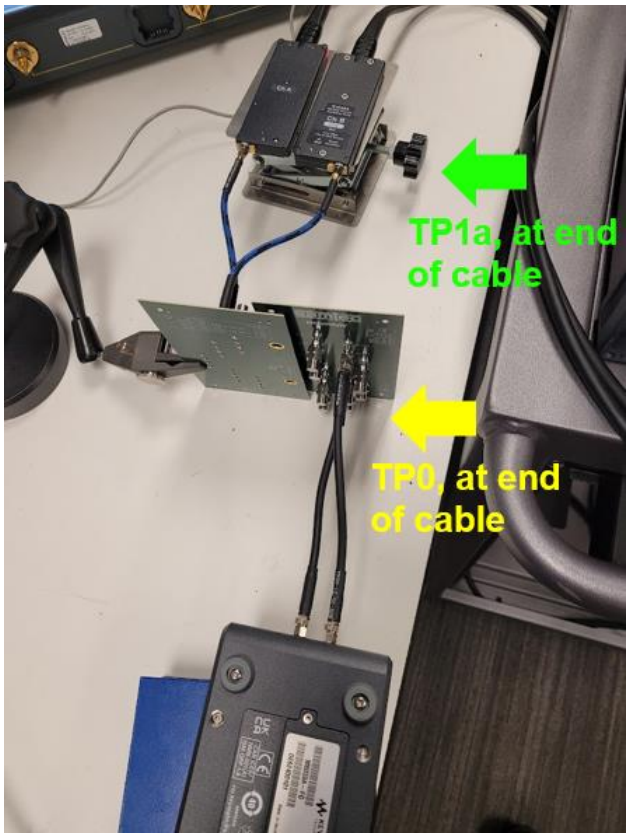
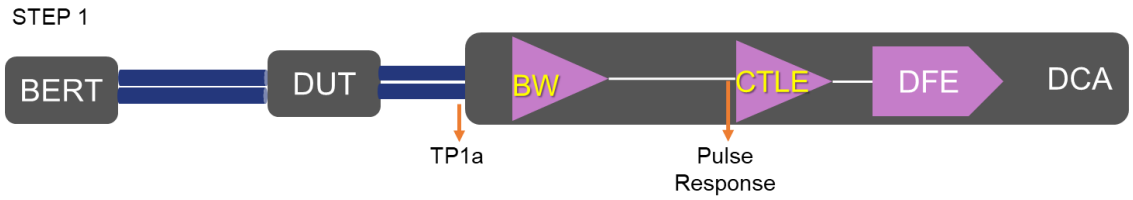


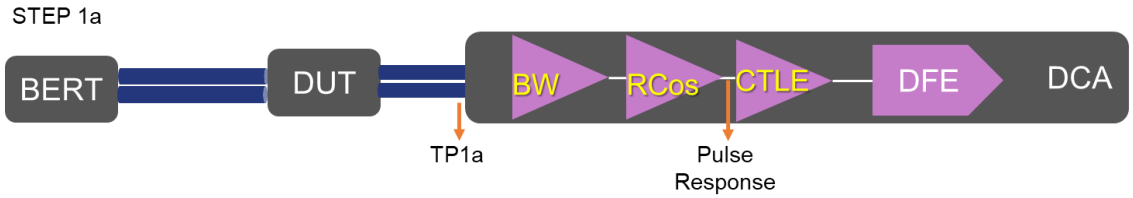
Fig. 5. Overview of the experimental setup at TP0 and TP1a.

3.2.1 Extraction of the Pulse Response from the Measured Waveform: Step 1

The key point of the setup in Fig. 6a,b is the extraction of the pulse response (PR) from the measured waveform right after the BW filter, thus ignoring, at this stage of the process, the subsequent CTLE and DFE equalization. The PR extraction is done directly by the FlexDCA mathematical processing. The PR extraction is repeated twice based on two slightly different FlexDCA setups; the setup at Step 1 in Fig. 6a includes only the BW filter, whereas the setup at Step 1a includes the RCos filter, and it is shown in Fig. 6b.. Several test cases varying the starting frequency of the RCos filter will be applied based on the Step1 setup, as discussed later. Four examples of the extracted pulse response based on Step 1 and Step 1a are shown in Fig. 7.



(a)



(b)

Fig. 6. Flowchart of the Step 1 and 1a to extract the Pulse Response from the measured waveform.

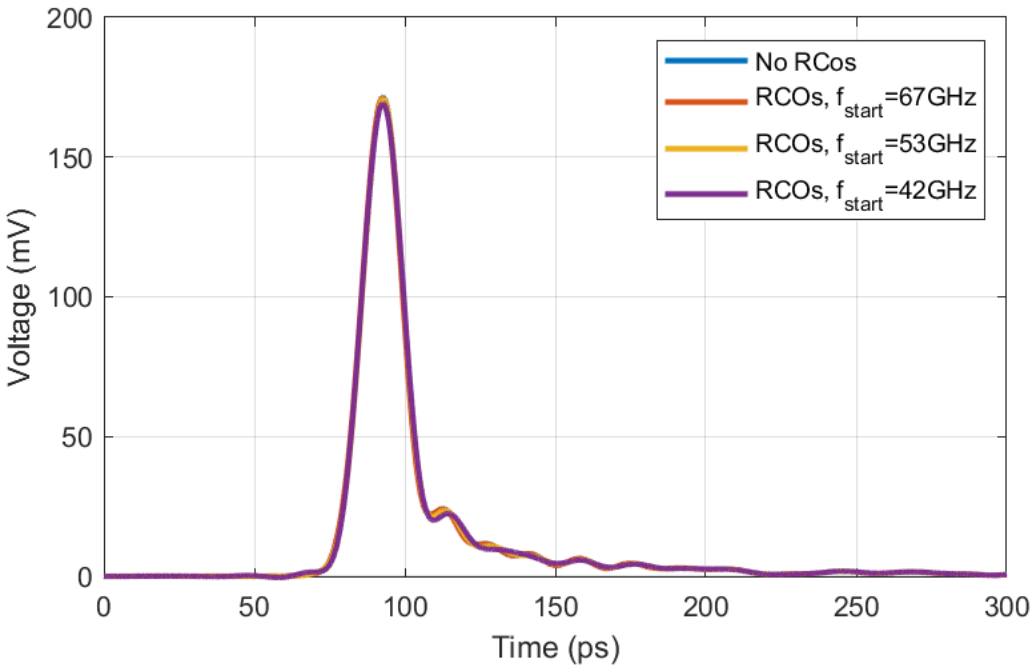


Fig. 7. Pulse response at TP1a without and with the RCos filter included within the FlexDCA processing. The f_{end} = 80 GHz for the three cases with the RCos filter included.

3.2.2 Calculation of FFE and CTLE Settings by COM: Step 2

Once the PR is extracted, it is used as the input of a modified version of the COM algorithm, which is different from the typical COM processing based on the S-parameters and based on the PR. In the Time Domain COM, instead, the impact of the DUT is embedded into the pulse response, thus the COM algorithm is able to optimize the FFE and CTLE settings according to the workflow in Fig. 8. The Step 2 is applied to both the measured PR extracted without and with the RCos filter, thus at the previous Step 1 and Step 1a.

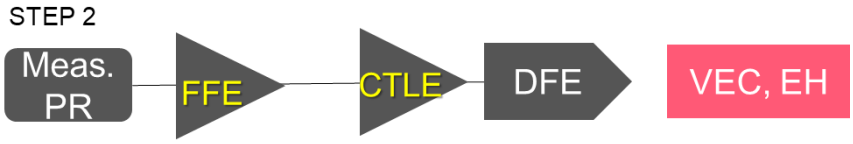


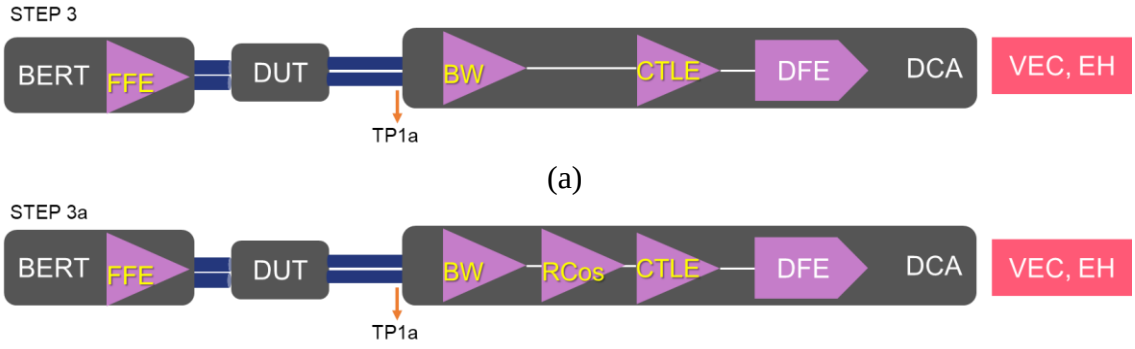
Fig. 8 Step 2: extraction of optimized equalization settings: FFE taps and CTLE g_{DC} and g_{DC2}.

Once the appropriate FFE and CTLE settings are optimized by COM, they can be applied to the measurement setup to obtain the measured eye diagram with its corresponding metrics such as VEC and EH.

However, it is found that a further refinement step is necessary in order to refine the source (BERT) characterization performed in Section 3.1. The Signal to Noise Distortion Ratio (SNDR) parameter is affected by the optimized FFE taps, since the latter may slightly reduce the signal amplitude, thus the SNDR is expected to be somewhat smaller than the original measured value of 32.8 dB. To do so, after the optimized FFE taps are set on the BERT, the measurement based on the TP0 setup is repeated once more and the updated value of the SNDR is extracted again. Therefore, the SNDR should be recomputed each time that the FFE settings at the source are modified.

3.2.3 Measurement of VEC and EH: Step 3

The last step is to bring up again the experimental setup at TP1a (thus with the DUT included) and perform the final channel characterization by extracting the VEC and EH from the measured waveform and the corresponding eye diagram, thus at Step 3 and Step 3a in Fig. 9a and 9b without and with the RCos filter included, respectively. An example of the outcome of Step 3 is shown in Fig. 10 where the DCA scope screenshot is given. The settings of the RCos filter will be discussed in the next Step 4; where the total number of taps of the DFE is set to 64, which is the maximum value currently available on the scope. However, after a careful look at the tap values that are computed based on the Pulse Response at the input of the DFE, the relevant taps are the first 12; all the other 52 have a small amplitude < 1% of the main cursor amplitude, thus they have a negligible impact on the equalized waveform.



(a)

(b)

Fig. 9. Overview of the (a) Step 3, and (b) Step3a setups.

Figure.10. Output eye diagram based on the experimental setup at Step 3.

3.3 DUT Characterization and Impact of the RCos Filter

The TP1a setup is used at Step 3 and Step 3a to characterize the DUT and to verify the DUT performances and the corresponding prediction by the COM process. The reference noise value that is added to the system is $\eta_0 = 4.1 \cdot 10^{-9}$ V^2/GHz, which is the value that may be reasonable for receivers designed for the 200 Gbps data rate. At this speed, a better Forward Error Correction (FEC) is expected to be used compared to the half data-rate standardized in [3], thus a lower Detector Error Rate (DER) value of DER = 10^{-4} is assumed in this case.

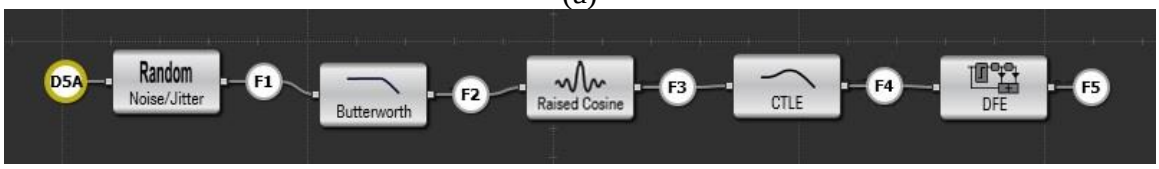
Four cases are considered and analyzed, the first one without the RCos filter, thus following the Step 3 DCA processing, and three cases with the RCos filter applied after the BW filter, based on Step 3a. In the latter case the RCos is configured to have a common roll-off frequency of f_{end} = 80 GHz, while the beginning frequency will be f_{beg} = 42 GHz, 53.125 GHz, and 67 GHz. Important note: the aim of this preliminary analysis is to investigate the impact of the RCos filter and its ability to minimize the high-frequency noise even when cutting a portion of the useful signal bandwidth.
After the application of Step 1 and 1a to get the measured PRs, Step 2 is performed to optimize the FFE and CTLE settings by COM obtaining the results in Fig. 11. Basically,

almost the same settings are found to be the optimum. The only difference is the amplitude of the main cursor c(0) and the post cursor c(1) for Case 2, where the strong impact of the RCos filter has likely reduced the signal amplitude more than the other 3 cases, thus a larger main cursor is necessary. This is also confirmed by the new values of the SNDR that are extracted by repeating the TP0 setup, as discussed in Section 3.2.2. Such values are 30.087 dB for Cases 1, 3, and 4, and 29.427 dB for Case 2, where the smaller signal amplitude led to a smaller SNDR. The CTLE gains are found to be always 0. The FFE settings are applied at the BERT according to the setup in Fig.12a, whereas the g_{DC} and g_{DC2} settings of the CTLE are applied to the complete DCA processing shown in Fig. 12b.

	RCos	f_{beg} (GHz)	f_{end} (GHz)	SNDR (dB)	FFE					CTLE (dB)	
					c(1)	c(0)	c(-1)	c(-2)	c(-3)	g_{DC}	g_{DC2}
Case 1	No	N.A.	N.A.	30.087	-0.04	0.62	-0.24	0.08	-0.02	0	0
Case 2	Yes	42	80	29.427	0	0.66	-0.24	0.08	-0.02	0	0
Case 3	Yes	53.125	80	30.087	-0.04	0.62	-0.24	0.08	-0.02	0	0
Case 4	Yes	67	80	30.087	-0.04	0.62	-0.24	0.08	-0.02	0	0

Fig. 11. Overview of the four cases considered and of the equalization settings optimized by the TD COM.

(a)



(b)

Fig. 12. (a) Implementation at the BERT of the FFE settings. (b) Procesing flow applied at the receiving waveform by the FlexDCA.

The Step 3 and 3a are performed and the results in Fig. 13a,b are obtained for the VEC and EH, respectively. The measured VEC and EH are given for the 3 eyes of the PAM4 signals, whereas the COM output provides a single value for VEC and EH. Therefore the measured three VEC and EH values are averaged and their difference with the corresponding metrics from COM are computed and reported in Fig. 13. The agreement is quite good, with a VEC difference that never exceeds 0.8 dB, whereas the difference in the EH is always smaller than 2 mV. The good agreement that is obtained by these comparisons makes the proposed process reliable and offers the possibility to further extend the RCos analysis to more cases based on COM simulations.

	RCos	f_{beg} (GHz)	f_{end} (GHz)	SNDR (dB)	Measurements				COM VEC	Diff.
					VEC0	VEC1	VEC2	Avg.		
Case 1	No	N.A.	N.A.	30.087	9.35	10	9.31	9.55	8.956	0.597
Case 2	Yes	42	80	29.427	12.1	9.26	10.5	10.62	9.845	0.775
Case 3	Yes	53.125	80	30.087	8.91	9.43	8.74	9.03	8.894	0.133
Case 4	Yes	67	80	30.087	8.99	9.63	8.91	9.17	8.988	0.189

(a)

	RCos	f_{beg} (GHz)	f_{end} (GHz)	SNDR (dB)	Measurements				COM EH	Diff.
					EH0	EH1	EH2	Avg.		
Case 1	No	N.A.	N.A.	30.087	18.1	18.2	18.9	18.4	17.7	0.7
Case 2	Yes	42	80	29.427	14.5	21.4	18.1	18.0	16.72	1.28
Case 3	Yes	53.125	80	30.087	18.9	19.4	20.0	19.4	17.73	1.7
Case 4	Yes	67	80	30.087	18.7	18.9	19.7	19.1	17.62	1.48

(b)

Fig. 13. (a) Verification of VEC results in dB for the Cases 1-4 from measurements and COM. (b) EH results in mV for the Cases 1-4 from measurements and COM.

4. Parametric Analysis and Results

A parametric analysis is carried out herein to verify the effectiveness of the proposed RCos filter. The previous validation in Section 3.3 is done based on a specific noise value of $\eta_0 = 4.1 \cdot 10^{-9}$ V^2/GHz. However, since the RCos is expected to be beneficial when large noise contribution should be mitigated, the parametric analysis will vary the η_0 from no noise to a quite large noise of $\eta_0 = 1.64 \cdot 10^{-7}$ V^2/GHz. The specific values are included into the result tables in Fig. 14. The two tables in Fig. 14a,b report the values of VEC (dB) and EH (mV).

When the noise increases it is evident that the RCos filter is very effective, although f_{beg} cannot be too low, i.e. f_{beg} = 42 GHz, otherwise too much signal bandwidth will be cut, resulting in a smaller EH and larger VEC. However, a reasonable f_{beg} value equal to the Nyquist frequency, f_{beg} = 53.125 GHz, appears to be very effective since it offers the best performances among the four cases with the smallest VEC and largest EH. The case of

f_{beg} = 67 GHz does not provide much benefit compared to the no RCos filter case, thus the best option is the one based on [f_{beg} = 53.125 GHz = $f_{Nyquist}$ - f_{end} = 80 GHz = ¾ f_b].

	RCos	f_{beg} (GHz)	f_{end} (GHz)	SNDR (dB)	COM VEC (dB)				
					η_0 (V^2/GHz) 4.1e-11	η_0 (V^2/GHz) 4.1e-9	η_0 (V^2/GHz) 4.1e-8	η_0 (V^2/GHz) 8.2e-8	η_0 (V^2/GHz) 1.64e-7
Case 1	No	N.A.	N.A.	30.087	8.843	8.956	9.942	11.182	13.706
Case 2	Yes	42	80	29.427	9.741	9.845	10.822	11.991	14.556
Case 3	Yes	53.125	80	30.087	8.792	8.894	9.911	10.876	13.194
Case 4	Yes	67	80	30.087	8.880	8.988	9.992	11.133	13.697

(a)

	RCos	f_{beg} (GHz)	f_{end} (GHz)	SNDR (dB)	COM EH (mV)				
					η_0 (V^2/GHz) 4.1e-11	η_0 (V^2/GHz) 4.1e-9	η_0 (V^2/GHz) 4.1e-8	η_0 (V^2/GHz) 8.2e-8	η_0 (V^2/GHz) 1.64e-7
Case 1	No	N.A.	N.A.	30.087	17.930	17.700	15.210	14.170	10.160
Case 2	Yes	42	80	29.427	16.920	16.720	14.940	13.060	11.120
Case 3	Yes	53.125	80	30.087	17.940	17.730	15.770	15.330	11.740
Case 4	Yes	67	80	30.087	17.840	17.620	15.110	13.250	9.500

(b)

Fig. 14. (a) VEC results in dB for the Cases 1-4 from measurements and COM. (b) EH results in mV for the Cases 1-4 from measurements and COM.

5. Discussion and Conclusions

Measurements of the 200 Gb/s PAM4 per lane and simulations with COM all show the performance improvement from the novel raised cosine filter. A modest improvement of at least 1 mV of EH and a dB of VEC were reported even though all the components and equipment targeted over 100 GHz of bandwidth. Both measurement and simulations (COM) showed the same trends. Practical applications show more improvement when chip BGA routing and crosstalk are considered [8].

The process of aligning predictions using COM computation and measurements in [4] was improved. The method utilized in this experiment consisted of acquiring the pulse response at the end of the DUT channel and output of the pattern generator (BERT) from a PRBS13Q signal waveform. The BERT pulse response and other BERT measurement of jitter, noise, and voltage parameters were supplied to perform a COM computation. The DUT channel pulse was input into the COM computation [9] as opposed to the normal way of suppling channel s-parameters. This allows the COM computation to quickly sweep the entire grid of equalization settings. The setting results were then applied to the BERT and DCA which in turn computed VEC and EH from the equalized PRBS13Q received signal waveform. VEC and EH from the COM computation compared favorably to the measured VEC and EH.

One finding proved that using TX_SNR derived from SNDR transmitter measurements for COM computations is context sensitive. In other words, adjusting TX_SNR to the SNDR measured with the transmitter FFE setting helped align COM computations to measurements.

In summary, the raised cosine filter, when properly tuned, improved VEC and EH measurements and is expected to improve even more when crosstalk and artifacts of practical design are considered. It turns out that measurements become more difficult as relevant bandwidth exceeds 70 GHz. As such, a second observation is that this filter may help to define how much measurement bandwidth is required for 200G/224 G PAM4 testing.

6. Emerging Trends

Pulse-shaping filters will continue to play a critical part in maintaining signal integrity of high-speed digital channels. Even though the majority of this technical manuscript was based on electrical signaling technology, there are currently major advances being made in the high-speed optical networking architecture. Future studies in the area of single-carrier coherent optical systems in the presence of laser phase noise are breaking new ground.

224Gbps design considerations focused on advances in equalization techniques are balanced by the strategic needs in reaching sub-4pj/bit power objectives. Proposed methods used decades ago in magnetic media related partial-response maximum-likelihood receivers and Maximum Likelihood Sequence Estimators (MLSEs) are candidate technologies in play in 224Gbps standardization. Through a combination of these and emerging methods 224Gbps will achieve improved error rate transmission across 35-40dB channels while reaching new levels in signaling efficiency.

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