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Realistic Use Cases for Edge, Angled and Vertical Launch Connectors Up to 100 GHz

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Abstract

Choosing the right coaxial connector for high frequency applications is a complex task involving trade-offs in electrical performance, size, ruggedness, ease of use, and cost. Different connector form factors such as edge mount, angled, and vertical launch offer varying benefits and drawbacks.

This paper examines the problem from multiple dimensions and provides a framework to tackle this problem. When applied, it will help improve the signal integrity of the path from the test instrument to the DUT, while minimizing the time spent in determining the best test fixturing required.

Author(s) Biography

Sandeep has 20 years of experience in signal and power integrity for IC packages, PCBs, PCB connectors and connectors for cable assemblies.

Shawn Tucker is an experienced signal integrity consultant with over 23 years in high performance system design, printed circuit board design and associated technologies, interconnect modeling and measurement, test instrumentation design, and currently focuses on RF compression mount applications.

Istvan Novak is a Principal Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution, and signal integrity design and validation methodologies for SUN's successful workgroup server families. He introduced the industry's first 25 μm power-ground laminates for large rigid computer boards and worked with component vendors to create a series of low inductance and controlled-ESR bypass capacitors. He also served as SUN's representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-nine patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website. Istvan was named Engineer of the Year at DesignCon 2020.

Gustavo Blando is a Senior Principal Engineer and leading Principal SI/PI Architect at Samtec Inc. In addition to his leadership roles, he's charged with the development of new SI/PI methodologies, high speed characterization, tools and modeling in general. Gustavo has over twenty-five years of experience in Signal Integrity and high-speed circuits.

Introduction

Why Read This Paper?

When assessing the performance of a device-under-test (DUT), the ideal scenario is to have the test equipment directly connected to the ports of the DUT. However, this approach is typically not feasible due to practical considerations. Therefore, a test fixture is used between the DUT and the test equipment. The test fixture usually consists of a combination of connectors, cables, and printed circuit boards (PCBs). The key requirement for the test fixture is that it must be electrically transparent—meaning it should not affect the measurement results—across the full bandwidth of the measurement being made.

Measuring the performance of a device under test accurately requires precisely de-embedding the measurement fixture all the way to the ports of the device. This concept is illustrated in Figure 1, which shows an example of a test fixture and its corresponding cartoon schematic. It shows that components like the cable, coaxial connectors, PCB traces and vias need to be effectively removed from the measurement to accurately gauge the DUT's true performance. This is particularly important for measurements that require high bandwidth, such as 112G and 224G testing. Many engineers performing 224G characterization, are targeting test bandwidth in the 70-90 GHz range [1], [2].

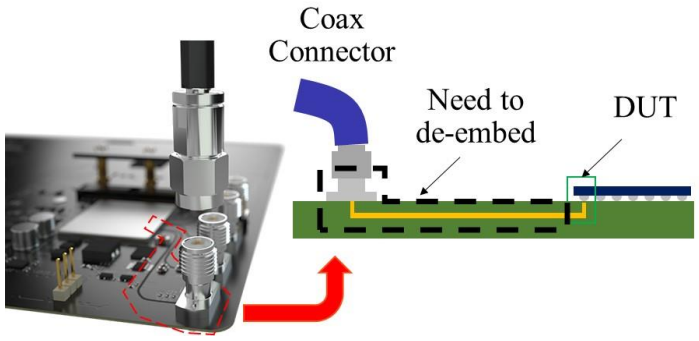

Figure 1: Measuring DUT performance accurately requires de-embedding the measurement fixture.

The paper suggests a holistic approach to the design of test fixtures. This approach ensures that testing of the DUT is not compromised by the fixture itself and remains accurate up to the highest frequency of interest.

Paper Assumptions

No single study can exhaustively cover every type of connector used in high-frequency applications. In our experience, high frequency setups employ 2 common types – edge mount connectors and vertical launch connectors. Edge mount connectors are aligned parallel to the PCB and mounted along its edge, as shown in Figure 2(a). Vertical launch connectors, which are set at an angle to the PCB surface, offer placement flexibility and can be located anywhere on the board, with examples depicted in Figure 2(b). Each of these connector types can also be in a ganged format to reduce the physical area needed for multiple connections. Examples are of ganged RF connectors are shown in Figure 2(c) [3], [4].

For any connector type, contact to the PCB can be through either soldering or pressure. This paper is focused on compression mount connector implementations. Soldering high frequency connectors

presents a series of additional challenges. For further information and an in-depth look at soldering techniques and their associated challenges for RF connectors, please see references [5] and [6].

Figure 2: Examples of (a) edge mount, (b) vertical/angled and (c) ganged connectors

Key Takeaways

1. Provide a high frequency coaxial interface as close to the DUT as possible to provide a calibrated reference plane. Even when getting close to the DUT requires ganged coaxial connectors, which cannot be calibrated with calibration standards at their PCB interface, the lower loss of cable enables de-embedding algorithms to remove the cables cleaner than PCB traces of similar length. For example, see Figure 7. It shows that the loss of coaxial cable is significantly lower than that of PCB trace. This is true even when using wide striplines, available using skip layer routing (Skip layer striplines reference planes that are farther away than the closest planes).
2. Use PCB stackup technologies that prevent waveguide modes below stripline via launches. This will help reduce the return loss at higher frequencies.

Incorporating these strategies into your design allows de-embedding with the widest possible bandwidth. In the remainder of the paper we will explore the reasoning behind these strategies, starting with methodologies for achieving optimal de-embedding bandwidth. To do this, let us first explore what limits de-embedding bandwidth.

Obtaining Widest Possible De-embedding Bandwidth

There are very few cases where the entire fixture up to the DUT interface can be calibrated out using mechanical or electronic calibration kits. In most cases, there is come combination of cables, connector launches, traces and vias that need to be de-embedded from the measurement of the DUT.

There are multiple de-embedding algorithms that can be used to remove fixturing contributions from measurements [7], [8], [9]. Different de-embedding algorithms have their strengths and weaknesses [10]. However, all the algorithms work better [11] when:

(a) Fixture insertion loss (IL) is lower.
(b) There is greater separation between IL and return loss (RL)

For accurate DUT measurements, therefore, **the test fixture should have the lowest IL and RL possible over the frequency range of interest**.

IL is directly correlated to the length of the fixture that needs to be de-embedded. In the next section, we look to get a sense of the physical sizes imposed on the test fixture by the choice of connector and how the loss of the fixture can be minimized.

RL is heavily impacted by the performance of transitions (connector to PCB and DUT to PCB being the primary examples). The impact of these launch transitions is investigated in subsequent sections.

Minimizing Fixture IL

To setup a common baseline to compare the different connector types, consider the following use case. Since both QSFP-DD800 [12] and OSFP [13] support 8 high speed diff. pair lanes, let's assume that 8 electrical lanes or 16 diff. pairs need to be routed to the DUT. Additionally, let's assume that the high-speed diff. pairs are all on one side of the DUT. Since the IL that needs to be de-embedded is proportional to the distance that cannot be calibrated out, let us distinguish the calibration reference plane from the de-embedding plane.

- The calibration reference plane is the point at which the NIST traceable, calibration reference plane can be defined. For current purposes the calibration reference plane is assumed to be the plane up to which a mechanical, coaxial calibration kit can be used.
- The ideal DUT measurement plane would be the launch of the DUT. However, this is a location where complex field interactions take place, making it difficult to make repeatable measurements. Instead, we define the DUT measurement plane to be 1 mm or so away from the DUT launch, where a good TEM reference plane can be defined (see hollow green box in Figure 1).

Under these conditions let us examine the physical distance that needs to be de-embedded for the different connector styles.

a) Vertical Launch Connectors

Vertical launch connectors (VLCs) are not limited to any particular area of the PCB. This means we need to look at a couple of different arrangements. Figure 3 is one possible arrangement, where all the connectors are the same distance from the center of the PCB. The DUT is assumed to be at the center of the PCB and since all the high-speed signals are assumed to be on one side of the DUT, the PCB is only a semicircle, not a full circle. Figure 3 shows that the center-to-center distance the two farthest VLCs is approximately 6.1 inches, which means the distance from the VLC to the DUT is 3 inches.

Figure 4 shows another possible arrangement of connectors for the VLC case. In this case all the connectors are not equidistant. The connectors are arranged in 2 rings – an inner and outer ring. By offsetting the connectors, the overall diameter of longest signals is reduced by 40%. This helps reduce the overall IL that needs to be de-embedded significantly. However, because the IL for the inner ring is different than the IL for the outer ring, the de-embedding process needs to account for this.

The physical floor planning of angled connectors is very similar to that of individual VLCs as described in the previous paragraphs.

Figure 5 is third possible arrangement of VLCs. This is the densest possible arrangement because it is a ganged connector arrangement, without the need for mounting hardware for each channel. Figure 5 shows, for example, that a 2x8 array of connections occupies a 28 mm x 6.85 mm area of the PCB and

that it can be placed right next to the DUT. This results in minimal trace length between the connector and the DUT. This minimum distance is usually only limited by the physical size of the DUT socket. Ganged connectors, like the ones shown in Figure 5, need not even be in a rectangular form factor.

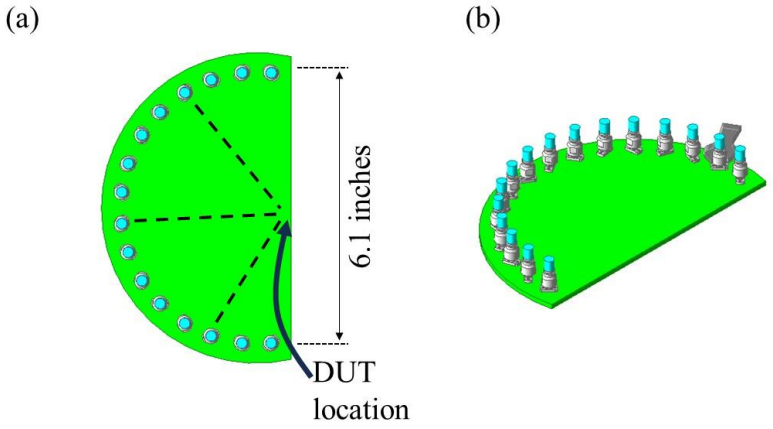

Figure 3: 16x VLCs placed equidistant from the DUT. The distance between the VLCs is large enough to allow a torque wrench room to tighten connections. Example routes shown by "-" lines.

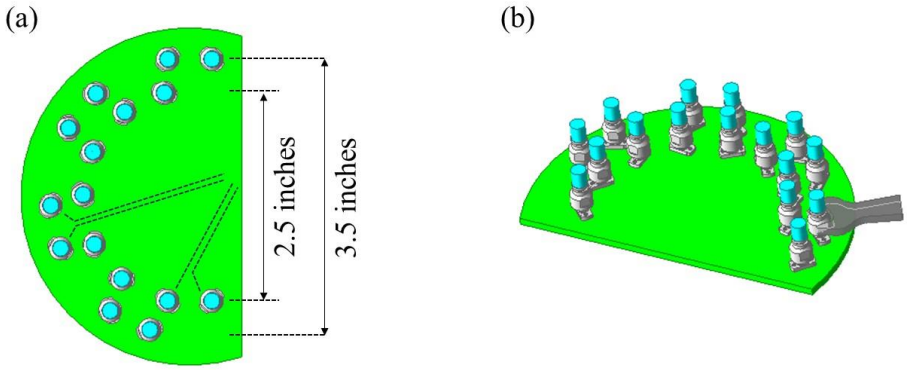

Figure 4: (a) 16x VLCs placed at 2 distances from the DUT. Example routes from inner and outer distances shown by "-" lines. Differential routing assumed, and (b) Connectors layout shown with space provided for a torque wrench to tighten connections.

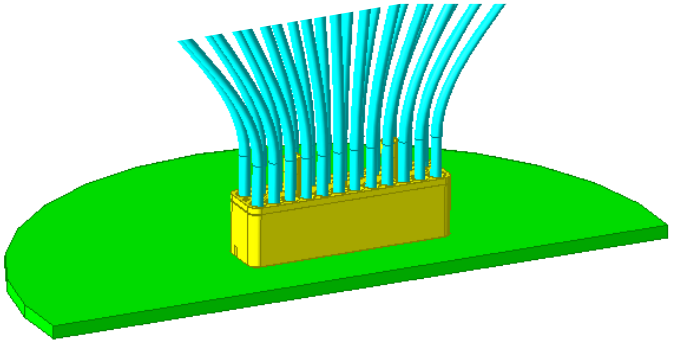

Figure 5: An array connector with 16 signals arranged in 2 rows.

Their housing shape can be changed to match the perimeter of the DUT to ensure that the distance to every channel of the DUT remains very close to the same. While the trace length is minimized with ganged VLC connectors, they usually do not have the ability to be calibrated at their PCB interface. The calibration reference plane is usually at the other end of the connector, at the end of the coax cable. This length of cable along with the trace on the PCB need to be calibrated out of the measurement.

b) Edge Connectors

Edge connectors are very familiar to most SI engineers. When used with small PCBs, they allow multiple PCBs to be placed one after another on a bench, in a daisy chained configuration. With larger boards however, their need to be placed only at the edge of the PCB can constrain the physical size of the PCB. Figure 6 shows the edge connector configuration for the case under discussion. Very similar to when the VLCs were all placed equidistant from the DUT, the distance from the edge connector to the DUT is about 3 inches. Unlike the VLC case however, there is no other configuration of edge connectors that can reduce this distance.

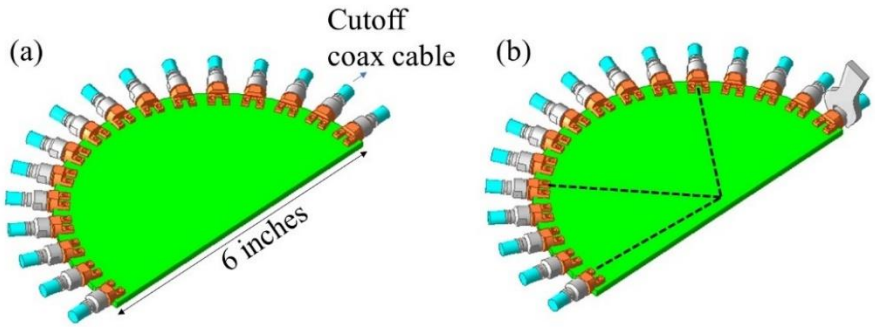

Figure 6: (a) 16x edge mount connectors and (b) Edge mount connectors spaced so a torque wrench can be used. Trace route paths shown by "-" lines.

The discussion above shows that tradeoffs can be made between connector types and the distance to the DUT that needs to be de-embedded. To fully comprehend these tradeoffs, we need to discuss what knobs are available to minimize the IL for the fixturing interconnects that are to be removed using de-embedding.

Figure 7 is a good place to start to understand the relative contribution of routing loss of different controlled impedance structures. It shows the insertion loss difference between low loss cables of 2 different diameters and a low loss PCB trace. The difference in attenuation is stark! While the larger diameter coax cable has a slightly lower loss than the smaller diameter (0.047") coax, either coax is much, much lower loss than the PCB trace. Key takeaway: **Design your fixture to cover most of the distance to be de-embedded with coax cable rather than PCB trace.**

If, however, you cannot minimize the amount of trace in the fixture, it is no secret that going with low loss dielectric materials, the smoothest copper and the widest line width is the best way to reduce trace loss. There are limitations on what is achievable though. Let us examine some of the tradeoffs that need to be considered.

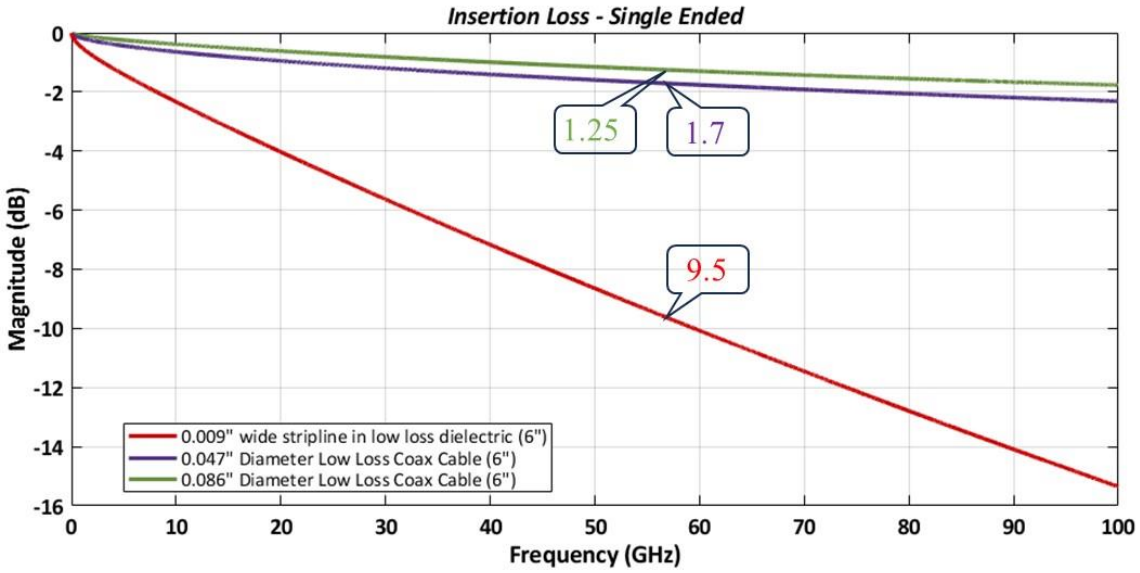

Figure 7: Loss of 6" of trace vs. coax

When considering inner layer routing, we must account for the vias that connect the stripline to its endpoints. Methods to minimize the RL of vias will be looked at in detail in the next section, but for now we assume a narrow microvia is needed for the high bandwidth via transition. Small diameter microvias are very desirable, but from a PCB fabrication perspective, they are very limited in terms of aspect ratio. Frequently they have to be wider than they are deep i.e., the height to width aspect ratio is typically in the 0.75:1 to 1:1 range. This poses a problem. To get a wide line while maintaining a fixed impedance (be it 50 Ohms single ended or 100 Ohms differential), we need thick dielectrics. Thick dielectrics mean even larger diameter microvias. This limits bandwidth. Small diameter microvias have lower return loss but mean thin dielectrics and lossy traces. A no-win situation! Figure 8 shows three different PCB stackups that attempt to make the best tradeoff between microvia size and stripline linewidth.

(a)

Layer Number	LayerName	Material	Thickness (mils)
	TOP_SM	PSR-4000-HFX	0.71
1	TOP	PLATED COPPER (0_5oz)	2.48
	CORE01	TACHYON 100G (2x1067) (66_5%) C	4.02
2	S02	COPPER (0_5oz) VLP2	0.59
	DIEL01	TACHYON 100G (2x1067)(74%) PP	4.69
3	P03	COPPER (0_5oz) VLP2	0.59
	CORE02	TACHYON 100G (3x1078)(68_5%) C	10
4	P04	COPPER (0_5oz) VLP2	0.59
	DIEL02	TACHYON 100G (2x1067)(74%) PP	4.69
5	S05	COPPER (0_5oz) VLP2	0.59
	CORE03	TACHYON 100G (2x1067) (66_5%) C	4.02
6	BOTTOM	PLATED COPPER (0_5oz)	2.48
	BOTTOM_SM	PSR-4000-HFX	0.71
Total thickness over solder mask and plated copper			36.16

(b)

Layer Number	LayerName	Material	Thickness (mils)
	TOP_SM	PSR-4000 HFX DI	0.71
1	TOP	COPPER_FOIL_HA	2.52
	DIEL01	FR-27-0040-43F (100%) PP	3.58
2	P02	COPPER_FOIL_HA	1.89
	DIEL02	FR-27-0040-43F (100%) PP	3.82
3	S03	COPPER (0_5oz) ULP	0.59
	CORE01	EZ-IO-F-0050 (1x1067) (90%) C	5
4	P04	COPPER (0_5oz) ULP	0.59
	DIEL03	FR-27-0050-40 (S) (100%) PP	5.79
5	P05	COPPER (0_5oz) ULP	0.59
	CORE02	EZ-IO-F-0050 (1x1067) (90%) C	5
6	S06	COPPER (0_5oz) ULP	0.59
	DIEL04	FR-27-0040-43F (100%) PP	3.82
7	P07	COPPER_FOIL_HA	1.89
	DIEL05	FR-27-0040-43F (100%) PP	3.58
8	BOTTOM	COPPER_FOIL_HA	2.52
	BOTTOM_SM	PSR-4000 HFX DI	0.71
Total thickness over solder mask and plated copper			43.19

(c)

Layer Number	LayerName	Material	Thickness (mils)
	TOP_SM	PSR-4000 HFX DI	0.71
1	TOP	PLATED COPPER (0_33oz)	1.5
	DIEL01	EM-892BK (1x1078) (67%) PP	2.99
2	S02	PLATED COPPER (0_33oz)	0.98
	DIEL02	EM-892BK (1x1078) (67%) PP	2.99
3	S03	PLATED COPPER (0_33oz)	0.98
	DIEL03	EM-892BK (1x1078) (67%) PP	2.99
4	S04	PLATED COPPER (0_33oz)	0.98
	DIEL04	EM-892BK (1x1078) (67%) PP	2.99
5	S05	COPPER (0_5oz) ULP	0.98
	CORE01	EM-892K (1x1078) (63_5%) C	2.99
6	S06	COPPER (0_5oz) ULP	0.98
	DIEL05	EM-892BK (1x1078) (67%) PP	2.99
7	S07	PLATED COPPER (0_33oz)	0.98
	DIEL06	EM-892BK (1x1078) (67%) PP	2.99
8	S08	PLATED COPPER (0_33oz)	0.98
	DIEL07	EM-892BK (1x1078) (67%) PP	2.99
9	S09	PLATED COPPER (0_33oz)	0.98
	DIEL08	EM-892BK (1x1078) (67%) PP	2.99
10	BOTTOM	PLATED COPPER (0_33oz)	1.5
	BOTTOM_SM	PSR-4000 HFX DI	0.71
Total thickness over solder mask and plated copper			39.17

Key
Reference Layer
Routing Layer

Figure 8: Three PCB cross-sections that try to increase IL-RL separation through different mechanisms. (a) XS0040; (b) XS0052; (c) XS0056

Figure 9 shows the IL differences between the 3 stackups. Figure 8(a) shows the baseline stackup called XS0040. It uses a low loss dielectric that is 4 mils thick, which resulted in 5 mil wide lines and

necessitated the use of 6 mil diameter laser drilled microvias. To improve the IL, XS0052 (Figure 8(b)) went with non-reinforced Taconic FastRise 27 prepreg and EZIO-F cores to allow a wider line (8 mil). While IL did improve, limitations of what prepregs are laser ablatable in combination with limitations on the diameter of the microvia the fabricator imposed, limited the RL possible in the launch for XS0052. The performance of these launches is covered in a previous paper [14]. To increase the de-embedding bandwidth even further, XS0056 (Figure 8(c)) went back to glass reinforced, EM-892K dielectrics. EM-892K has a greater selection of dielectric thickness that are laser ablatable and they can be double stacked too. This combination allowed XS0056 to use 4 mil microvias and a wide line (7.6 mil)! One point to note here is that because stacking microvias require the use of foil Copper layers in the stackup, the copper in XS0056 is not as smooth as in XS0052. The tradeoff was still worthwhile though, because the slight reduction in IL in XS0056 compared to XS0052 was more than compensated for by improved RL of the vias, resulting in a much higher de-embedding bandwidth. The results are shown in a later section.

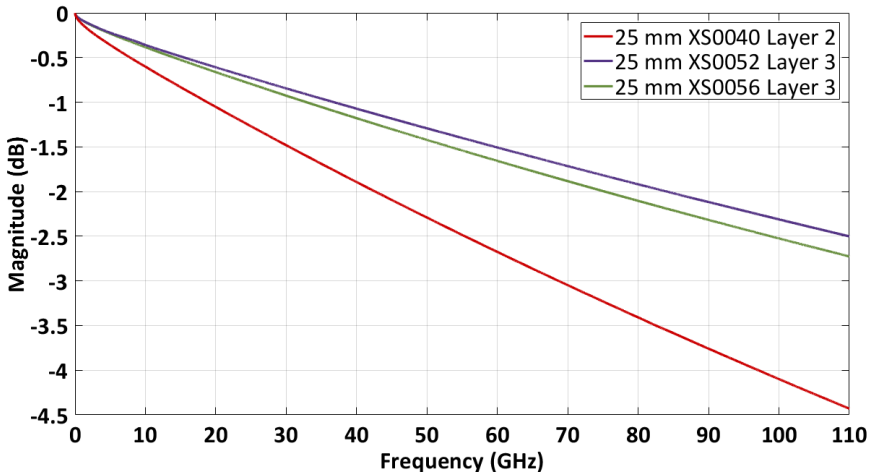

Figure 9: Insertion loss differences between the stackups shown in Figure 8

In summary, moving the test instrumentation as close to the DUT as possible is the goal. That said, given the much larger loss of PCB trace compared to test grade coax cable, **using coax to get as close to the DUT as possible to have minimal PCB trace** is the target to shoot for. In addition, using PCB stackups that provide the **best tradeoff between trace loss and return loss of via transitions** will provide the widest frequency performance test fixtures.

To make the best tradeoffs, we need to understand what limits the RL of connector to trace transitions and what knobs we have at our disposal.

Minimizing Fixture RL

When considering how to minimize the RL of connector transitions, it is first important to draw a distinction between the “footprint” of a connector and the “launch” under the connector.

The footprint refers to the minimum dimensions and clearances required to instantiate a connector on a PCB. An example vertical launch connector and its footprint are shown in Figure 10 (a) and (b). It is based on mechanical dimensions and tolerances and speaks nothing of the actual performance of the

connector transition a particular PCB. Figure 10 (c) shows the top view of the electrically tuned launch of this connector on a PCB. Clearly, there is a lot more going on in the electrically tuned launch than in the footprint.

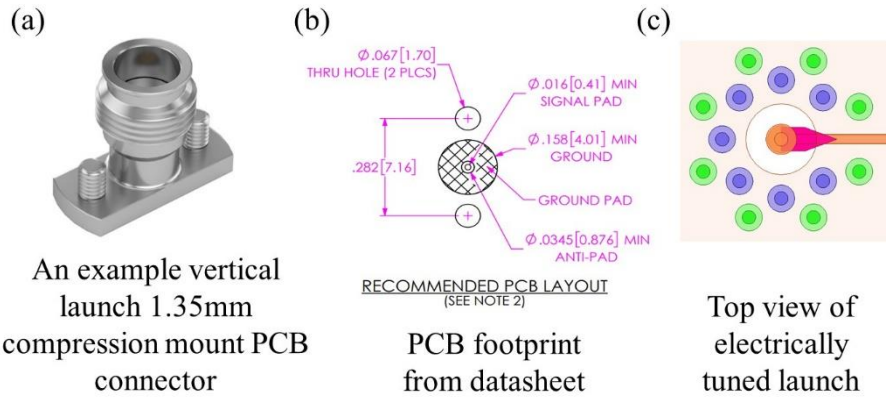

Figure 10: (a) 1.35 mm VLC example, (b) mechanical footprint and (c) tuned launch of the connector

The launch in Figure 10 transitions into a stripline. A via-in-pad design is assumed here. If a thru via is used instead, except for the case when the signal layer is on the opposite side of the board, a via stub extends from the signal escape layer to the bottom of the board – assuming the connector is on top side. Such via stubs can negatively impact high-frequency performance, as they are not ideal for signal integrity at high speeds.

To mitigate the adverse effects of via stubs, backdrilling is utilized. This technique involves using a drill, larger than the diameter of the signal via and its pads, to remove as much of the stub as possible. However, the backdrilling process is not perfect. To avoid damaging the connection between the trace and the signal via, backdrilling typically stops before the signal escape layer. The length of the remaining stub depends on the PCB manufacturer's capabilities. In the context of high-speed data rates, it is crucial to have the shortest possible stub to minimize signal degradation. Figure 11 illustrates the impact of a non-zero via stub on performance.

Figure 12 provides an alternate way of looking at the information in Figure 11. It presents the frequency at which the connector launch's return loss reaches 15 dB—a threshold selected because launches lower return loss performance than this are likely to have a negligible effect on the signal quality. The graph indicates that a stub length under 4 mils has an essentially negligible impact on launch bandwidth, whereas an 8-mil stub can lead to a bandwidth reduction of about 10%. For even longer stubs, performance deteriorates rapidly. Thus, understanding the capabilities of the PCB fabricator's backdrilling precision is crucial.

It's also vital to consider the tolerance specified by the fabricator for the via stub length. For instance, if a fabricator claims a backdrill stub length of 6 mils with a tolerance of ±4 mils, the actual stub could range from 2 to 10 mils. While a 2-mil stub might have negligible performance degradation, a 10-mil stub would need to be compensated for in the design to minimize its deleterious effect. The problem here is the following: Suppose the design is adjusted to compensate for a 10-mil stub, but the board is produced with a 2-mil stub instead; this would lead to an overcompensated design, resulting in poor

signal integrity. Figure 13 depicts the impedance profile for a trace-to-via transition with compensation for a 10-mil backdrill stub. The compensation aims to counteract the impedance discontinuity of the 10-mil stub. It is quite effective, because the impedance mismatch with a 10-mil stub is minimal (within ±1 Ohm). However, if the actual stub is only 2 mils long, the transition appears excessively inductive.

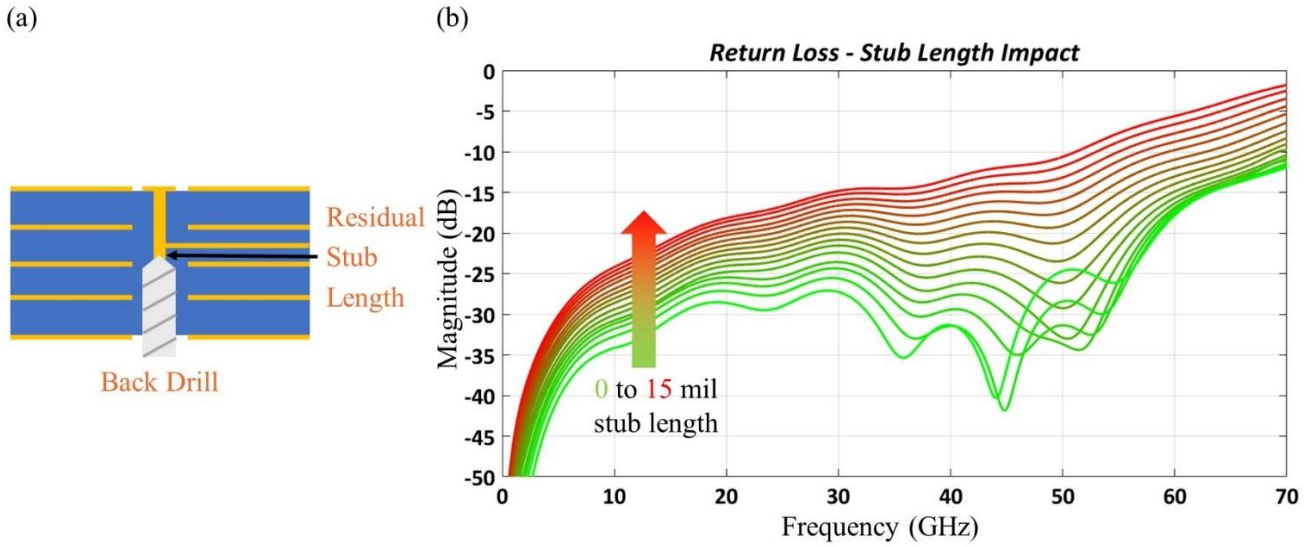

Figure 11: Degradation of performance as backdrill stub increases

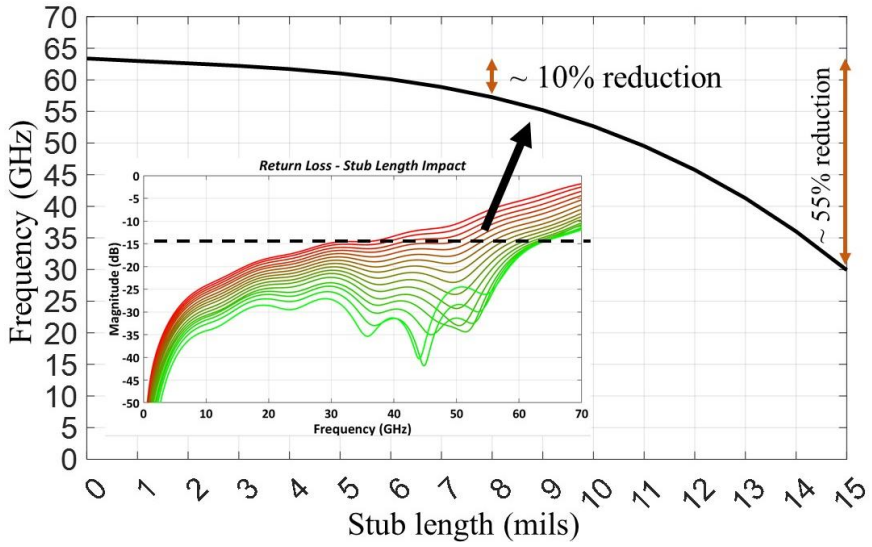

Figure 12: Reduction in the frequency at which RL crosses 15dB as a function of stub length

The better solution here is to use a blind via, which would eliminate the need for backdrilling altogether. This would ensure that there are no stubs to affect the high-frequency performance of the launch.

Another useful guideline to remember when designing connector launches is to mimic the size of the connectors themselves. What does this mean? Precision coaxial connectors, in general, get smaller the higher their working frequency [16]. One of the main drivers is that we only want one electromagnetic mode of signal propagation in the test signal path. If multiple modes can propagate simultaneously,

signal distortion will be the result. The minimum frequency necessary to excite higher order modes is inversely proportional to the dimensions of the signal transmission structure. To get to bandwidths, close to 100 GHz, the diameter of the launch must be on a similar order to that of a 1 mm connector. This is a rough guideline to provide some perspective. Launch design is explored in significant detail in a previous paper [14]. The most pertinent aspect of the discussion from [14] to the current discussion is shown in Figure 14.

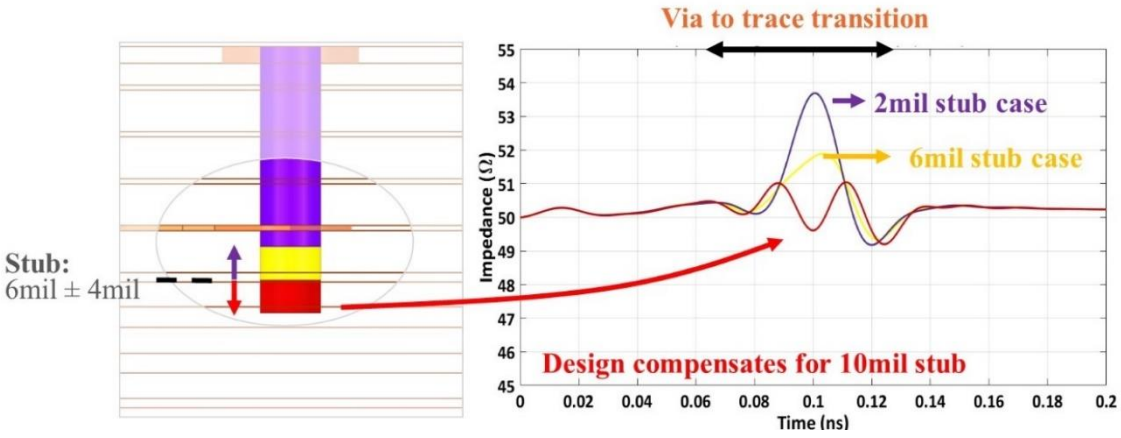

Figure 13: Large via stub tolerances in a PCB can result in an inability to provide adequate compensation.

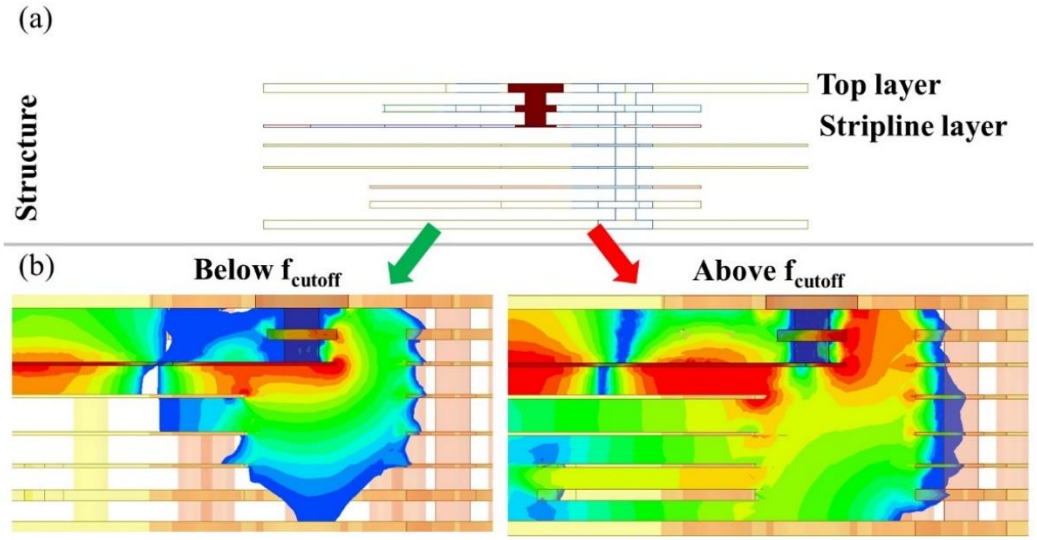

Figure 14: (a) A stripline launch and (b) electric field magnitude plots below and above the cutoff frequency for higher order modes to propagate in the launch area

Figure 14(a) shows the cross-section of a stripline connector launch, which consists of a layer 1 to layer 3 blind via transitioning to a layer 3 stripline. To provide a better broadband impedance match, several of the reference plane layers below the via have been opened up with circular antipads. The openings mean the signal energy sees all the plane cavities in the board. At low frequencies the waveguide formed by the openings is "cutoff". This means energy cannot propagate in the waveguide and so the energy stays confined in the stripline layers. At higher frequencies, energy can propagate through this

waveguide to the plane cavities and so the energy, instead of being confined just to the stripline layers can propagate through all the plane cavities beneath the launch. These 2 scenarios, energy flow in the structure above and below the cutoff frequency of the waveguide are shown in Figure 14(b).

Once the signal energy can propagate through paths other than just the stripline, the RL gets worse because the impedance is now the combination of the impedance of possible signal different paths and the IL gets worse too because energy that is going down the plane cavities is not coming back to the stripline connection at the other end of the line. In combination, the IL to RL gap starts closing quickly. This in turn starts limiting the de-embedding capability and the fixture starts becoming opaque.

To move the cutoff frequency higher, beyond the bandwidth of interest, it is useful to look at the structure created by the return vias of the launch below the stripline layer. As seen in Figure 15(a), they form a circular waveguide structure. The smaller the diameter of the structure and the lower the dielectric constant of the medium inside the waveguide, the higher the cutoff frequency [14], [17]. A point to note: The ε_r in the formula is the dielectric constant in the X-Y plane [14], [15].

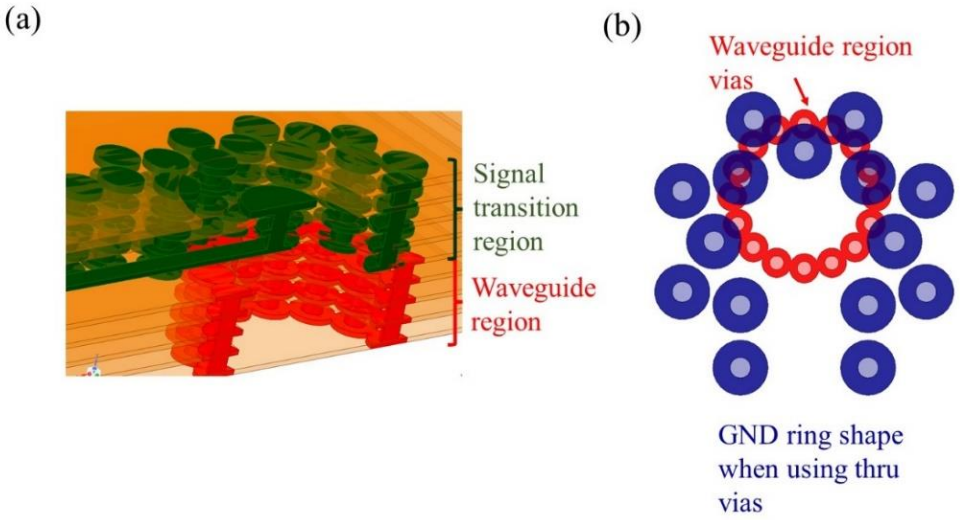

Figure 15: (a) PCBs using ELIC can completely close off the waveguide created under a stripline launch (b) Overlay between GND ring size when using thru vias and GND ring size in the circular waveguide section when using ELIC. ELIC allows for a smaller, fully closed ring.

Let's consider both these knobs.

(1) Reducing the diameter of the structure: If we assume the return vias are thru vias, then when the diameter of the GND ring is reduced, the signal via diameter must decrease as well. Otherwise, the impedance of the via transition will be compromised, resulting again in poor RL. There are limitations on how small the via diameter can be made depending on the via aspect ratio limits imposed by the PCB fab and the thickness of the dielectric used. Usage of thru vias also has the disadvantage that they cannot be placed where the trace escapes, creating an opening in the GND ring (see Figure 15(b)). No matter how tightly the GND vias are placed, this opening will allow signal energy to escape into the plane cavities below the reference layer and cause poor RL.

To push out the cutoff frequency higher, a different technique can be used – an Every Layer Interconnect (ELIC) technology [18], [19]. ELIC refers to PCB technologies that allow microvias for every layer transition, thus allowing very high-density routing. That means the vias in each layer are independent of the ones above and below. This allows the return vias in the layers below the stripline transition to be placed closer together than the vias in the signal transition region. Therefore, the cutoff frequency of the waveguide created under the launch can be tuned independently of the GND ring in the launch area. In addition, as shown in Figure 15(a), (b), the waveguide portion below the launch can be completely enclosed with vias. This prevents signal energy from propagating into the plane cavities. Figure 15(b) highlights another important point. ELIC vias only have to penetrate one dielectric layer. That allows them to use smaller drill and pad sizes, allowing them to be more compact than structures built with thru vias.

(2) Reducing the ε_r: This is another route to take when trying to improve the launch bandwidth. Naturally, going with a lower dielectric constant material will help. Keep in mind though that glass reinforced laminates tend to be anisotropic because the dielectric constant of the glass and resin are different from each other. Choosing laminates with lower anisotropy when using the same resin system is also beneficial in reducing the dielectric constant (lower ε_r fiberglass or higher resin content).

A further way to reduce the dielectric constant in the waveguide section of the launch is to increase the amount of air in the region by backdrilling the region with a large drill. The more material that is removed, the closer the overall ε_r will be to air and the higher the cutoff frequency of the waveguide. Drill to copper clearances required by the PCB shop will limit the diameter of the drill that can be used. Backdrill tolerances will also come into play in how close to the launch layer material can be removed. Simulating the performance of the launch with consideration to these factors is needed to ensure the performance is acceptable over the frequency range of interest.

In summary, the goal is **to shrink the cross-sectional size of the launch via structure as much as possible**, which still going through a thick dielectric (for increased trace width) and making sure all the waveguides in the vicinity of the launch are in cutoff over the bandwidth of the launch.

With this background, let's examine how the different connector types impact the RL performance of the launch.

Flavor 1(a): Vertical Launch

With vertical launch connectors, the launch is directly below the connector itself. The end of the connector and the top part of the launch heavily influence one another. Since the inside of the connector, near the PCB, is usually an air cavity for compression mount connectors, managing the transition from air to the dielectric medium of the PCB can be difficult. Using 4 mil microvias for the signal via has significant advantages when the goal is to have excellent performance up to 100 GHz.

The keys to keeping RL low for VLC launches are:
- Small signal pin diameter
- Microvias
- Staggered, blind GND vias below the signal trace layer

Flavor 1(b): Ganged Vertical Launch

All the design principles that apply for individual vertical launch connectors apply here as well. There are two additional considerations when using ganged connectors.

1. Since adjacent channels tend to be close to each other, the GND via structures for each channel need to be dense enough to limit channel-to-channel crosstalk. If the vias can't be close enough to form an electrical wall, consider using two interlocking rings of vias, with the vias in the outer ring placed in the gap between the vias of the inner ring.
2. With compression ganged connectors, some type of backer plate is often needed for mechanical rigidity. There are usually channels grooved into the backer plate to prevent shorting or excessive capacitive loading on the bottom side of the PCB. These backer plate channels can form waveguides in the 60-70+ GHz range. Unless the launch design allows the bottom return plane of the PCB to be completely closed or the circular waveguide below the launch is in cutoff for the whole frequency range of interest, this can become a source of significant high-frequency crosstalk.

   Figure 16 shows a measured example of this. Measurements were performed on a Keysight N5227B VNA with 110 GHz extension heads. The crosstalk was measured at the PCB VLC connectors. The cable ends of the compression mount connectors were terminated with 50 Ohm terminations. When the crosstalk is measured between two channels whose launches are closed on the bottom layer of the PCB, the level of crosstalk seen is the same as the noise floor of the VNA. When the bottom side of the PCB is open though, enough energy can leak through the launch to the channel in the backer plate, use the backer plate channel as a waveguide and couple into the adjacent channel. Once the backer plate waveguide channel is above its cutoff (at roughly 50 GHz), high levels of crosstalk are seen. 50 GHz is below the Nyquist frequency for 224G, so this can be a major concern when trying to measure 224G devices.

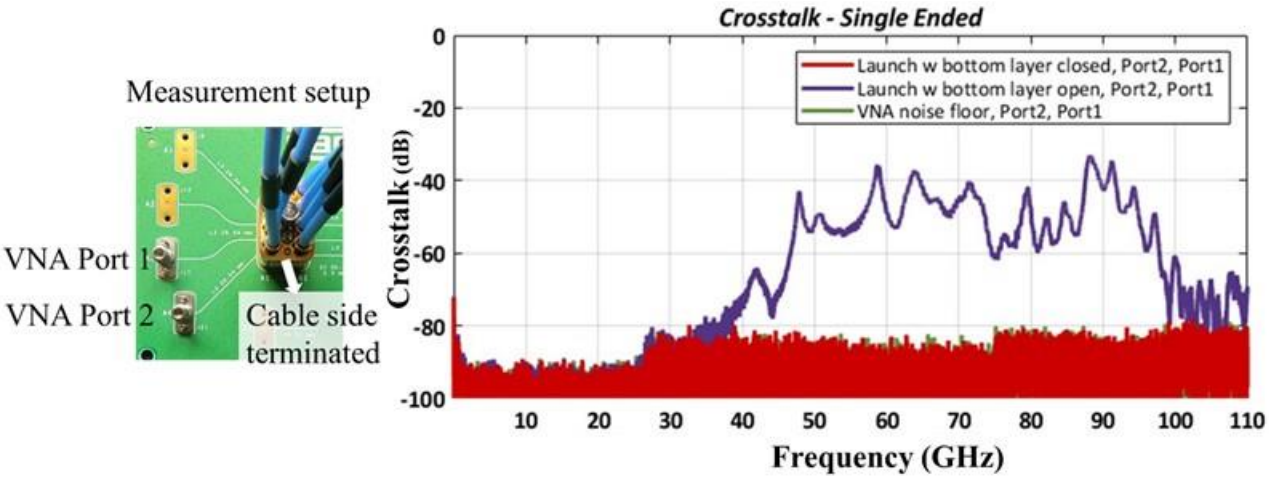

Figure 16: Compression mount connector crosstalk when bottom plane of launch is open (purple) vs. closed (red). The closed launch crosstalk is at the VNA noise floor (green).

Flavor 1(c): Angled Launch Example and Issues

To a large degree the design for angled launches is identical to the standard vertical launches. Figure 17 shows a cross-sectional view of an angled 1.85 mm launch. The main difference is that the angled connectors usually taper toward the signal pad on the PCB. A smaller landing pad allows for a smaller GND ring diameter as well as smaller voids in the return plane layers.

These factors along with the fact that the connector shield also tapers down at the PCB, usually means a lower return loss can typically be obtained. This is design dependent though and so is not a guarantee.

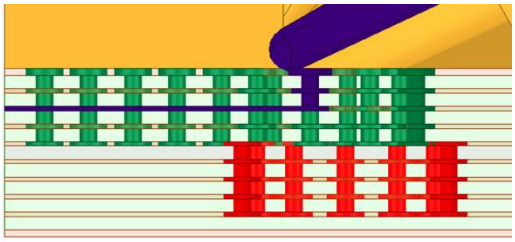

Figure 17: Angled launch connector cross-section

Flavor 2: Edge Launch Example and Issues

Edge launch connectors are familiar to most people and allow the PCB trace to escape in the same plane as the center conductor of the connector. The connector shield has an opening though which the center conductor sticks through and lands on the PCB pad. Signal energy flows through this opening. The opening overlaps several plane cavities in the Z direction, as shown in Figure 18. This means energy can couple into the plane cavities resulting in poor return loss and signal dissipation.

Additionally, if the connector is not perfectly flush to the PCB route border and the PCB planes are not exposed and in contact with the connector, a cavity forms that greatly impacts both thru performance and isolation. The isolation becomes a major issue when edge launch array connectors are used. Figure 19 shows the electric field intensity for an edge connector array in the launch area. Figure 19(a) shows that fields couple strongly between the channels because the edge of the PCB is not metallized. This allows the signal to propagate along the channel between where the vias in the PCB end and the body of the connector.

Most commonly, there is a minimum clearance between the edge of the metal planes and the edge of the PCB. This is on the order of 10 mil. This clearance prevents the planes of the PCB from coming into electrical contact with the body of the connector to create an uncontrolled planar cavity. Figure 19(b) shows the strong fields that exist in this region. Overall, this results in both high crosstalk and poor RL. Figure 20 shows very high crosstalk (>30dB above 30 GHz) for an arrayed edge launch that hasn't been properly tied to the PCB planes.

Edge plating is a mechanism to mitigate this issue. Figure 21 shows how edge plating the PCB helps significantly improve the RL and isolation when using edge connectors. Closing off unwanted signal propagation avenues forces the signal to travel down the intended path tuned for performance.

If using stripline to route to the DUT, the transition to inner layer routing is made difficult due to the space required to make a good transition interfering with the connector to PCB transition fields in the connector area. Effectively, the stripline transition via must be moved far away from the connector launch. Since the connector transition is now decoupled from the via transition, it can allow a better via transition to be designed. However, it does mean that the signal must travel as a microstrip for a certain distance, increasing crosstalk among exposed surface traces if in close enough proximity.

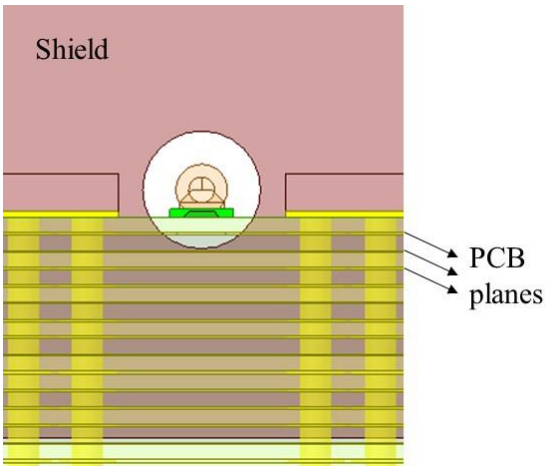

Figure 18: Edge connector mounted on top surface of PCB. The opening in the connector shield, through which signal energy flows onto the PCB, overlaps the first several plane cavities. These cavities provide alternate transmission paths for the signal energy.

In summary, **minimizing the RL for a connector launch involves reducing the X/Y cross-sectional physical size of the launch as much as possible, while keeping all waveguide structures in contact with the launch in cutoff.**

Bringing it All Together

All measurements in this section, that were done to 67 GHz, were performed on a Keysight Technologies N5227B PNA Microwave Network Analyzer. Calibration was done using Keysight's N4694D ECal module.

Measurements to 110 GHz were performed on a Keysight N5227B VNA with 110 GHz extension heads. The VNA was SOLT calibrated using a Keysight 85059B calibration kit.

The goal was to measure the performance of ganged, vertical launch cable assemblies –

DUT 1. Samtec BullsEye BE70A with 6" of 0.086" coax and 1.85 mm connectors at the end of the cable. Rated performance 0 to 70 GHz.
DUT 2. Samtec BullsEye BE90A with 3" of 0.047" coax and 1 mm connectors at the end of the cable. Rated performance 0 to 90 GHz.

Measurements were performed by connecting the VNA to the cable side of the DUT on port 1 and a VLC mounted on the PCB on port 2. There is approximately 25 mm of trace between the VLC on the PCB and the DUT-PCB interface. The VLC on the PCB and PCB trace needed to be de-embedded from the measurements to isolate the performance of the DUT.

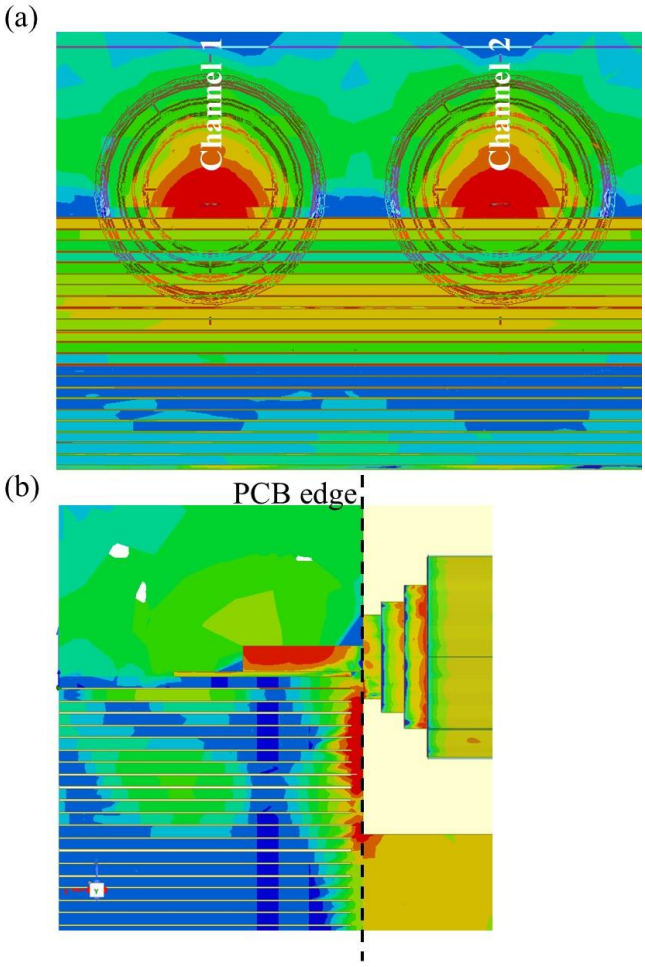

Figure 19: Electric field plots at 30 GHz in 2 orthogonal planes. (a) shows strong field coupling between adjacent channels of an edge mount array connector and (b) shows strong fields at the interface between the connector and PCB edge

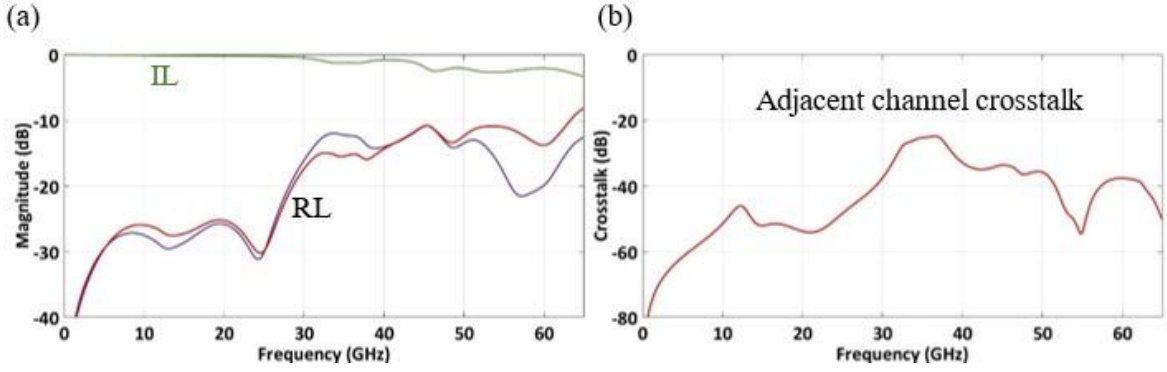

Figure 20: (a) IL, RL of edge launch connector without edge plating. (b) Crosstalk between adjacent channels for the same connector. RL and isolation degrade above 30 GHz without PCB edge plating

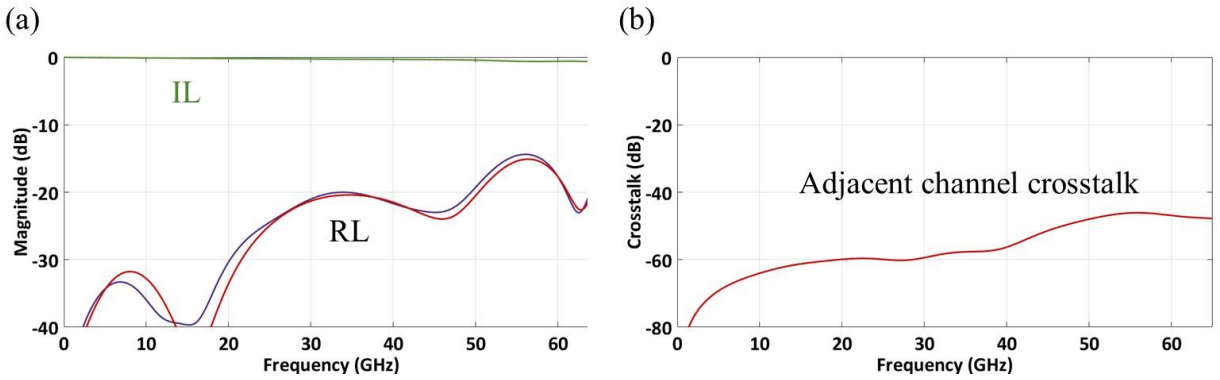

Figure 21: Improved return loss and isolation for arrayed edge launch connector when PCB has edge plating

To do the de-embedding a "2X" structure was measured. This consisted of two 1.85 mm VLCs with 50 mm of trace between them. The 2X structure was instantiated on the same PCB as the DUT, to minimize fabrication variation. The 2X structure is then bifurcated and the equivalent 1x structure is de-embedded from the DUT measurement.

The effectiveness of the concepts outlined in the previous sections is shown in Figure 22. It shows the frequency at which the IL equals the RL for the 3 fixtures discussed previously - XS0040, XS0052 and XS0056. XS0040 us usable only up to about 52 GHz. The higher IL, due to the narrow trace, and the poor RL above this point, due to a relatively large VLC launch, limit the performance to this frequency.

XS0052 is much better and exceeds the bandwidth for its targeted 70 GHz application, with the crossing frequency being approximately 85 GHz. To get this performance though, 1.85 mm VLCs can't be used. Higher performance 1.35 mm or 1 mm VLCs must be used. To understand why this is important, look at Figure 23. XS0052 used with a 1.85 mm connector can quite clearly measure the performance of the DUT well (BE70A in this case), but it becomes hard to tell whether the poorer RL above 52 GHz is caused by the DUT or is a limitation of the fixture. Measurement with 1 mm connectors, allows greater IL-RL separation, showing much lower RL for the DUT itself.

Finally, Figure 24 shows that XS0056 can de-embed well up to 90 GHz. The fixture was used to measure the performance of DUT2. Results are shown in Figure 24. De-embedding works well to 90 GHz and DUT performance correlates very well to simulation, up to that frequency. XS0056 is the fixture that performs to the highest bandwidth because:

1. ELIC allows the use of smaller diameter vias, reducing the cross-sectional size of the launch and preventing excitation of higher order modes up to 90 GHz.
2. ELIC allows the circular waveguide below the launch to be completely sealed and in cutoff, again to 90 GHz.
3. Even though narrow vias required the use of thin dielectrics, stacking the dielectrics allowed wide lines and low attenuation loss.

While the copper in XS0056 is rougher than other constructions, the combination of the wide line and lower RL allowed by points 1, 2 above, results in a test fixture that performs better to a higher frequency.

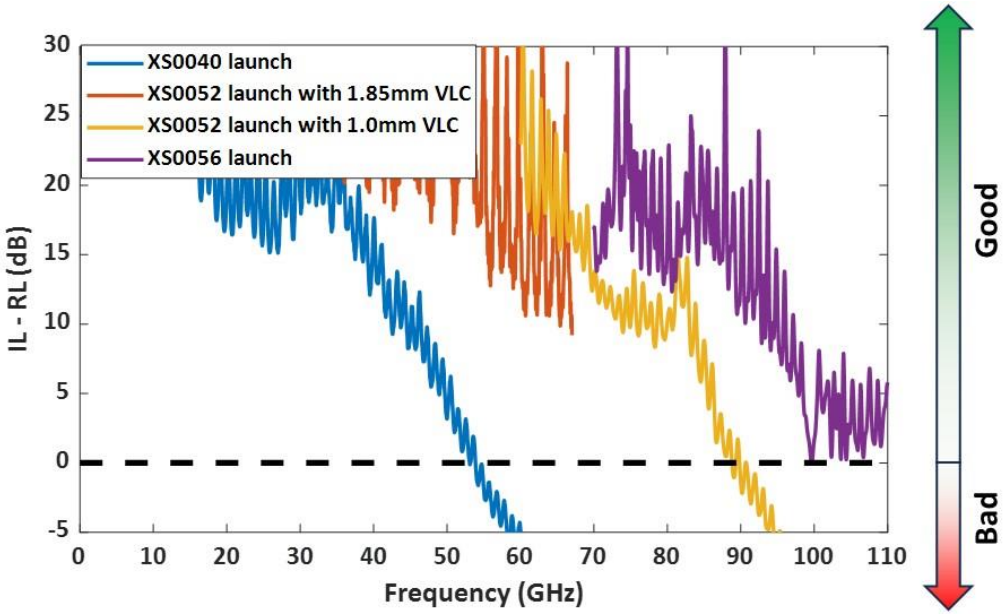

Figure 22: IL-RL for 3 test fixtures indicating the frequency at which the separation goes to 0

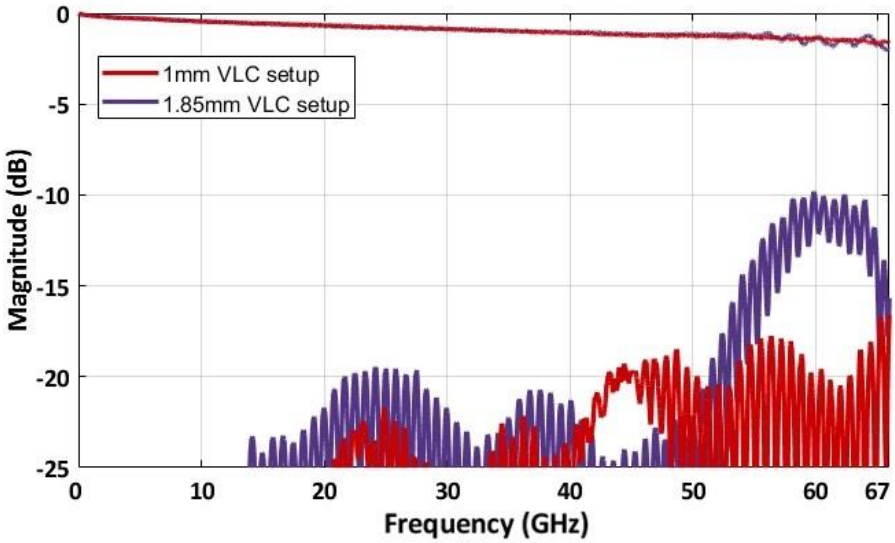

Figure 23: The same DUT measured with 2 different fixtures. Purple curves use a fixture with 1 mm VLCs while red uses 1.85 mm VLCs in the same fixture

There are differences between simulation and measurement above that frequency, but that will need a higher performance test fixture to resolve what is a simulation model inaccuracy vs. a test fixture limitation.

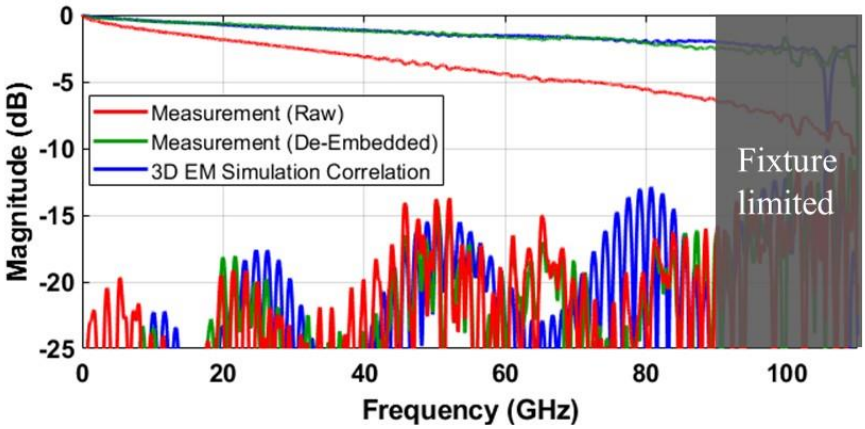

Figure 24: Measurements for DUT2 with XS0056 test fixture and simulation correlation

Conclusion

Figure 25 shows a comparison table to make the process of comparing the different connector types easier.

	Edge	Angled	Vertical	Ganged
Distance to DUT				
Via transition to inner layer RL performance				Depends on flavor
Calibration plane at the connector				
Crosstalk for ganged version				
Cost				

Color key: Poor … Best

Figure 25: Comparison table to allow easier tradeoff analysis between the different connector types

A test fixture is going to depend heavily on the DUT and the equipment available. There is no one size fits all guidance. However, Figure 25, suggests that a good place to start when trying to test several channels on a DUT is ganged vertical/angled launch connectors placed as close to the DUT as possible. This scheme provides:

- Low IL because the distance to the DUT is minimized.
- If the connector can be calibrated at the PCB interface, that will be ideal. Even otherwise, since coax cables have very low loss per unit length, they can provide good IL-RL separation to very high frequencies, which in turn allows de-embedding algorithms to better reflect the performance of the DUT.

- With proper launch design, the impact of the RL of the connector launch can be minimized over the operating bandwidth.

In conclusion, by using the guidelines provided here, a test fixture design that performs well for 224G devices is entirely feasible without needing exotic techniques.

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