DesignCon® 2024
WHERE THE CHIP MEETS THE BOARD

Survey on Correlation & Simulation Methodologies for PCB Structures Through 67GHz

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Abstract

This paper focuses on achieving high accuracy in simulating PCB structures, essential for obtaining realistic representations of fabricated PCBs. Numerous papers in the field of Signal Integrity have explored accurate PCB modeling, covering various factors. However, implementing best practices can be challenging due to the abundance of literature and multiple modeling techniques for the same topic.

The objectives of this paper are twofold. Firstly, it aims to understand the current state of PCB modeling strategies, considering factors impacting performance. These factors include conductor characteristics (etching, surface roughness, and conductivity) and dielectric modeling (soldermask, glass-weave, and lamination), among others. Secondly, the paper utilizes 224G capable test boards to assess the relationship between these factors and modeling accuracy.

The research involves surveying existing literature on PCB performance factors and employing a 3D electromagnetic field solver to analyze various PCB structures. The results will be used to catalog the impact of individual factors on PCB performance and to evaluate the accuracy of PCB modeling through correlation.

Ultimately, the paper aims to provide an accessible guide on best modeling practices and their relative importance. This guide will serve as a valuable reference for design engineers, facilitating the optimization and correlation of nominal PCB structures.

Authors Biography

Robert Branson has been a Signal Integrity Engineer at Samtec for the past 4 years. He received his undergraduate in Electrical Engineering from the University of South Carolina in 2020 and masters in EE in 2022. He has worked in connector/PCB design, development, and correlation for numerous Samtec products, and has experience in using 3D modelling software for the analysis of connectors.

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Scott McMorrow currently serves as a Strategic Technologist for Samtec, Inc. As a consultant for years too numerous to mention, Scott has helped many companies develop high performance products, while training signal integrity engineers. Today he works for "the man," where he continues being a problem solver, a change agent and "betting his job" every day.

Steve Krooswyk is a Sr Signal Integrity Design Engineer at Samtec. His 19 years of experience includes contributions to the design, simulation, and correlation of interconnect and I/O, as well as an influential role in PCIE standards. Prior, Steve was the PCI Express technical lead for Intel Data Center Group, co-authored the book *High Speed Digital Design: Design of High-Speed Interconnects and Signaling*, and received an MS in EE from University of South Carolina.

1. Introduction

Before the building of a PCB, the role of a signal integrity (SI) engineer is to design the SI relevant sections of the PCB in order to ensure that the PCB will achieve the target bandwidth. Generally speaking, these structures are the footprints, layer-to-layer transitions, and the traces. It is vital that this optimization is done correctly as, especially for 112G and beyond, very minor miscalculations in these metrics can have a large impact on the performance. While some of this is controlled/modified by the fabricator, there are significant areas that are entirely dependent on the SI optimization. For instance, areas such as vias, are inherently dependent on the accuracy of the model selected. This paper explores how to build the best possible nominal model such that the optimization performed on SI-relevant regions of the PCB will be effective.

For the purposes of this paper, we are defining a nominal model as the model designed prior to building a PCB which is used to design and optimize its layout. The obvious best-case scenario would be to have a nominal model which is 100% accurate to the measurement that is eventually performed on the finished PCB. However, anyone with any time spent designing or measuring PCBs will know that such a thing is nearly impossible. The variation inherent in the tolerances of manufacturing and fabrication necessitates variation in PCB performance. With perfection therefore out of reach, the goal instead becomes to build the most accurate model possible, within the limitations that variation imposes.

Our paper defines three PCB modelling fundamentals. The first is manufacturing information. This contains all of the concrete and known quantities of the PCB. For instance, the drill size of the vias, the stackup dimensions, or the number of layers. These are all modelling questions which can be answered by looking at relevant datasheets as well as manufacturer/fabricator published and confidential materials.

The second is manufacturing variation. This is the variation that occurs when a PCB is fabricated, shifting values from their nominal point to something within tolerance. For instance, the layer-to-layer misregistration or the via stub length on a back-drilled through-hole via. These tolerances are available from the material vendor and/or PCB fabricator. The fabricated dimensions can only be verified after a board has been fabricated.

The third is what we are categorizing as simulation methodology. This is a broad group which can be largely defined as containing all information pertinent to simulation which is not contained within the two previous groups. It covers the particulars of how the simulation is done to achieve the best correlation. Oftentimes, these decisions will have to be made without the benefit of measured data. These are the topics that we will be focusing on in this paper, and include factors such as surface roughness modelling, etching, and temperature. They are modelling questions through which the best answer can only be derived from experience, research papers, and if available, correlation.

Of the three components of modelling, we are focusing on simulation methodology because it is the most useful to a SI engineer seeking to build the best nominal simulation. Manufacturing information has a correct answer, it just must be sourced from vendors. Manufacturing variation can be understood ahead of time (variation analysis can be done on the nominal model to model what possible change in performance will come from variation), but ultimately the specific variation can only be determined retroactively on a panel-by-panel basis. On the other hand, simulation methodology represents real changes that a SI engineer can make to improve their modelling accuracy in general, such that future boards are more accurate on an all-encompassing basis.

There have been a great many papers that look at individual components of simulation methodology and different methods that can be used to more accurately determine one of them. While each is useful in their

specific context, the broad issue, as pointed out in [25] by Bert Simonvich, is that many of these papers focus on correlating to specific measurements on a specific panel. They can be useful to retroactively understand the performance of a PCB, but it can be difficult to apply that understanding to future designs. Instead, most of the widely-known and referenced papers focus on the big picture, and how to build a model that will be accurate to any stackup and design. For instance, one of the most recent and famous examples of this is Huray's paper [21] which became the basis for the widely used Huray model. As such, our paper will be focusing on these techniques, which can be applied across a wide range of designs.

This paper will begin with an investigation of some of the best works on each of the factors which we have defined as simulation methodology. We will look at how these factors function, how to model them, and some of the papers to best reference for more information. Then, we will use the accumulation of data gathered by these factors to build a dataset comparing relative impact of the different simulation methodologies. This will have the dual use of determining where time is best spent during the design process to get an accurate model, as well as during correlation to understand where the biggest impacts to performance could be coming from. Finally, we will use the data and techniques developed to look at a measured 224G board and analyze how we can improve accuracy of our simulations using superior simulation methodology.

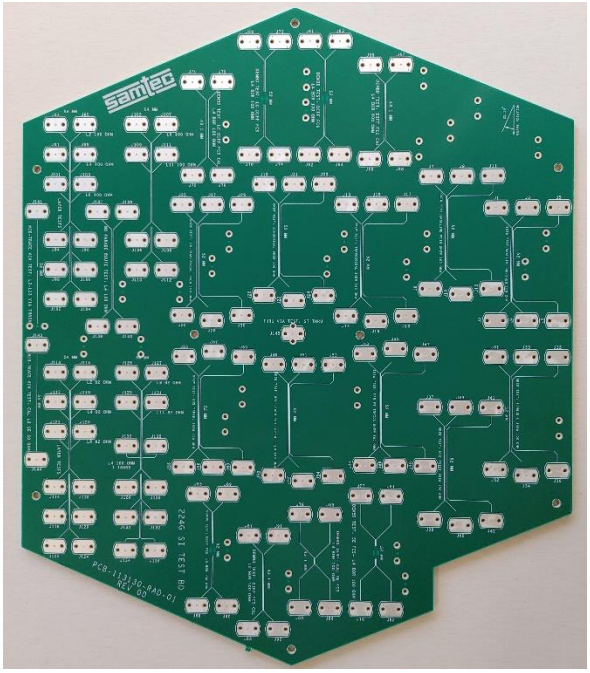

Figure 1: 224G Samtec Test Board to Validate Simulation Accuracy

There are many different structures possible on a PCB, but to somewhat bound this problem for the sake of our investigation, this paper will focus on differential stripline trace routing and differential via designs. These structures should give a representation of what can be seen across other, similar structures. What follows is intended to give an overview of the current state of the literature and a starting point for any SI engineer who wants to improve their simulation modelling accuracy at 67GHz and beyond.

2. Background

In the two sections that follow, the characteristics of simulation methodology are laid out. The sections are separated by material characteristics and environmental characteristics. Environmental characteristics model the environment around the PCB, such as temperature and humidity. While the material characteristics are inherent to the PCB stackup, such as surface roughness, dielectric constant, and loss tangent.

For each of the characteristics, we split the information into four different subsections. First, what the characteristic is and how it impacts PCB performance. Second, how it can be simulated and how we simulated it. Third, what ranges we considered in order to weigh its impact on PCB performance. Finally, we cite sources which were helpful to understand each characteristic.

For the range portion of each characteristic, two ranges are given. A narrow and a broad range. The broad range is meant to represent most, if not all, of the possible design spaces one might see in that particular characteristic on a PCB. This would include most PCBs from around 14Gb/s to 224Gb/s The narrow range is meant to represent the more realistic range of design spaces that one would see across high-speed boards. This would include most PCBs from around 112Gb/s to 224Gb/s.

Additionally, each characteristic's ranges were given an accuracy ranking to illustrate the confidence with the gathered performance data. This ranking was based on how reliable the research is for that particular topic in terms of consistency among sources and number of available resources. If the simulation technique to simulate a particular metric was questionable or the current research was inconclusive a lower ranking was given.

Great efforts were made to ensure that all characteristics in the simulation methodology category were included in this paper. When it comes to stripline, this paper should cover every characteristic due to the relative simplicity of its geometry. For vias, our ability to cover characteristics was somewhat limited by the simulation software we used. Some physical aspects of a via, such as plating and capping, were not included in this paper because they cannot be simulated by our solver. It is questionable if they are of SI relevance, but regardless their absence should be noted. It is also possible that some minor factor that is SI relevant was missed during the course of our research, but this paper will cover every characteristic which has a significant impact on SI performance.

3. Material Characteristics

Surface Roughness

Surface roughness is one of the most complicated and researched factors that impacts PCB performance. For this paper, our group evaluated numerous papers covering the topic [18-26] and there are almost innumerable papers that have covered the subject. Surface roughness describes the imperfections in level occurring on the surface of the copper trace, caused from when the copper was created as a sheet. There are two sides to a traditional copper foil. The matte side is the roughest side and it is bonded to the core laminate. The drum side is smoother, faces the prepreg and is treated with oxide etching during the PCB fabrication process. [24] Note that reverse-treated-foils (RTF) flip this orientation (and fabricators can smoothen/roughen surfaces to achieve what is necessary for a specific stackup), but our paper focused on the more traditional electrolysis approach.

While more complicated methods for modelling surface roughness exist, the basic method involves building a mathematical model of the impact of surface roughness and applying the additional loss which is generated by that model onto the simulation. The concept was popularized with the publication of the Hammerstad or Groiss models [35], however these models roll-off in accuracy at 30+GHz. [26] The new standard for surface roughness modelling is the Huray model. [21] This model holds out to higher frequencies very accurately. The difficulty with this model, however, is relating Rz values from copper foil datasheets to the physical parameters required by the model only obtainable by cross sectioning and SEM.

In order to utilize the Huray model without having to build a PCB and correlate to it, we use the method identified in [24]. This paper holds all Huray model inputs constant expect one, nodule radius, for which it derived a formula to calculate the nodule radius from the Rz value of the copper foil datasheet. For most simulators, the process of simulating surface roughness is to then enable the Huray method and use these derived values to simulate it correctly. We followed this process in our 3D EM field solver.

To determine the ranges for this metric, we combined information from the papers already mentioned [18-26] with the data offered by numerous copper foil manufacturers. To simplify understanding, we related all surface roughness metrics to a standard notation of using Rz. This value is the average of the five highest and lowest points in a region (measured in microns) and is useful for understanding the maximum of the macro surface roughness. First, we looked at the range of copper foils that are currently being made (the matte side). At the roughest end is HTE, and at the smoothest end is either rolled annealed (RA) or HVLP5. From there, our narrow range was defined as being HVLP-HVLP5, and our broad range was defined as HTE-HVLP5. These copper foils associate with Rz values of 3.0-0.8um on the narrow range and 10-0.8um on the broad range. Since surface roughness metrics are well-documented and the methods for modelling them are also well-documented, we rate this range as being high-accuracy.

Surface Roughness Conversion									
Foil Type	HTE	LP	VLP	HVLP	HVLP2	HVLP3	HLVP4	HVLP5	RA
Rz	10um	4um	2.5um	2.0um	1.5um	1.0um	0.8um	0.6um	0.5um
Chart shows approximate roughness values which can vary by vendor									

Table 1: Chart of Surface Roughness Ranges

For more information on surface roughness, a good starting point on understanding the various standard notations is [22]. This paper goes over all the basics of surface roughness and the notations that will be seen on most datasheets. For information on modelling surface roughness, a good source is [24]. This paper goes into detail on how to build a Huray model and get the most accurate simulations possible. Unfortunately, there is little published information on surface roughness in relation to plated vias.

Dielectric Modelling

Proper dielectric modelling is crucial for high-speed correlation in PCBs. This involves the creation of the core and prepreg layers in the stackup. There has been much industry research into dielectric modelling materials and their impact on realized performance [1-4]. As data rates have increased, the attention to the details of dielectric modelling has increased as well.

For our simulations the Djordjevic-Sarkar model was used to simulate the dielectric material properties of both core and prepreg materials [1]. These were simulated as blocks of material substrate stacked on top of one another with the corresponding embedded copper geometry. 3D tools require the user to build this

out as rectangular prisms stacked on one another. Most 2D tools give the user the ability to implement dielectric modelling as a stackup. In our 3D EM field solver we imported our predesigned stackup.

The broad range of dielectric modelling was defined by sweeping both manufacturers specified loss tangent (Df) by 45% and dielectric constant (Dk) by 15%. The narrow range was defined by ranging the properties by a third of the broad range: 15% in Df and 5% in Dk. These values were derived from both existing measured results seen in material extraction and outside research showing variation from manufacturer specified properties [2].

There are many reasons why the effective dielectric properties on a transmission line or via may appear different, which can be explained by the complexity of fiber weave in resin. Anisotropic modelling has been proposed and shown to have better correlation in some cases [3]. However, consistently predicting anisotropic properties can be difficult without adequate characterization. Another method for complex dielectric modelling is simulating the fiber weave within resin [4]. This method of modelling is difficult to realize in correlation without a cross section of a PCB. Both of these modelling methods highlight why the material properties in a PCB would vary from the originally specified value. Changes in copper utilization could also result in fiber becoming closer or farther away from strip-line, increasing, or decreasing the effective dielectric constant seen by the line. The reality of PCB material manufacturing, their anisotropic nature, and location of glass fiber weave with respect to transmission lines show why dielectrics vary in their properties. Based on the above concerns, we rate the defined ranges as medium-accuracy.

For more information on dielectric simulation see [5], which simplifies the dielectric manufacturing process, and complications in simulation. The Djordjevic-Sarkar model is proposed in [1], which is the baseline for much of the high-speed dielectric modelling that exists today.

Solder Mask

Solder mask is the dielectric that covers the TOP and BOTTOM layers of the PCB to protect and isolate outer layer conductors during solder reflow. It is one of the final steps in the PCB fabrication process. High-frequency designs sometimes use keep-outs to prevent solder mask from influencing performance. When present, however, solder mask can be a deceptively complicated subject when it comes to PCB performance. While it is true that solder mask is not relevant to stripline performance, it often does come into play when looking at signal vias in BORs or transitions. As such, understanding its impact can be SI relevant for many designs.

Simulating solder mask is done by adding the dielectric layer, then cutouts to remove the solder mask where it won't be present due to holes in the mask. Similar to any other dielectric layer, the dielectric properties should be taken from the vendor. In our 3D EM field solver, we added a dielectric layer over the TOP layer and applied our soldermask Dk and Df .

The ranges for this metric were difficult to discern, given that there has not been much research into variability in solder mask properties from vendor specifications. Unlike laminate layers, the most prevalent solder mask research does not look at variability in relation to vendor specifications. [27-28] As such, without specific research into this subject, we decided to use the same ranges from the previous laminate section. In theory, this is imperfect due to the lack of glass weave in solder mask. Solder mask will likely vary less than laminate in terms of pure Dk and Df variation. However, solder mask likely varies more than laminate in terms of thickness. As such, we chose to use the same ranges despite some potential concerns. Given these concerns, we rate this range as being low-accuracy.

For more information on solder mask, a good reference is [28]. This paper goes into how solder mask effects microstrip electric field distributions, impedance, and performance. It also provides some basic formulas for evaluating microstrip trace with solder mask. Unfortunately, there is little information regarding solder mask impact on vias outside of the original research provided by this paper.

Conductivity

Conductivity measures the ability of material to conduct electrical current. Higher conductivity means that current will flow more readily in a material. Typically, conductivity is measured with units of Siemens per meter(S/m). In transmission line applications, conductivity is one of the factors needed to quantify the loss of a model. Using more conductive/less resistive materials helps reduce transmission lines losses.

Conductivity can be input into any solver as its typical units (S/m). Alternatively, it could also be input as a materials resistivity with units of ohm-meter. In our 3D EM field solver, we defined the conductivity of the metals (S/m).

At room temperature (20°C), pure copper has a conductivity of $5.96 \times 10^7 (\frac{S}{m})$. In real PCB applications, copper conductivity normally can be defined in the range of about $5.6 - 5.8 \times 10^7 (\frac{S}{m})$. This discrepancy comes from the difficulty of refining pure copper and the introduction of impurities that come from PCB manufacturing [13-14]. In practice, boards have come out with lower conductivity such as in [6] which saw an average of $4.44 \times 10^7 (\frac{S}{m})$. In our study, a narrow range of $5.6 - 5.94 \times 10^7 (\frac{S}{m})$ was used based on common high-frequency measured boards from both our experience and the sources already mentioned. The broad range is $4 - 5.94 \times 10^7 (\frac{S}{m})$, coming from the outliers in measured copper foils. We rate the defined ranges as high-accuracy.

There are no explanative papers for conductor conductivity, but it is a well-understood physical characteristic of conductors and there are numerous online sources and textbooks which cover its functionality.

Via Conductivity

Copper foil conductivity is a well understood electrical characteristic. Meanwhile, via material characteristics have never been fully characterized. This is likely because any one via in a high-speed electrical channel is relatively small. The reflections caused by the via have more impact in a high-speed channel than the conductive loss caused by the via. Although electrodeposited plating of a via can be similar to that of copper foil it should not be assumed to have the same predictable characteristics, i. e. conductivity and potentially surface roughness.

Modelling via conductivity is much like that of any other conductor. The via barrel has its own conductivity, defined in the same manner as the previous conductivity section. In our 3D EM field solver, we defined the via conductivity in (S/m).

Defining the ranges for via conductivity proved to be challenging due to the lack of research on the topic. Using copper conductivity as a basis, an upper bound was set to that of copper. The lower bound was set to a reasonable value advised by an industry expert. The broad range was defined as $0.5 - 5.94 \times 10^7 (\frac{S}{m})$, and the narrow range was defined as $0.5 - 2.5 \times 10^7 (\frac{S}{m})$. The smaller range was decided to represent about a third of the broad range, starting on the low end. The real conductivity of a particular

via could lay somewhere outside of this range, but it is the most accurate information available at this time. Due to lack of research in this topic, we rate this range as having medium-accuracy.

Like the previous sections than are no explanative paper for this topic. Further research will need to be conducted to derive more accurate values for via conductivity.

Etching

Etching is a well-understood factor of PCB fabrication, relating to the process of removing unnecessary copper to create the intended routing and features. Acid etching removes sections of the copper foil after placing a mask over the copper based on the Gerber file generated by a fabricator. This applies to both trace geometry and via pads. In the process of doing so, an imperfect edge is created on all copper. [31] This edge will have a slight angle to it, known as the etch angle, creating a trapezoidal shape for trace geometry.

All copper on the board are influenced by etching, but there are two categories of PCB structures when it comes to etching. The first is controlled impedance. These are generally traces, and they are pre-compensated in the Gerbers by the fabricator to ensure the correct impedance is hit. This doesn't change the actual etching value achieved, only the resultant trace width after etching. The second type of structure is non-impedance-controlled copper. These structures do not have compensation applied to them, and thus will generally become smaller in width after acid etching is applied. This can cause over-etching for influential SI structures such as via pads and antipads.

Simulating etching is fairly simple in most simulators. In 2D simulators, the setting for etching simply needs to be enabled. In 3D simulators, the etch factor will need to be cut out of the rectangular trace geometry. The etch factor is defined by formula 1, and is the general way that etching is defined. In our 3D EM field solver, we defined the etch factor through the relevant toolbox and included it in our simulations.

$$(1)\quad EF = \frac{2*Thickness}{TW_{Bottom} - TW_{Top}}$$

There were some papers that looked at the impact of etching [31-33], but there was a lack of research looking at the etch factor that is measured across a variety of fabricators and stackups. As such, we reached out to fabricators to get estimates on what amounts of etching should be expected. The nominal etching is dependent on copper ounce, but for example 0.5oz copper came out to 0.5mils subtracted on either side for the top side of stripline. The narrow range sees a 10% variation on this etch-back and the broad range sees a 20% variation. Given the information was received directly from fabricators, we view this range as having a high-accuracy.

For more information on etching, the most concise and understandable paper we found was [31] which looks at the impact of etching on crosstalk and impedance. On top of this, etching is a fairly well-documented and understood characteristic of PCB fabrication, so there is a number of freely available online resources available explaining and exploring it.

Copper Utilization

Copper utilization is another well-understood component of PCB simulation, relating to the adjustments that need to be made to the prepreg dielectric height based on the percentage of copper on the signal layer. Prepreg fills in the gaps in the etched signal layer, such that there is prepreg surrounding the stripline

routing. It is a purely volumetric equation (2), which considers copper foil thickness and the percentage of copper utilization to calculate final prepreg thickness.

$$(2)\quad Thickness = Nominal\ Thickness - Foil\ Thickness * (1 - \frac{Copper\ Utilization\ \%}{100})$$

To implement this equation in a field solver, the effective laminate height for the prepreg layer must be calculated. This can either be done beforehand using formula CopUt1, or the formula can be inputted as a function within the solver. Some solvers can even take copper utilization as a percentage. For our 3D EM field solver, we implemented a formula that calculated prepreg thickness from our copper ounces and copper utilization.

Due to how simple and well understood copper utilization is, there is little to be looked at in terms of a research papers. Instead, we spoke with several leading experts in signal integrity to determine the common ranges for copper utilization across PCBs. This was done based on the assumption that the ground reference layer on the other side of the prepreg will have 100% copper utilization. As such, the narrow range was determined to be 10-40% utilization and the broad range was 0-100% utilization. The broad range contains cases that are extremely unlikely to occur, but localized regions of higher or lower copper utilization can occur in PCBs which could mimic the impact of a different copper utilization than was intended to be implemented across the entire board. Since this metric is purely a volumetric equation, its rated as high-accuracy.

There are no sources listed here for copper utilization, but the explanation provided should be enough to understand how it functions.

4. Environmental Characteristics

Copper Temperature

Temperature has a well-documented effect on the loss characteristics of high-speed transmission lines in PCBs. Numerous papers have investigated this effect [7-8]. At higher temperatures, losses increase. There are two sources of this excess loss. Conductor temperature dependent losses and dielectric temperature dependent losses. This section will focus on the conductor side while the next will discuss dielectric.

At higher temperatures thermal vibration of copper atoms disrupt the electrical flow of current. This results in the effective increase of resistance of copper traces at higher temperatures. As such, high speed interconnects will have different loss characteristics at different temperatures due to differences in resistance. As applications of high-speed interconnects spans more environments outside of climate-controlled datacenters, and increased power usage used to drive chips produces more heat, it is important to understand how conductive traces changes with temperature.

Some high-speed solvers will have temperature dependencies built into the material properties of any given conductor. For others temperature dependency has to be built into a material directly. For this study, copper conductivity was defined in CopTemp1 to account for temperature, where T represents temperature, 20℃ is room temperature and $5.8 \times 10^7 (\frac{S}{m})$ was used as the nominal copper conductivity. The coefficient of copper dependence in the equation was defined as .00386 [9]. This coefficient is quite common and known to reliably predict temperature dependent loss from copper. For our 3D EM field solver, we simply implemented this equation in our material conductivity

(3) $Conductivity = 5.8 \times 10^7 * (1 - (.00386 * (T - 20)))$

Defining a reliable range in temperature for a high-speed PCB is difficult, because of the numerous environments, applications, and heat producing components on a board. Originally it was proposed to follow ASHRAE Class A2 temperature range $10℃ - 35℃$ for our study, but it was suggested this was too narrow of a range when considering temperature. Inside the system, highspeed chips dissipate heat on a scale much higher than this range, and as mentioned previously high-speed boards are not limited to only external environments similar to data centers. With this in mind our narrow range was selected to be $15℃ - 70℃$, increasing the bounds on the ASHRAE Class A2 standard, and the broad range was selected to be $0℃ - 105℃$. It should be noted that real applications will experience a gradient temperature change relative to ASIC position and effective impact is somewhere in between. This metric is rated as high-accuracy.

Good sources to reference showing transmission line losses with respect to change in temperature are shown here [7-8]. Each of these papers show transmission lines have increased loss at higher temperature.

Dielectric Temperature

As mentioned in the previous section, dielectric temperature dependent loss is another component of loss when varying temperature. This metric was considered separately from conductor temperature dependence. It is both less predictable than copper conductivity change and effects loss through both Dk and Df variation of PCB laminate materials [10].

Modeling changes in dielectric properties due to temperature of materials is not as straightforward as modelling that of temperature. Most papers note a change in Dk and Df as a percent. This is implemented by changing the input dielectric material properties and then solving the Djordjevic-Sarkar model with the new material properties. Some modelers give the user the ability to set temperature dependencies of laminate properties making it easier to keep change temperature. Much like copper variation with temperature, a variable has to be created to separately track temperature. In our 3D EM field solver, we built a modifier into our Dk and Df for our dielectric materials.

The temperature ranges used in this section were identical to that in the previous section. This allowed a direct comparison of copper and dielectric temperature dependencies.

A few different papers were relied upon to determine a percent variation per degree Celius change in temperature for Df and Dk [6-8]. Each paper observed differences in dielectric properties with a change in temperature. The papers saw a much greater change in Df than Dk over the same temperature range. After surveying the results of other papers, a dependence on temperature of 0.192% per degree C was made to Df, and 0.033% per degree C was made to Dk. Each of these dependencies was applied to both prepreg and core properties separately. It should be noted that lower loss PCB materials tend to have less variation in dielectric properties than higher loss materials [7]. The materials presented in the papers used to compute the percent per degree did not test the ultra-low loss materials available today. Thus, the percent per degree values used may be on the higher side than would be realized on newer materials. Futures studies could help to either validate or invalidate values for more laminate materials. Due the potential inaccuracies of this approach, this metric is rated as medium-accuracy.

Good resources which document and characterize dielectric temperature dependence are here [6-7]. Futures studies would be needed to characterize modern ultra-low loss materials.

Humidity

Much like temperature, humidity is an important environmental factor that affects high speed PCB performance. Higher humidity indicates more water vapor in the air and cause more water to be absorbed by PCB. Because water's dielectric properties are very different from that of typical high-speed laminates increased loss could be observed in high humidity environments [8] [11].

Modeling humidity and its effect on high-speed boards is not a well-defined process. There are no known simulation tools that the authors could identify that have the functionality to consider humidity. In order to account for losses due to humidity, an addition to loss tangent was made to correlate to insertion loss increase measured in other papers. No modifications were made to the dielectric constant of materials because only loss per inch was recorded in the paper used. Any change in loss caused by a difference in the dielectric constant should be captured by the data. In our 3D EM field solver, humidity was modelled as an additive on our Df on our dielectrics.

The ranges used to evaluate humidity's effect on performance was not as straightforward as that of temperature. Research is needed to evaluate the humidity at various levels to adequately extract a per percent or g/kg increase in humidity. Instead, research has leaned more towards evaluating different materials at high and lower humidity environments [8] [12]. Lower loss materials have less variance in loss than higher loss materials. For the narrow range, the Df modifier was made to reflect variance in loss due to humidity [8]. For the broad range, the higher loss material variance was used. Much like temperature the materials used for our ranges do not reflect the top-of-the-line ultra-low loss materials currently on the market today.

It should be noted-that for our study a change in humidity is shown to have an effect on loss, but others have seen a smaller if any effect in performance in a more humid environment. In [12], there was virtually no change in insertion loss of high-speed traces due to humidity. Package humidity dependency was measured in [7], which did see increase in loss with variation in both Dk and Df of the package material, with more variation in the dielectric constant. This variation could be what causes the difference in loss seen in [8]. It is difficult to draw any definitive conclusions of the effect of humidity on high-speed interconnects from the current research. The difficulty of studying humidity is twofold. First it is highly dependent on temperature. Higher temperature means air can hold more moisture. Holding temperature constant while also increasing or decreasing humidity is difficult without a well-controlled environment. Second, PCBs take a long time to absorb moisture. It takes weeks if not months for a board to absorb water into the inner layers. Designing a proper experiment to measure humidity's effect on PCB will take time and a well controlled climate chamber. For these reasons, the metric is rated as low accuracy.

A good source of information on this topic is [7]. This paper explains how humidity measurements are performed and the interrelation of humidity and temperature. However, no paper that conclusively evaluates this topic exists at this time. Further studies which perform material extraction would help build a better working knowledge of the effect of humidity.

Lifespan

Lifespan is an often-ignored component of environmental impacts on PCB, relating to the degradation that occurs in a PCB over time. This is identified as a shifting of dielectric properties within the laminate over time. That shift comes about from a combination of melting/shifting/settling within the laminate. [29] Additionally, there is a general loss of adhesion over time which can cause layers to separate leaving air to fill in the gaps.

Simulating lifespan is like that of laminate temperature. It can be applied as a multiplier on the Dk and Df of the dielectric layers. The greater challenge is determining what that multiplier should be rather than how to apply it. In our 3D EM field solver, we modified the material properties of each dielectric layer by the calculated ranges.

To calculate the ranges for lifespan, we surveyed papers on heat cycling PCBs. [29-30] These papers used a gradual increase and decrease in heat repeated numerous times over the course of weeks to simulate years of PCB usage in a datacenter. While this is the most practical method of analyzing lifespan, it is unfortunately a simplification and not fully accurate to 5 years of actual use in a datacenter. Additionally, the research is generally on older materials, and is potentially less accurate to modern ultra-low loss materials. Regardless, the research showed around 30% increase in Df and 5% increase in Dk for lower loss materials, so that was treated as the narrow range. The broad range is the largest change which was seen in dielectric properties, which came out to 200% increase in Df and 10% in Dk. This is likely overly pessimistic of what would be observed in the vast majority of systems, but is included in our broad range due to it being a measured result. However, concerns about the viability of this data led to it being rated as medium-accuracy.

Lifespan is one of the easier to understand factors, but for more information a great source is [29]. This paper succinctly goes into the background, how tests are conducted, and the resulting data.

5. Data Methodology

The first part of this paper focused on the background research necessary to understand the characteristics of PCB simulation. From here, the paper will utilize that research to analyze and compare those characteristics. This will be done in the two sections that follow.

The first section, called data/discussion, will use a design of experiments (DOE) to analyze the different characteristics across a variety of stackups and board types. The section will build an understanding of the relative impact of the characteristics, as defined by the broad and narrow ranges previously identified. All of this analysis was done in a 3D EM field solver.

To properly compare the different characteristics, it is necessary to use a wide variety of stackups. The reason for this is that different characteristics vary in importance as factors of a stackup change. For instance, surface roughness will have a greater performance impact on PCBs with thinner dielectric than ones with thicker dielectric. As such, we used a DOE to build 50 unique stackups so that our analysis could be performed across a variety of different board designs. The stackups were varied across what is common within high-speed SI PCB design. It is of course impossible to contain every possible PCB design, but this data is meant to represent the common range of PCB designs as currently exists within the market. This process was done twice, once for the stripline dataset, and another time for the via dataset. Pictures of these two simulation models are below in Figure 2.

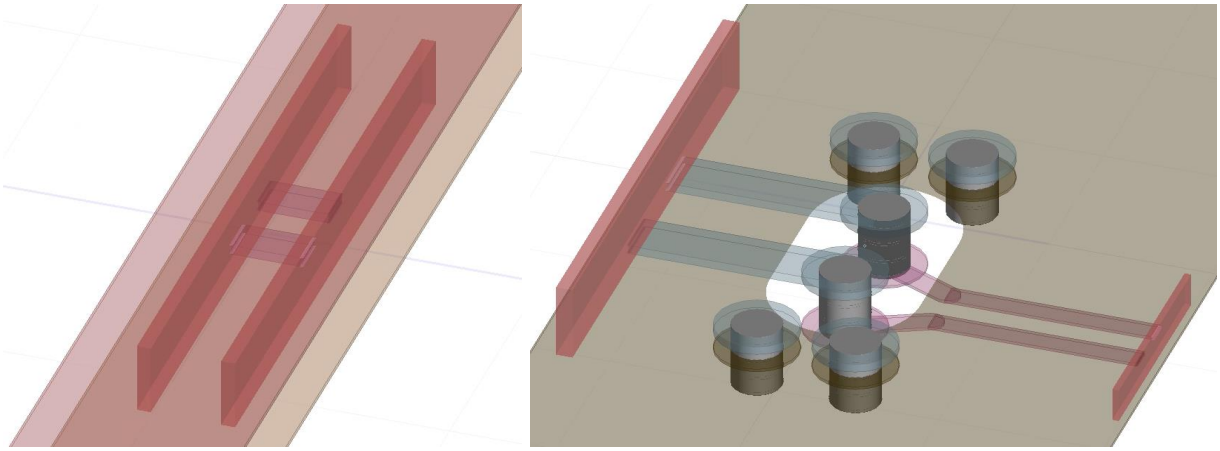

Figure 2: Stripline DOE Baseline Model (left) and Via DOE Baseline Model (right)

These PCBs were varied by multiple factors, which were determined to have most significant impacts on PCB performance contained within the bucket of manufacturer information. (As defined in the introduction of this paper) These factors were Dk, Df, dielectric thickness, copper thickness, and differential pitch for the stripline. For the via, it was those factors as well as differential via spacing, drill diameter, antipad size, soldermask thickness, soldermask Dk, soldermask Df, and plating thickness. With these factors defined in our simulations, we were able to design a DOE of 50 unique simulation designs which varied those factors to create a range for our dataset.

From there, we built a parametric sweep within each simulation which varied the characteristics from our background section by the narrow and broad ranges. Our simulation was designed to look at performance data out to 100GHz. (Though the DOE dependent stackup meant that not all designs performed out to that high of a frequency) The data that is shown in the next section shows the percentage difference from nominal for the narrow and broad ranges. This is shown both as an average and as a box plot to show the variation. This data is intended to show the relative impact of the different characteristics in a wide variety of stackups, such that relative importance can be determined. This will be discussed more along with the data itself and in the conclusion of this paper.

The second section, called simulation/measurements, will use some of the learning from this paper to show the importance of building a good nominal model. It should be clear by this point in the paper that simulation characteristics can vary greatly from board to board and that modelling them correctly is important to achieve an accurate simulation of a PCB, but this section will prove that conclusion out. It will show measurements from a 224G PCB designed for this project and provide simulated data to correlate with the PCB. Once again, this will be discussed in greater detail within that section.

The purpose of the following data is to help the reader as they go forward to apply what they have learned in the background section of this paper. We will show the reader where they should focus their efforts to get the most effect and prove that the methodology being presented is broadly effective. In the conclusion, we will discuss how best to utilize this data for the reader's own projects.

6. Data/Discussion

The first part of the data from the DOE that will be presented is the stripline data. This data was made using the differential stripline model from Figure 2 and contains the results of parametric analyses on 50 unique stackups. In order to analyze this data, a metric was necessary to compare performance. The metric chosen for this dataset was loss per inch. Since it is trace data, this is generally considered the best overall metric for evaluating trace performance. The reader should note that the relative importance of the variables would not be the same if a different metric was used, and that other metrics can still be viable avenues through which to analyze the data. Nevertheless, loss per inch was considered the best all-around metric for this dataset. The data will specifically be showing percent difference between nominal loss per inch and the varied loss per inch according to the characteristic and the range. These characteristics are split into material characteristics and environmental characteristics.

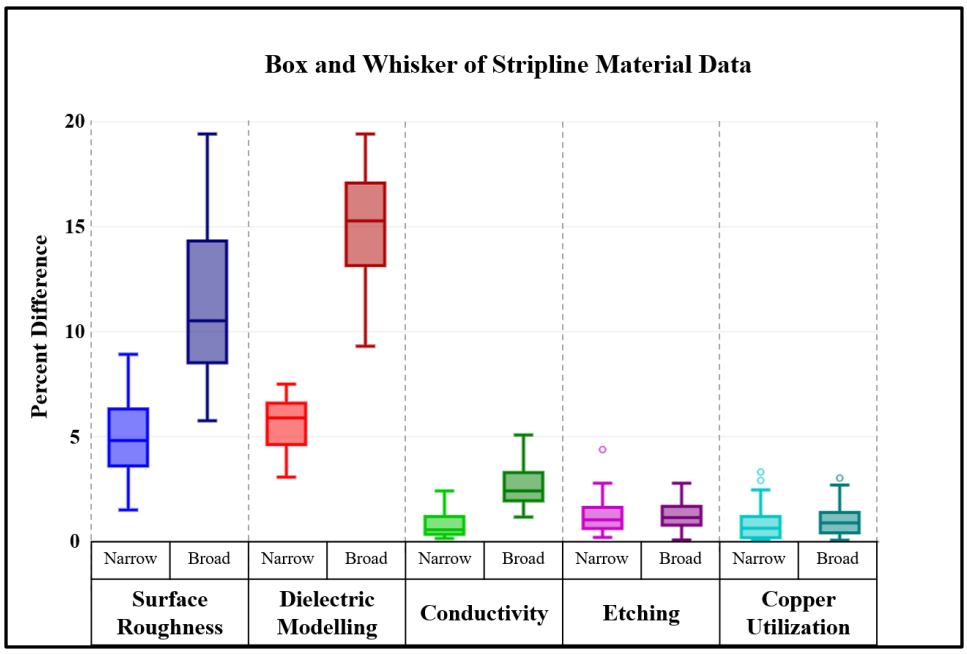

Figure 3: Box Plot Showing Percent Difference of Material Characteristics in Stripline

Box plots were chosen to represent the full effect of each characteristic summarized in the background section of the paper. Figure 3 shows the material characteristic data in this format.

Stripline Material Data(Percent Difference Summary)			
Characteristic	**Average Narrow Range**	**Average Broad Range**	**Confidence**
Surface Roughness	5.11%	11.41%	High
Dielectric Modelling	5.68%	15.19%	Medium
Conductivity	0.88%	2.68%	High
Etching	1.18%	1.22%	High
Copper Utilization	0.85%	1.01%	High

Table 2: Summary of Stripline Material Characteristic Data

Table 2 specifically calls out the averages in the box plot for both the narrow and the broad range while also highlighting the confidence level of the ranges as they were stated in the background. Of the two

ranges provided, the most useful for analysis is the narrow range. It represents what is most common in high-speed stackups. The broad range is more intended as a point of comparison, to show the totality of what impact is possible. This can be good to understand, but it generally outside the scope of most PCB designs. This will carry forward through all of the data in this section.

For stripline material data, surface roughness and dielectric modelling both show the highest percent difference. These characteristics are well-known to play a large role in performance and also had some of the largest ranges in our background. The variation our parametric sweep applied in Rz for surface roughness was over 300%, whereas the variation in something like conductivity for the was 30%. This is the nature of the two variables, as there are more differences to be seen in surface roughness and dielectric modelling as compared to the other characteristics.

Of the other three, performance was very similar between them. This indicates that the relative importance of our final three characteristics is roughly the same. Additionally, the broad and narrow ranges were very similar for them, showing that the total design space for these characteristics is once again smaller than that of surface roughness and dielectric modelling.

The confidence levels shown in the chart are the same as identified in our background section and are meant to show how reliable the data is that was used to generate the ranges. In this data, the dielectric modelling is the only characteristic with medium confidence, because determining the exact variation from datasheets in dielectric materials is very difficult.

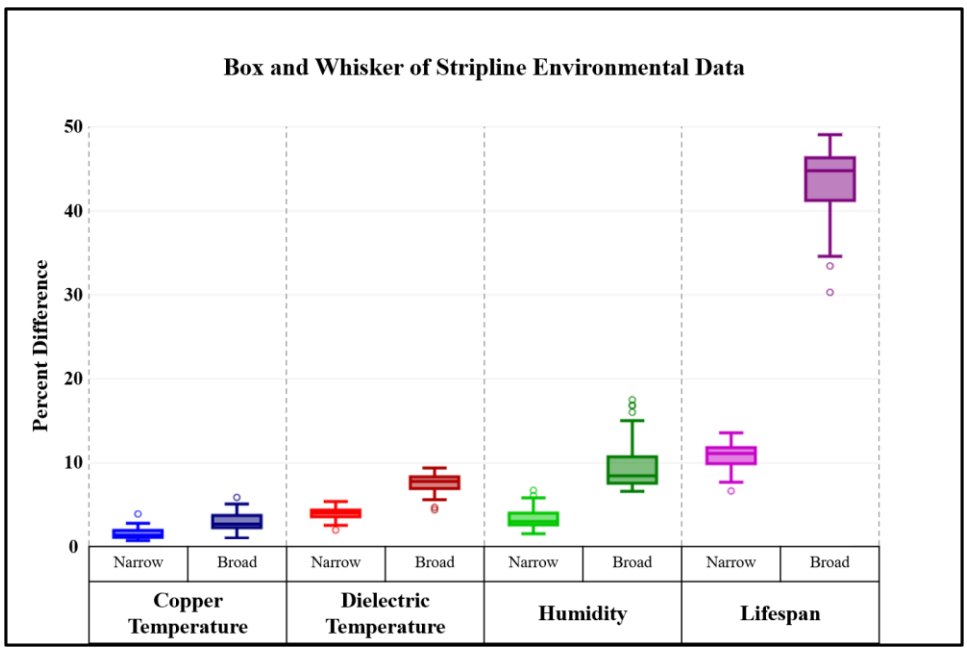

Figure 4: Box Plot Showing Percent Difference Data of Environmental Characteristics in Stripline

Stripline Enviromental Data(Percent Difference Summary)			
Characteristic	**Average Narrow Range**	**Average Broad Range**	**Confidence**
Copper Temperature	1.60%	3.03%	High
Dielectric Temperature	3.94%	7.59%	Medium
Humidity	3.39%	9.78%	Low
Lifespan	10.72%	43.32%	Medium

Table 3: Summary of Stripline Environmental Characteristic Data

For stripline environmental data, there are three distinct categories. By far the largest impact was seen from lifespan. This is due to the massive ranges that were identified in the data. Were the ranges to be true, it would mean that lifespan is overwhelmingly impactful on PCB performance. However, most who have used PCBs over many years will not see this level of impact, meaning that the data or methodology used to collect that data for lifespan likely needs to be called into question. The actual variation is almost certainly a great deal lower.

The second category is dielectric temperature and humidity, which both have similar levels of impact. These numbers are much more within the range of what might be expected, and make sense given the data used to generate them. Of the lowest importance is the third category of copper temperature. It plays the least role from an environmental perspective. It is of note in the data that dielectric temperature is more influential than copper temperature, as it is the more difficult to correlate of the two. This indicates the importance of considering both in systems where temperature will play a role. Humidity is also clearly showing its impact on performance. A large amount of water entering the PCB will have a large impact. (Though this is an increasingly difficult thing to occur as PCB materials improve)

It needs to be noted with this data that the confidence level is much lower on average. There are few papers that look into environmental factors of PCB performance, and it reflects in the confidence levels. The actual ranges for everything except copper temperature (which is well understood and has good data supporting it) could vary greatly from what is actually shown here. We are using the best data available to us at the time of writing this paper, which limits how accurate the results can be.

The second part of the data from the DOE that will be presented is the via data. This data was made using the differential via model from Figure 2 and contains the results of parametric analysis on 50 unique stackups. Once again, in order to analyze this data a metric was needed to compare performance. While loss per inch was appropriate for stripline, a via is a much more complicated geometry. It is much shorter than an inch of cable, and thus will have much less overall loss. Additionally, the metric used to evaluate via performance is generally not that of insertion loss, but instead return loss. A via is designed to minimize reflections so that it has the least impact on channel performance. However, given that return loss varies so greatly with frequency, it was decided to use integrated insertion loss as a metric. This has the advantage of containing the return loss impact and insertion loss impact across broadband frequencies. The method of integration was done using [34] as a guide, with a power weighting filter applied using our given baud rate. Once again, the data will use percent difference between nominal and the varied characteristics, split into material and environmental categories.

One specific note that should be made when it comes to vias is that they vary far more than the differential trace from the first section. While it was fair to vary the stackup and pitch for differential trace and assume that our data contained the majority of designs, that cannot be said for any individual differential stripline model. The specific model that was used is shown in Figure 2 and it has to be

emphasized that a different via design could have different relative levels from what is shown in this data. Unfortunately, in the interest of time and brevity, it was only possible to use one differential via design. Despite this, it is our belief that, given the generic nature of our differential via design, these relative levels should hold true for the vast majority of via designs.

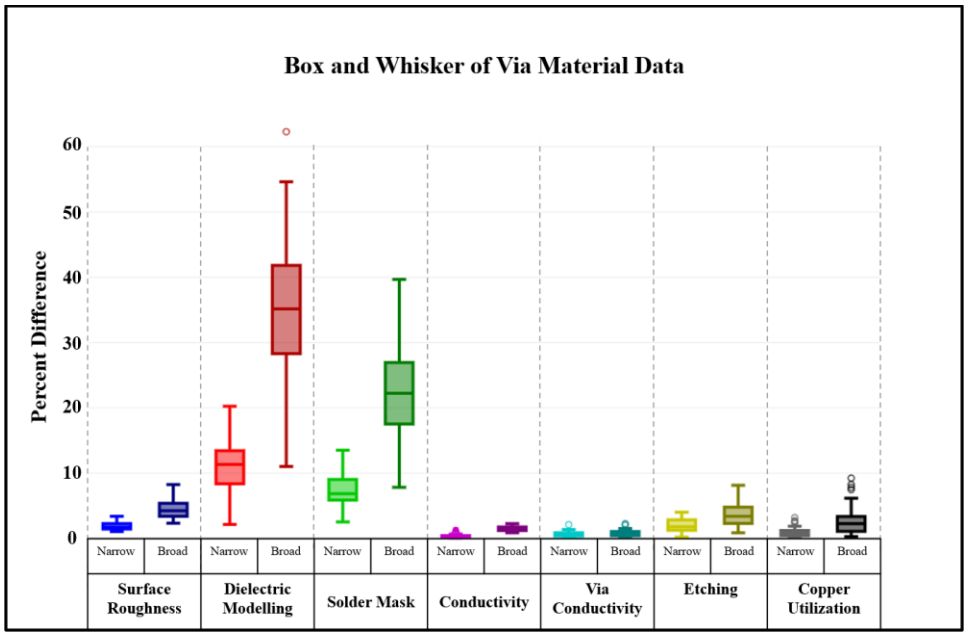

Figure 5: Box Plot Showing Percent Difference Data of Material Characteristics in Vias

Via Material Data(Percent Difference Summary)			
Characteristic	**Average Narrow Range**	**Average Broad Range**	**Confidence**
Surface Roughness	1.82%	4.41%	High
Dielectric Modelling	11.38%	35.60%	Medium
Soldermask	7.45%	22.80%	Low
Conductivity	0.37%	1.49%	High
Via Conductivity	0.65%	0.79%	Medium
Etching	2.01%	3.66%	High
Copper Utilization	0.98%	2.81%	High

Table 4: Summary of Via Material Characteristic Data

When considering a via, dielectric modelling increases in importance. That is because of its impact on impedance and thus return loss, which is included in our integrated insertion loss metric. Solder mask is the next highest, for very similar reasons. This via has soldermask over both the microstrip and the via hole itself, which explains its impact. Any well-tuned via will change its performance greatly when the dielectric properties change, thus emphasizing the importance of getting those properties right when modelling such structures.

Of the other characteristics, there is generally a very similar performance through them all. One additional difference to note between vias and stripline is that surface roughness becomes less important. This could be explained by the via being less sensitive to surface roughness due to its antipads. However, it should also be considered that our 3D EM field solver did not have the capability to model surface roughness on

the face of the via, only on trace. This likely means that our ranges are underestimating surface roughness impact.

In general, metrics which impacted impedance showed greater importance for vias, while metrics which impacted loss per inch showed lesser importance. This is due to the importance of reflections when it comes to vias performance and the de-emphasized impact of loss. It is seen in metrics like conductivity getting a lower percent difference, while metrics like etching increased in percent difference.

The two added characteristics for vias, being via conductivity and soldermask, were of the lower confidence. Again, this is due to a lack of papers looking at this topic, and so these ranges must again be called into question.

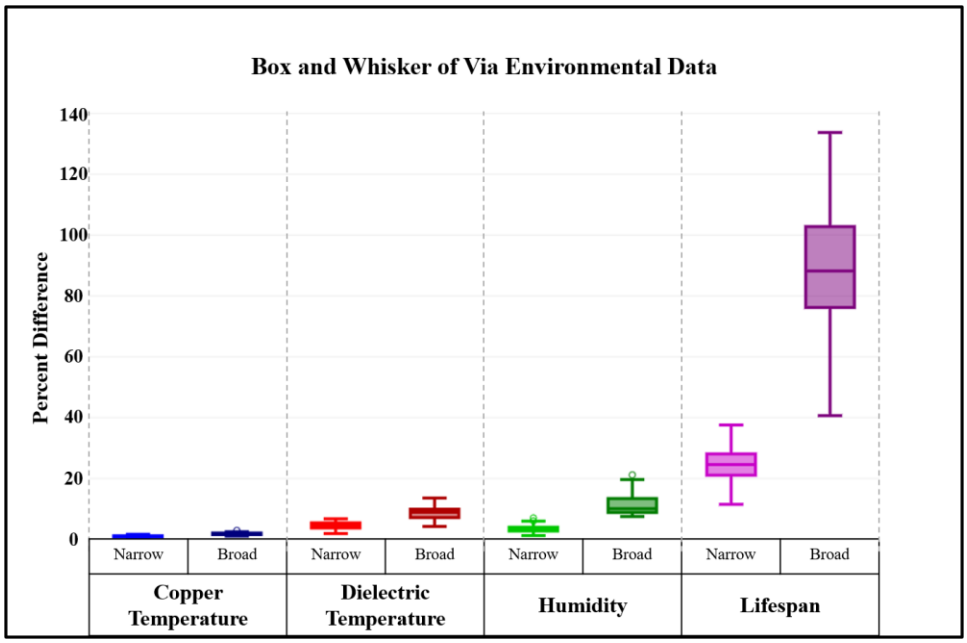

Figure 6: Box Plot of Percent Difference Data of Environmental Characteristics in Vias

Via Enviromental Data			
Characteristic	**Average Narrow Range**	**Average Broad Range**	**Confidence**
Copper Temperature	0.93%	1.79%	High
Dielectric Temperature	4.50%	8.53%	Medium
Humidity	3.47%	11.24%	Low
Lifespan	24.42%	89.07%	Medium

Table 5: Summary of Via Environmental Characteristic Data

Figure 6 and Table 5 show the via environmental data. The lifespan assumptions still have the highest percent difference of all other characteristics. Dielectric temperature and humidity also saw an increased percent difference from the stripline simulations. The percent difference caused by change in temperature on copper remained small.

Aside from Copper Temperature Dependence, all the other environmental characteristics were simulated by changing the dielectric properties of the via structure. It is clear that changing the dielectric properties has the largest impact on via performance.

In totality, the data from the stripline and via material characteristics simulations point to a few key takeaways. Surface roughness plays an important role in determining stripline losses. Improper surface roughness modelling could result in poor prediction of losses. Vias have a smaller dependence on surface roughness, though this could be coming from our modeler being incapable of simulating roughness on the via walls. Proper dielectric modelling is important in both structures. Much like dielectric modelling soldermask is important for modelling vias. This reflects its state in our model as an additional dielectric layer placed overtop of the TOP layer trace and pads.

The observed percent difference data due to environmental characteristics deserve consideration. The effects of temperature on both copper and dielectric properties combined constitute attention to this factor in system environments. The data shows a high dependence on humidity and an even higher dependance on lifespan. In the case of humidity, the data is conflicting and inaccurate, so our low confidence represents a low level of trust in the results. In the case of lifespan, the data agrees more, but the method of collecting data is likely overestimating the impact. Together, these two metrics likely need further research to reach a more conclusive comparison to the relatively well-understood metric of temperature.

With all of the data in mind it should also be noted the interconnectedness of some of the characteristics above, which makes research into their effect on PCB performance so difficult. As mentioned previously, temperature and humidity are highly related. Differences seen in measurement caused by one could be a result of the other. It is for this reason that separate humidity measurement data is so difficult to take. The same goes for other characteristics such as conductivity and surface roughness. Because both are directly related to the conductor and one can never be reliably held at a constant value, decoupling them from one another is nearly impossible within a low degree of tolerance. Surface roughness and certain dielectric properties have also been shown to be related in such a way as well as other characteristics, such as copper utilization and Dk. This paper uses the best data as is currently available to separate out the metrics, but keep in mind that the ranges could be larger or smaller due to the influence of other characteristics.

7. Simulation/Measurements

This section validates the research performed on simulation characteristics using measurement. For the purpose of this section, a 224G capable test board was designed using EM892K, HVLP3, and best design practices to achieve a 67GHz deembedding bandwidth. From there, a variety of different structures were built on the board to test numerous 224G related issues. A few of these structures are shown in the plots below.

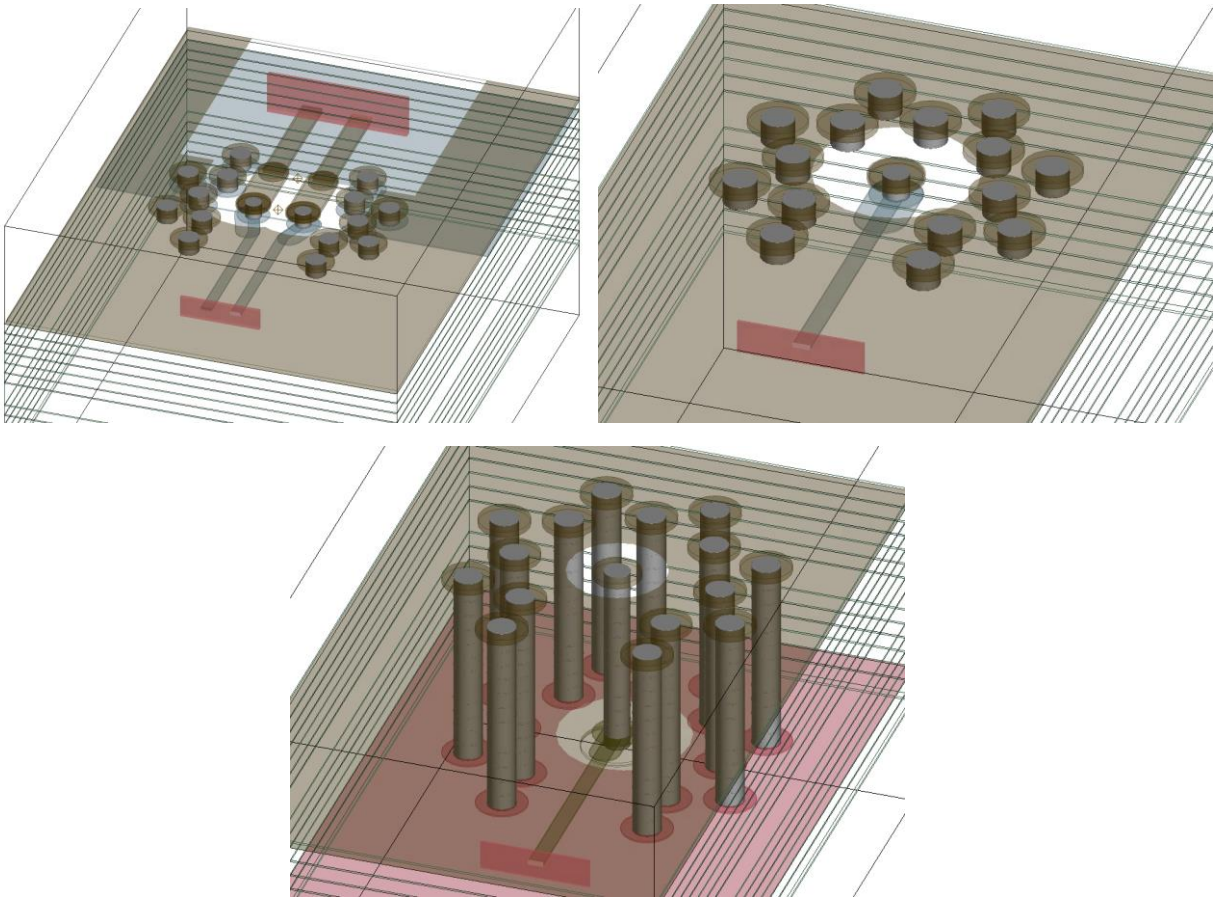

Figure 7: 224G Samtec Test Board Simulations: L2 BOR (top left), L2 SMA (top right), L11 SMA (bottom)

This data is intended to show that best practices for simulation will result in a significant improvement to correlation with the measured PCB, before a full correlation effort is undertaken. The measurements shown are full channels within the PCB, containing vias, traces, and even mock BORs. Given their complicated geometry and the impact of manufacturing variation (such as in backdrill depth variation), a CT scan or cross-section would be necessary to achieve perfect correlation. However, the purpose of this paper is to show simulation methodologies, not to show how to correlate to PCB measurements. In the interest of that goal, the data below therefore shows only the difference between low-effort simulation accuracy and best-practice simulation accuracy, as evidenced in the background.

There is not enough space in this paper to go over all the changes that distinction entails, but it should be largely apparent to a reader who has gone through the background section. We used the simplest methods of modelling in the low-effort simulation (such an older model for surface roughness or the perfect copper conductivity) and the best methods of modelling for the best-practices simulation (such as the Huray model for surface roughness and a tuned conductivity value). This data shows what was gained from making these changes to the model.

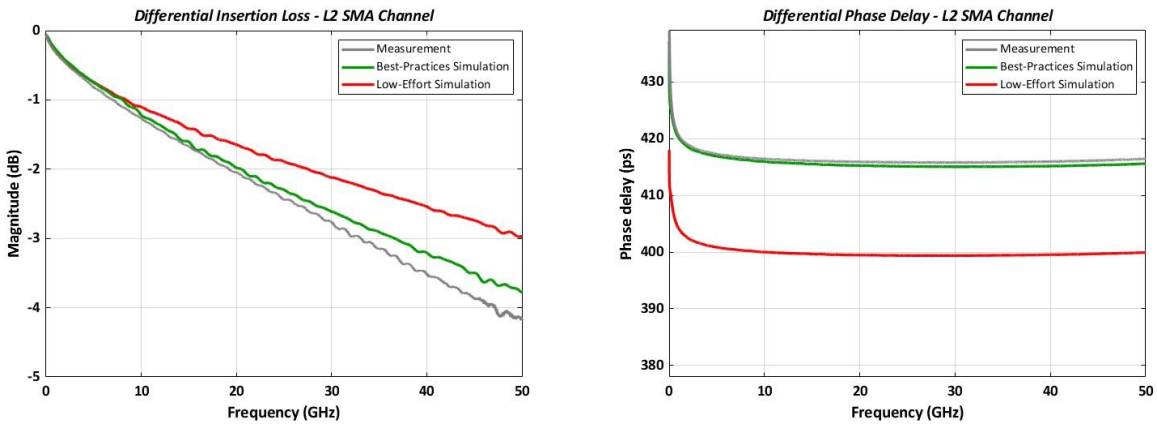

Figure 8: L2 SMA Channel Insertion Loss and Phase Delay Correlation

This first channel is a 30mm differential trace segment on L2 with 10mm of SE trace on either side and a TOP-L2 microvia connecting to a 1.85mm SMA. This is the simplest design on the board, and shows a first look at the impact of best simulation practices. As can be seen, the phase delay lines up very closely between simulation and measurement, but there is some additional loss that isn't accounted for. Note that most of the difference between best-practices and low-effort comes from dieletric modelling and surface roughness, as makes sense from the data within the previous section of this paper.

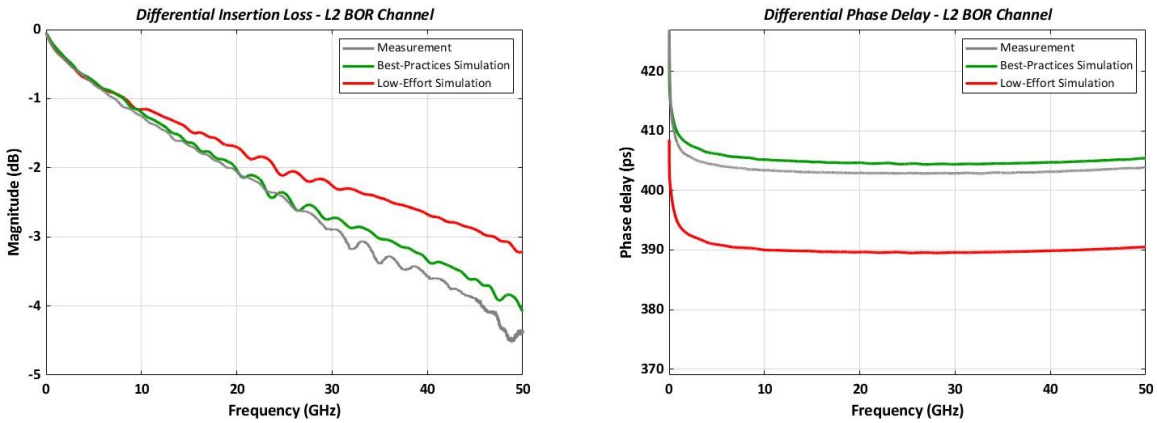

Figure 9: L2 BOR Channel Insertion Loss and Phase Delay Correlation

The channel in Figure 9 is a 30mm differential trace segment on L2 with 10mm of SE trace on either side and a TOP-L2 microvia connecting to a 1.85mm SMA. In addition, there are two L2-TOP then TOP-L2 differential via transition in the middle of the 30mm trace segment with 6mm of microstrip connecting them. This is meant to simulate the BOR region of a connector, without the actual connector being present. The results of this simulation are very similar to the previous one, which makes sense given it is of the same board. Once again, the best practices simulation is more accurate, though this time the IL is closer and the phase delay is slightly further away.

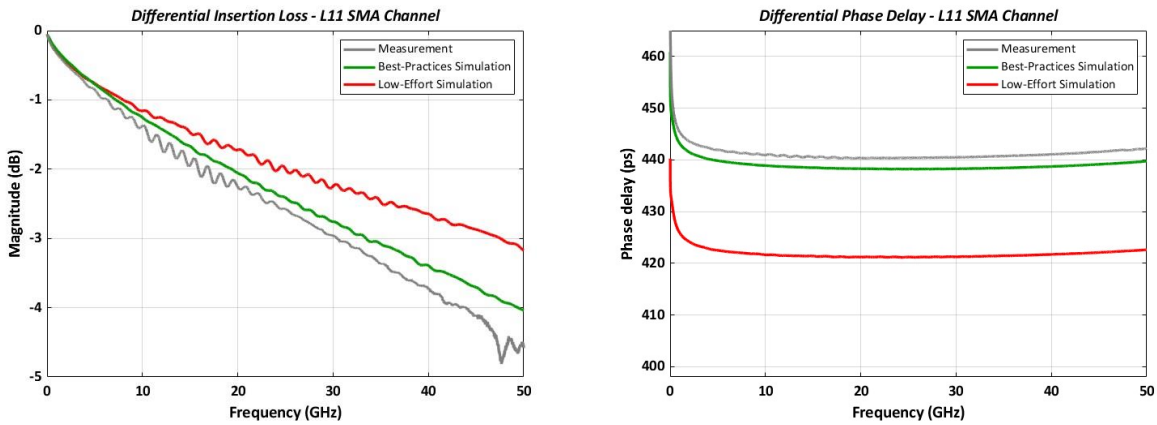

Figure 10: L11 SMA Channel Insertion Loss and Phase Delay Correlation

This final channel is a 30mm differential trace segment on L11 with 10mm of SE trace on either side and a TOP-L11 through via connecting to a 1.85mm SMA. This is the longest via in the board, meant to test the high-frequency performance of deeper vias on 224G capable test boards. There are once again no major differences in this data, with best-practices being much closer to the measurements as compared to the low-effort simulation. The baseline correlation is slightly worse in L11 as compared to in L2.

In total, this data shows that although CT-scans or cross-sections are necessary to fully understand how manufacturing varaition affected a board, good simulation practices can be instrumental in getting a much better fit right at the start. All three of these simulations were done with the exact same settings, showing that best-practices consistently gave a more accurate model than the low-effort approach. Not only do these differences help in correlation, but they are also instrumental in accurately modelling the PCB during the design process. The data here is only one stackup, but hopefully between it and the DOE from the previous section, this paper has provided sufficient evidence of the efficacy of the contained modelling approaches for PCB characteristics.

8. Conclusion

The goal of every PCB designer is to design a PCB and then receive measurements that are exactly the same as what was designed. The unfortunate reality is that varaition in the manufacturing process as well as mistakes made in the build or design process will often result in the measurements coming out slightly or even significantly different from intention. Some of this is unavoidable, as mistakes happen and variation is an inevitability of fabrication. However, through a continous effort of learning and growing, a designer can improve and make it so that each subsequent board (be they on the same stackup or a different one) performs slightly better and is more closely correlated than the previous. This only becomes more important as frequencies increase and 224G or 67GHz becomes the target.

This paper has gone into great detail on the nature of PCB simulation, with a focus on the fundamentals of accurate simulation modelling. This is intended to be a starting point for any individual entering the field, or learning about a different characteristic that they weren't already familiar with. This paper is not meant to be the final word on the matter, as technology is progressing rapidly and some of the specific information contained within will likely be dated within a few years. Instead, the authors intend for each reader to take the information here and build upon it into something useful for their own work and experience.

At the start of this paper, we discussed the issues with some of the more exotic modelling methodologies. They can be very specific to a particular panel and/or a particular stackup. They often require a board to have already been built and then correlated to be useful. The techniques presented and discussed throughout the paper have been general, such that they are agnostic to any one stackup. However, do not interpret this as a condemnation of more complicated modelling methodologies. General modelling techniques are exactly what their name implies, general. If the reader has a more accurate modelling method for a specific stackup or has time to perform a more complete correlation of its properties, then that data should clearly be used instead of the information within this paper. General methods are the baseline starting point, so that future work can build upon and expand those techniques further.

It is therefore our hope as authors that the reader will use this information to start building their own database of simulation methodologies. The sources provided have a wealth of additional information that couldn't be contained within this paper, and there are numerous modelling techniques that in the right situation will give better results than what was utilized here. Use this paper and its research to help further an ever-growing list of techniques and approaches to ensure every model is better than the last.

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