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January 30 – February 1, 2024

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Impact of Finite Interconnect Impedance Including Spatial and Domain Comparison of PDN Characterization

Ethan Koether, Amazon Project Kuiper
Kristoffer Skytte, Cadence

John Phillips (Cadence), Shirin Farrahi (Cadence), Julia Van Burger (Samtec), Abe Hartman (Oracle), Mario Rotigni (retired), Jason Miller (Amazon), Gustavo Blando (Samtec), Istvan Novak (Samtec)

SPEAKERS

Ethan Koether

Sr. Signal and Power Integrity Engineer, Amazon Project Kuiper
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Ethan Koether earned his master's degree in EECS in 2014 from MIT then spent seven years as a hardware engineer at Oracle. He then joined Amazon's Project Kuiper as a Sr SIPI engineer. His interests are in commercial power solutions and power distribution network design, measurement, and analysis.

Kristoffer Skytte

Application Engineer Architect, Cadence
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Kristoffer Skytte has 20 years experience working on chip, package, board and full system analysis including SI, PI, thermal, and EMC challenges. His recent efforts are on examining differences between measurement and simulation. He holds an M.Sc.EE. degree from the Technical University of Denmark.

SPEAKERS

Shirin Farrahi

Sr. Principal Software Engineer, Cadence

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Shirin Farrahi is working on SI and PI tools for automated PCB design. Prior to joining Cadence, she spent four years as a Hardware Engineer in the SPARC Microelectronics group at Oracle. She received her Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology.

John Phillips

Sr. Principal Application Engineer, Cadence

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John has 30+ years experience working on SI, PI, and EMC challenges at the chip, board, and system level in applications including high-end computing and mil-aero. He holds an MSc. from Bolton University, UK. His current interests are SI/PI co-simulation and modelling for high-speed interfaces.

Julia Van Burger, Samtec

Intern, Samtec

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Julia is pursuing her master's degrees in electrical engineering at Northeastern University and is a SI/PI intern at Samtec. She has a strong coding background and has transitioned her focus to power systems.

Abe Hartman

Principal Hardware Engineer, Oracle

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Abe works on system SI/PI at Oracle and has worked at Amphenol TCS, Juniper Networks, Enterasys, and GM. Abe holds a MS in EE from UMass-Lowell, a MS in Engineering Science from Rensselaer Polytechnic Institute, and a BS in both ME and EE from Kettering University in Flint, MI.

SPEAKERS

Mario Rotigni

Retired

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Mario retried after a 45-year career in R&D working on micro-controllers and EMC for automotive applications. He has co-authored 22 papers about EMC of Integrated Circuits and is a member of the IEEE EMC Society.

Gustavo Blando

Sr. Principal SI Architect, Samtec

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In addition to Gus's leadership roles at Samtec, he is charged with the development of new SI/PI methodologies, high speed characterization, tools and modeling. Gustavo has 25 years of practical experience in SI and high-speed circuit design. He has participated in numerous prize-winning conference publications.

Jason Miller

Hardware Manager, Amazon Annapurna Labs

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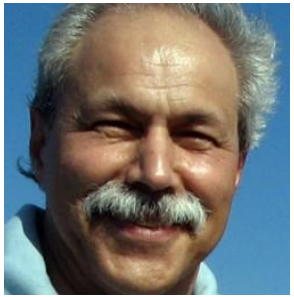
Jason leads the SI/PI team at Annapurna Labs and previously led the ASICs SI/PI team at Oracle. He has published numerous SI/PI papers on modeling and simulation and co-authored the book *Frequency-Domain Characterization of PDNs.* Jason holds five US patents and has a PhD in EE from Columbia University.



Istvan Novak

Principal SI/PI Engineer, Samtec

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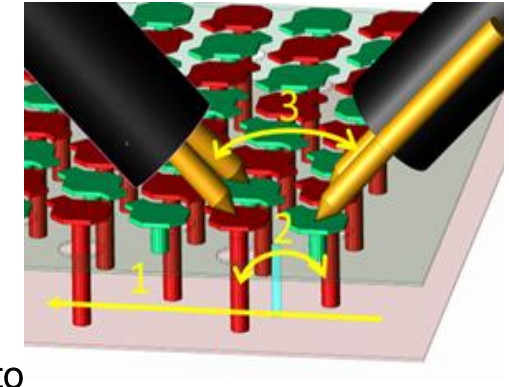
Istvan works on advanced SI/PI designs at Samtec and was previously a Distinguished Engineer at SUN later Oracle. He introduced the first 25μm power-ground laminates for large rigid PCBs and worked to create a series of low inductance, controlled-ESR capacitors. He is a Life Fellow of the IEEE with 25 patents, author of two books on PI, teaches SI/PI courses, and maintains a popular SI/PI website. He was named Engineer of the Year at DesignCon 2020.

OUTLINE

- Background
- Impedance Definitions and PDN S-Parameter Measurements
- Wafer Probe Considerations in PDN Measurements
- Low Impedance Measurement Setup
- IEEE Benchmark Board Analysis
- Production Board Analysis
- Conclusion

BACKGROUND

- The PDN impedance required in today's high-power electronic systems is no longer in the mΩ range, and may be 100 μΩ or less
- The design and measurement procedures developed in the last few decades must be re-visited and updated accordingly
- Three major aspects of PDN measurements and simulation are investigated:
  - The spatial effects associated with large via arrays in low-impedance PDNs (1 in figure)
  - The impact of via coupling within the Device Under Test (2 in figure)
  - The impact of probe-tip coupling in wafer probe calibrations and measurements (3 in figure)
- The purpose is to explore these relationships and provide insight to designers to correctly take the spatial and other 3D effects* into account to face the new level of performance needs

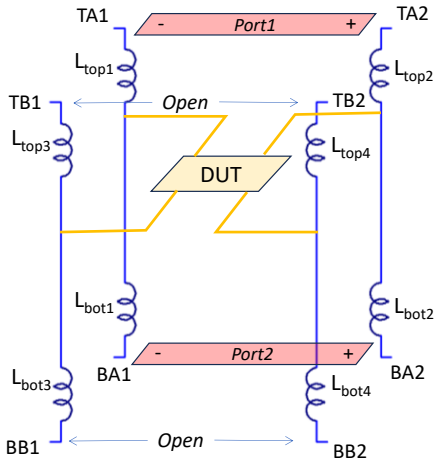


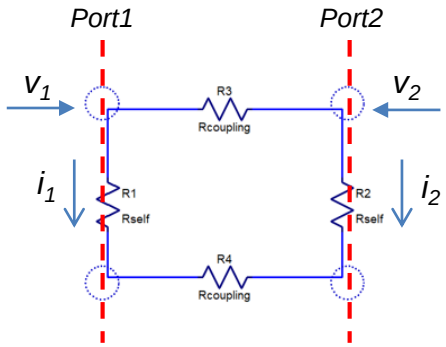
* Koether et al. "3D Connection Artifacts in PDN Measurements" DesignCon 2023

IMPEDANCE DEFINITIONS

- The normalized impedance matrix can be calculated from the S parameters
- With two power-ground via pairs, there are multiple options to approximate impedance
  - TOP-DOWN data along one via captures the DUT impedance most closely
    - No loop coupling, no spatial attenuation
  - DUT impedance can be approximated from S21
- The transformation uses all four S parameters
  - Reflection terms are very inaccurate for large reflections
  - For many PDN impedances $|S_{ii}| \sim 1$

$$\begin{bmatrix} Z_{11n} & Z_{12n} \\ Z_{21n} & Z_{22n} \end{bmatrix} = \begin{bmatrix} \frac{2\Delta_1 S_{11} + S_{12}S_{21}}{4} & \frac{S_{12}}{2} \\ \frac{S_{21}}{2} & \frac{2\Delta_2 S_{22} + S_{12}S_{21}}{4} \end{bmatrix}$$

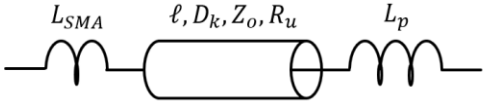




PROBE MODELS

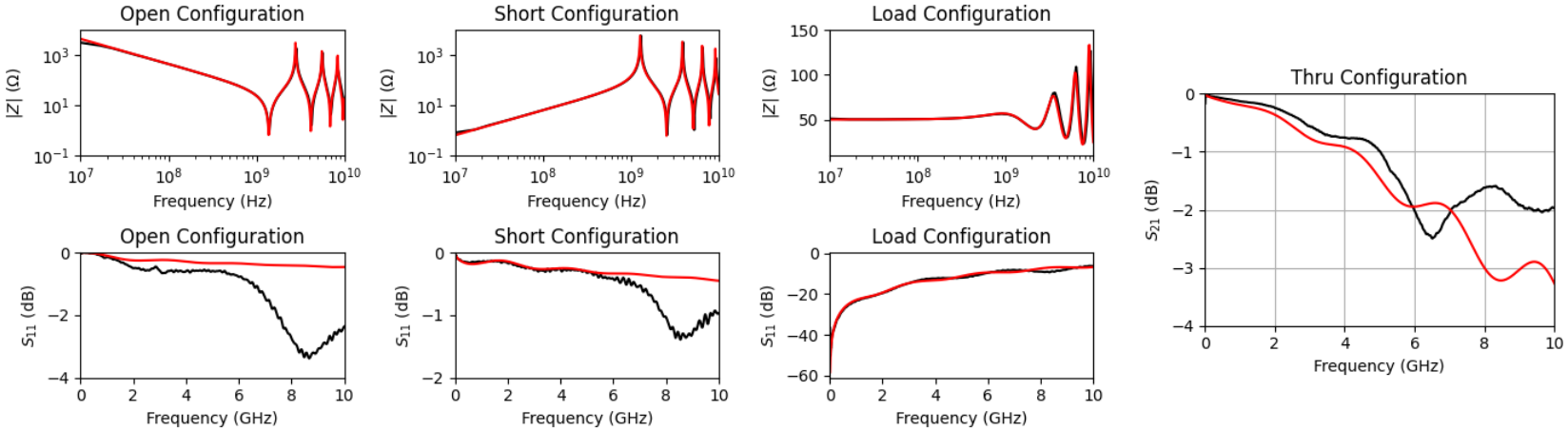
- Probe models consist of series coax with lumped inductance to emulate the separated landing pins

Right: (1) Example wafer probe
(2) model of wafer probe.



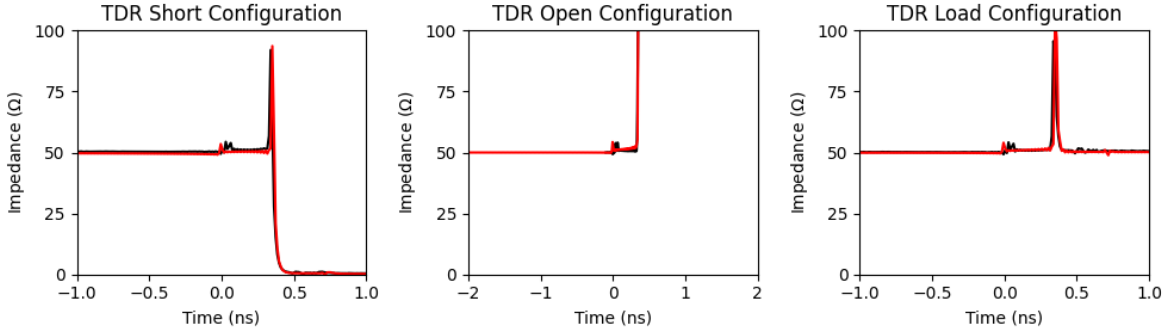
$L_p = 0.935nH$ $L_{SMA} = 50pH$
$\ell = 36mm$ $R_u = 2\Omega/m$
$D_k = 2.175$ $Z_o = 51\Omega$

- Measurements (black) and fitted probe model (red) to illustrate probe electrical behavior

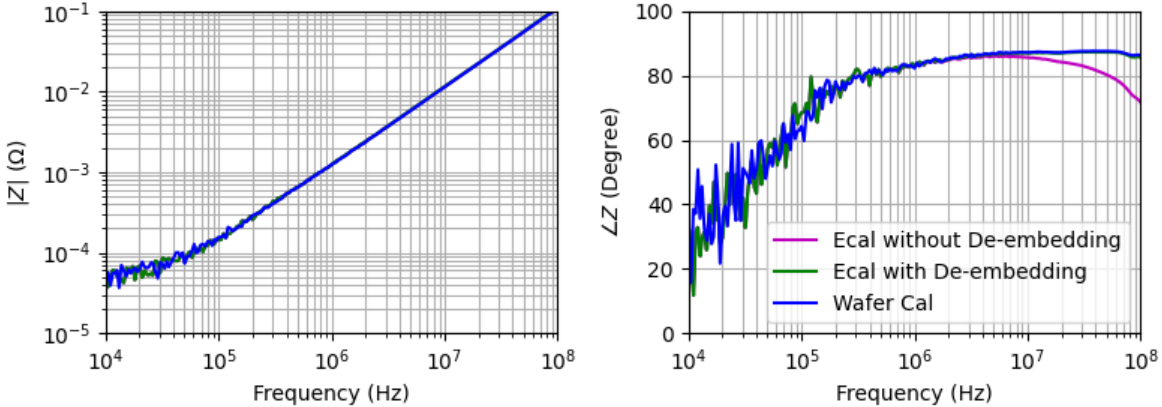


PROBE MODELS

- TDR of measurements (black) and fitted probe model (red) to illustrate probe electrical behavior



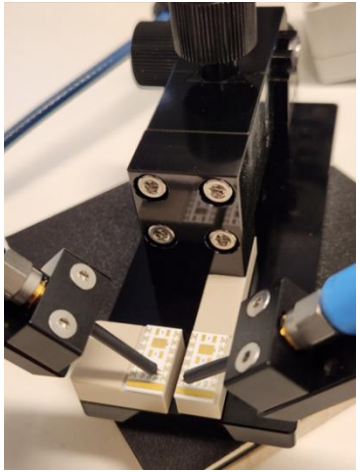
- De-embedding not necessary for frequencies below 10MHz

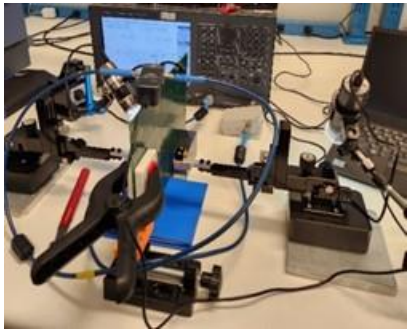


Left: Impedance measurement taken of shorted structure with wafer cal to end of probe tips (blue), with ecal to end of coax cables without wafer probes de-embedded (green) and without wafer probes de-embedded.

MEASUREMENT SETUP AND CALIBRATION

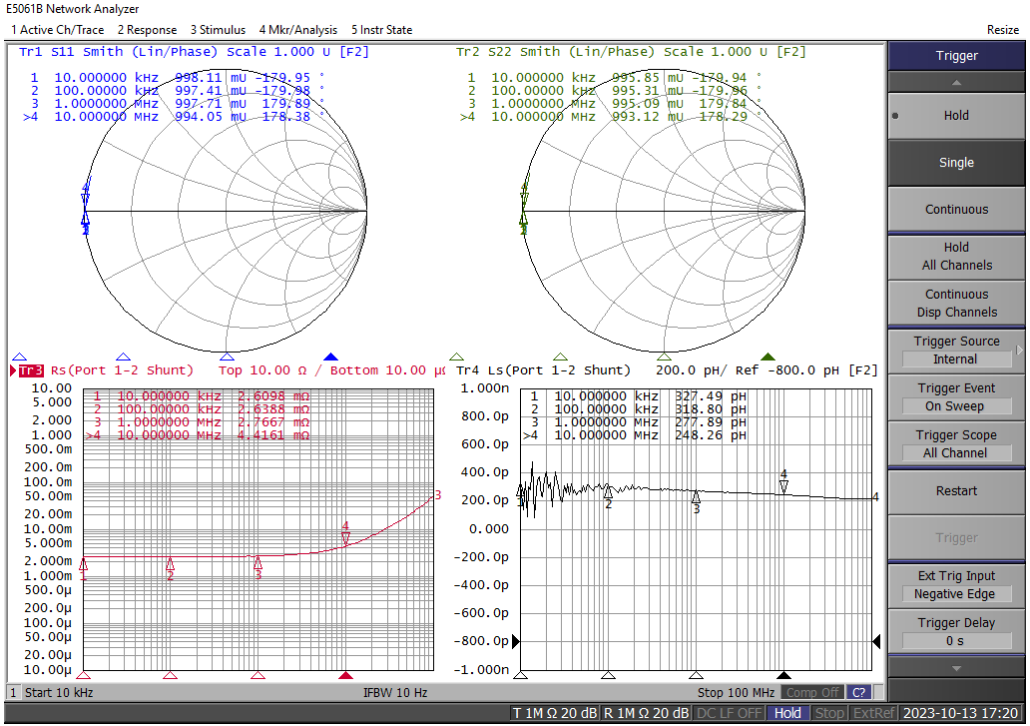
- Keysight E5061B-3L5 5Hz-3GHz 2-port VNA
- Keysight N7550A DC-4GHz Ecal unit
- Keysight N85561A mechanical calibration kit
- Custom common-mode choke
- Various sweeps used for the different tests
  - 100Hz-10MHz log (regular impedance measurements)
  - 10Hz-3GHz log (full-band noise floor test)
  - 10kHz-100MHz log (quick checks)
  - 2MHz-3GHz lin (probe characterization)
- PacketMicro RP-GR-121510 1mm probes
- PacketMicro TCS50-V2 calibration substrate
- PacketMicro custom substrate positioner





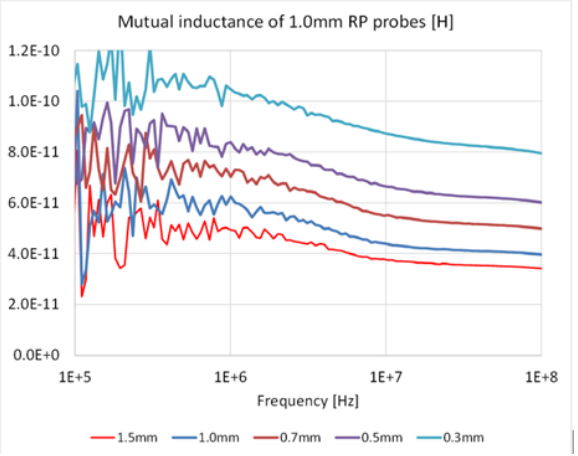
MEASUREMENT SETUP AND CALIBRATION

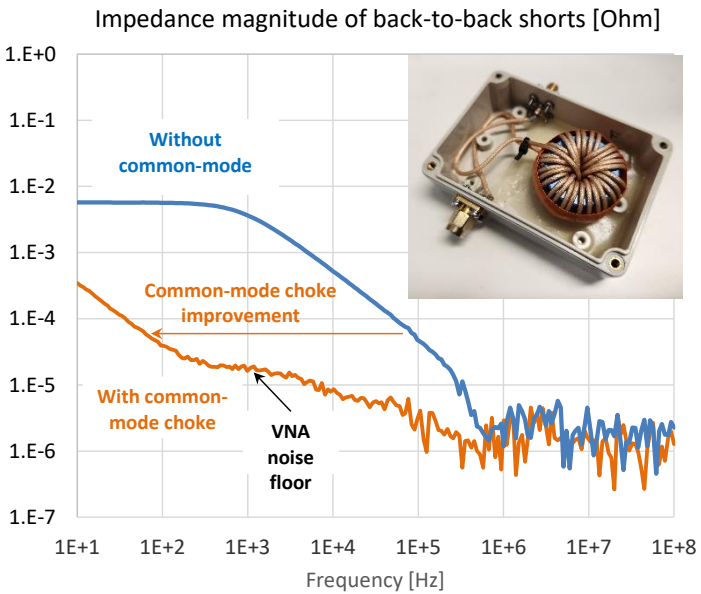
- VNA screen is set up to facilitate robust probe landing
  - Smith plot format of S_{11} and S_{22} visually confirm landing
  - Lower left plot shows the ESR value extracted from S_{21}
  - Lower right plot shows the ESL value extracted from S_{21}
- Fast not de-embedded measurements with N7550A calibration
- More accurate measurements with N85561A (not de-embedded) and TCS50-V2 (de-embedded)



REFERENCE MEASUREMENTS

- The cable-braid loop error suppression depends on multiple variables
  - Cable braid resistance and inductance (length and construction)
  - Common-mode choke braid resistance (length and construction), toroid core permeability and its frequency dependence, DC and AC bias
- VNA noise floor depends on
  - Source power
  - IF BW, averaging
- Probe spacing

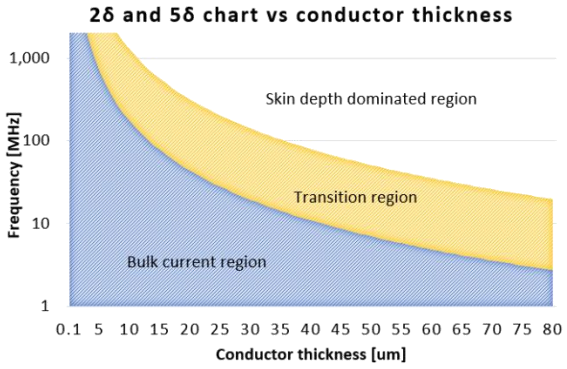


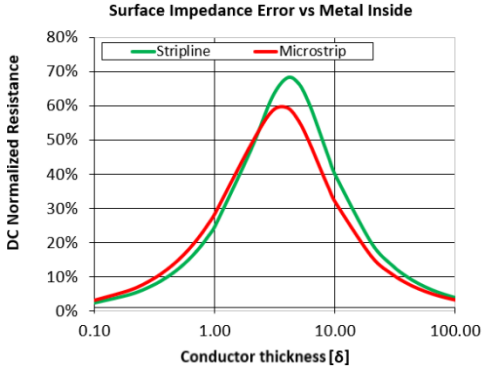


Left: Mutual inductance between two probe tip loops landed on isolated shorting strips

SIMULATION SETUPS

- Low frequency characterization can be challenging
  - Solver type, extraction settings, boundary conditions, frequency sweep etc
  - Particular importance is how metal is discretized as the band of interest is in the bulk current and transition regions – this is an area where significant error in the resistance can be made
- Power delivery = hybrid solver?
  - Normally yes, however
  - For this study a lot of the simulations for the IEEE test board were done using a 3D solver to allow full flexibility in characterization and field plotting
- Convergence judged by final parameters (RL)
  - Reported results are within ~1% of their final value at the mesh frequency (10MHz)
  - Result found not to vary with mesh frequency in frequency range of interest





Devices Under Test

Two boards are used in this work:

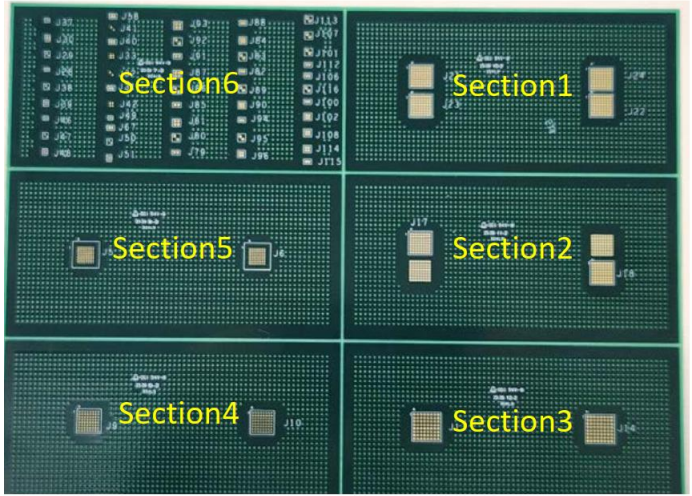
- A test board developed for the IEEE Electrical Packaging Society (EPS) technical committee on electrical design, modeling, and simulation (TC-EDMS)*
  The board ('IEEE board' in the following text) answers the need for an open-source PDN benchmark platform available to the vendors of simulation tools, verification, test and measurement solutions

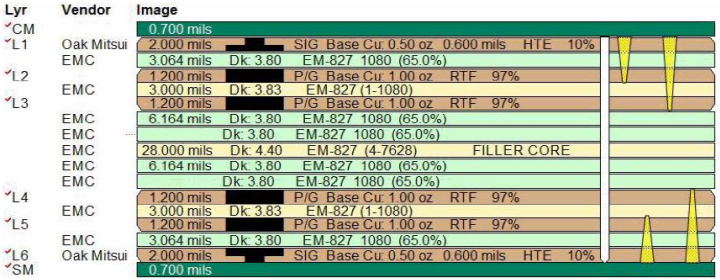
- A production board for high-power ASICs for ML/AI workloads

*Novak, et. al., "Introducing an Upcoming IEEE Packaging Benchmark," Signal Integrity Journal, 2024.

IEEE BENCHMARK BOARD

- **Designed for board low frequency wafer probe measurements**
  - Micro vias connect to solid power and ground planes on internal layers
  - 6-layer board with 6 sections, each with a different analysis target
  - Section 6 and Section 2 used for the present work



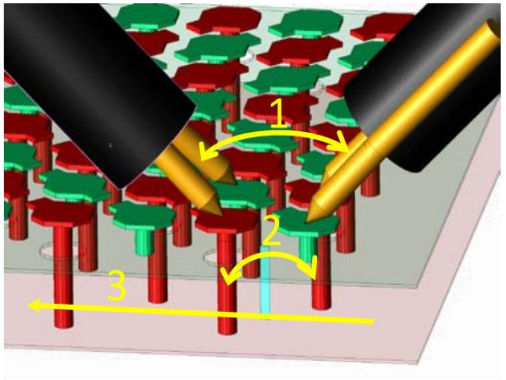


DRILL TABLE

Start Layer	End Layer	Drill Type	Plate Type	Via Fill	Stacked Via	Min Drill Size (mils)	Drill Depth (mils)
1	6	Mechanical	PTH	----	----	0.000	58.5
1	2	Laser	Micro Via	Copper Fill	No	6.000	3.7
6	5	Laser	Micro Via	Copper Fill	No	6.000	3.7
1	3	Laser	Micro Via	Copper Fill	No	10.000	7.9
6	4	Laser	Micro Via	Copper Fill	No	10.000	7.9

IEEE BENCHMARK BOARD

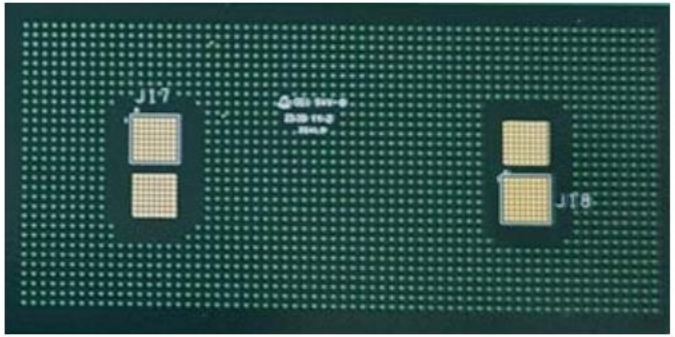
- The benchmark test board facilitates the investigation of three areas
  1. Analyzing the impact of probe-tip coupling in wafer probe calibrations and measurements
  2. Investigating the impact of via coupling within the DUT
  3. Understanding the spatial effects associated with large via arrays



- Designed for low frequency measurements and modeling
  - Well below cavity resonance frequencies
  - Single or double cavity (L2-L3, L4-L5)
- Many options offered by different isolated board sectors
  - Wafer-probe connection from same side or opposite side of board, adjacent or distant vias, and different orientations
  - Through-hole or partial blind via arrays
  - Array pitch options: 0.8mm, 1mm, or 1.27mm
  - Allows exploration of the effects of different de-embedding and calibration procedures
  - This work focuses on single cavity, through-hole vias, 1mm pitch (as supported by sector 2)

IEEE BOARD SECTION 2

- Sections 2 has four 8x8 via arrays with 1mm pitch.
- J17 and J18, used in this work connect to a single plane cavity (L2-L3 plane cavity, on the top side of the board)
- Through holes via used to make the arrays accessible from both the top and bottom side

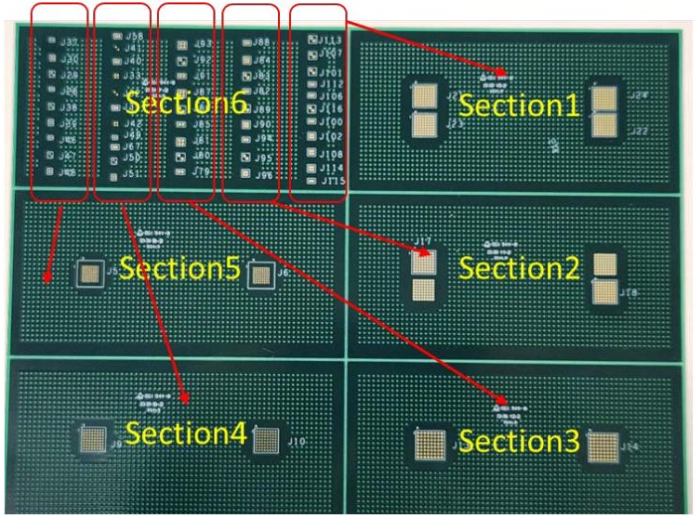


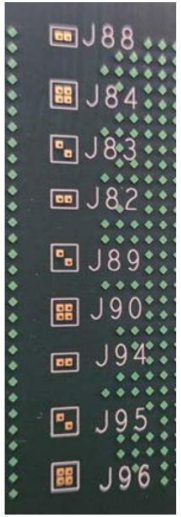
Section 2 overview

The via array

IEEE BOARD SECTION 6

- Reference structures containing through-hole via structures shorted to a single layer, mimicking VDD and VSS plane connections in a board's PDN
- Allows for measurement and simulation of short and long via loops without plane effects
  - The shorted launch, J84, will be examined – it has both the shortest loop path on the board from the top side as well as the longest loop when measured from the bottom





J88: both vias (straight) land on L3

J84: all four vias land on L2

J83: both vias (diagonal) land on L2

J82: both vias (straight) land on L2

J89: both vias (diagonal) land on L3

J90: all four vias land on L3

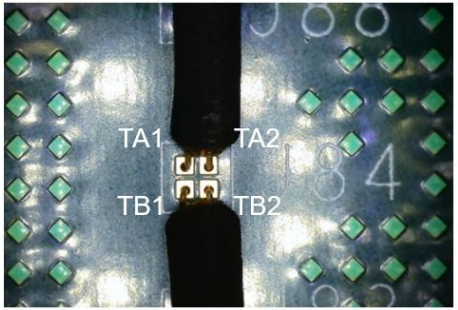
J94: straight pair landing on L2 and L3

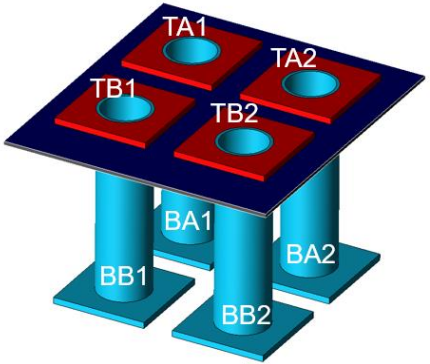
J95: diagonal pair landing on L2 and L3

J96: checker-board quad landing on L2 and L3

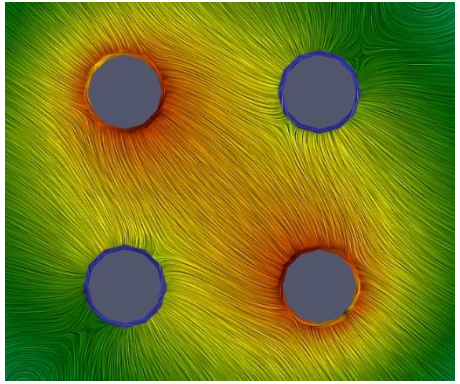
CALIBRATING OUR EXPECTATIONS

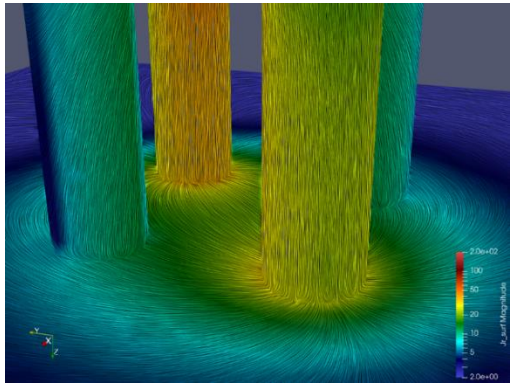
- Measuring a simple plane short seems trivial, but as we discussed in earlier paper, that may not be the case
- The geometry measured and probe connections are shown below





- Ideally we want to attach on probe at each side, but with access restrictions we often end up probing either of the two sides
- The spatial current distribution follows what minimizes the overall loss – this includes using neighboring via – it's a complex 3-dimensional current flow

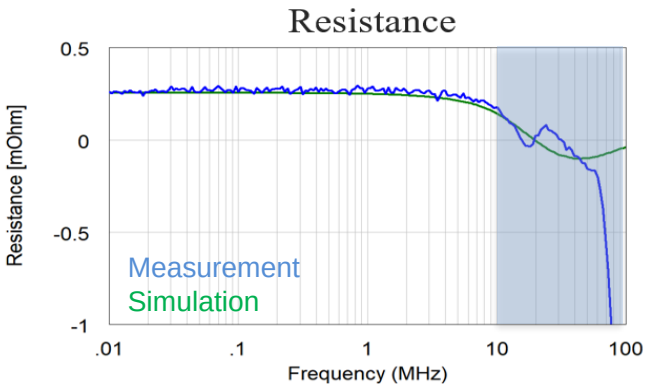


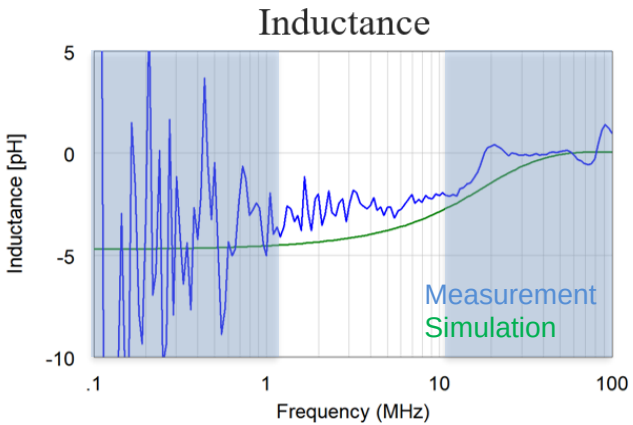


Current density distribution at 1MHz during diagonal resistance measurement

SHORTED VIA CONFIGURATION – THROUGH

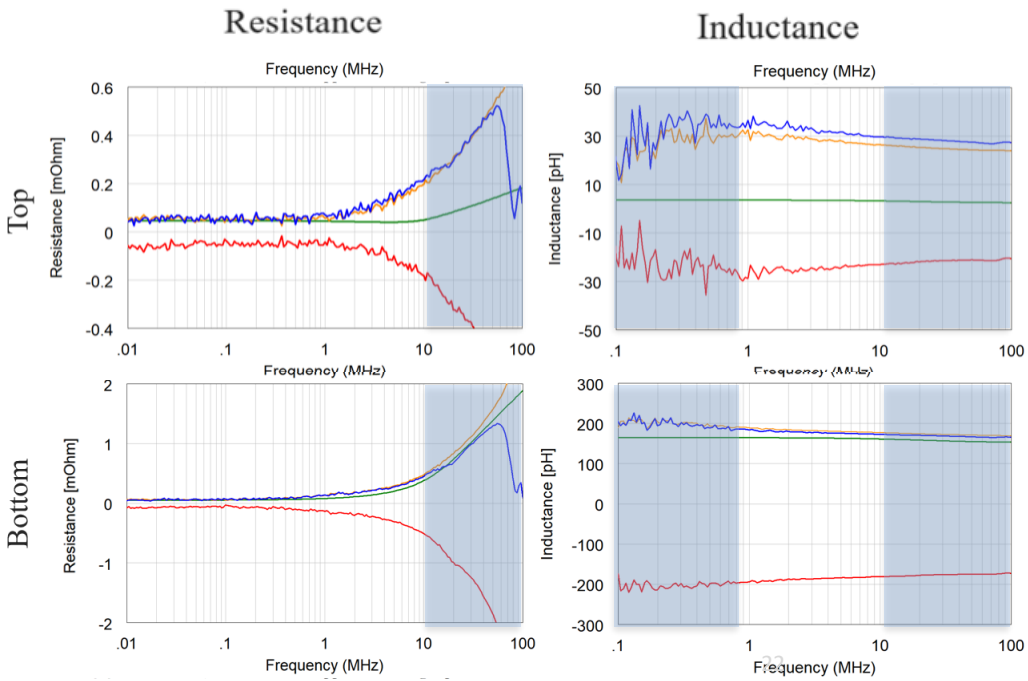
- J84 measured in through (preferred), bottom side connection (longest loop) and top side (shortest loop)
- This slide shows only through measurement
- General measurement result findings
  - R noisy < 200μΩ and valid to 10MHz
  - Inductance noisy <1MHz. As with R valid band to 10MHz
  - 10MHz bandwidth due to cable braid
  - Increasing source power and lower IF BW can improve results below 1MHz
- Simulation to measurement (through)
  - Essential features and values are well aligned
  - Through configuration has negative inductive coupling which will be discussed next





SHORTED VIA CONFIGURATION – ONE-SIDED

- Measurement depends on orientation of probe
  - Average of straight and flipped configuration should cancel out probe-to-probe coupling
- Simulation to measurement
  - Trends generally similar when comparing to average of straight and flipped orientation
  - Top side probing (short via)
    - Resistance in good agreement to 3 MHz – short via section is masked by probe coupling
    - Measurement series inductance and coupling > inductance being measured . Indications that probe contributes around 30-35pH
  - Bottom side probing (long via)
    - *Good agreement between simulation and measurement but ΔL 35pH – probe coupling may add or subtract from measured DUT impedance*

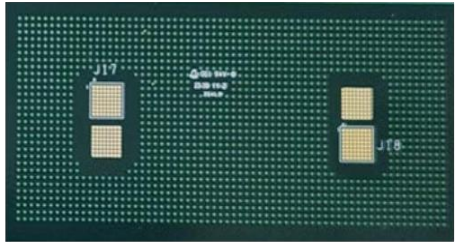


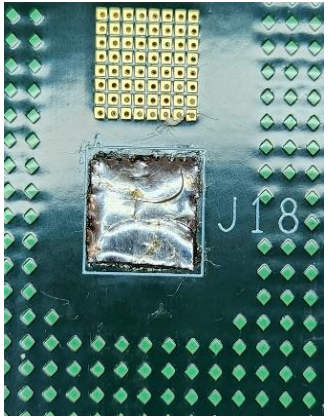
- In an actual board you may not have a choice whether probe configuration will be flipped or straight – the uncertainty in L can be a real problem

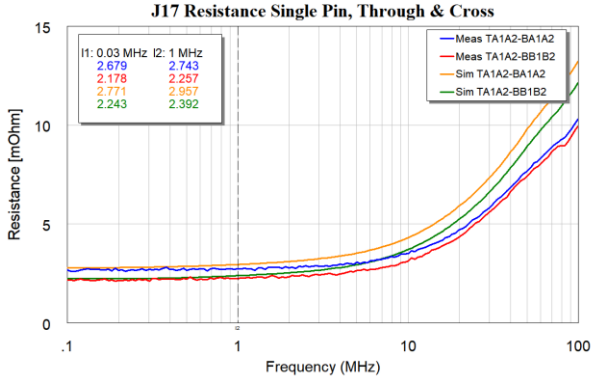
Meas – Straight probe config
Meas – Flipped probe config
Meas – Average of straight/flipped
Simulation

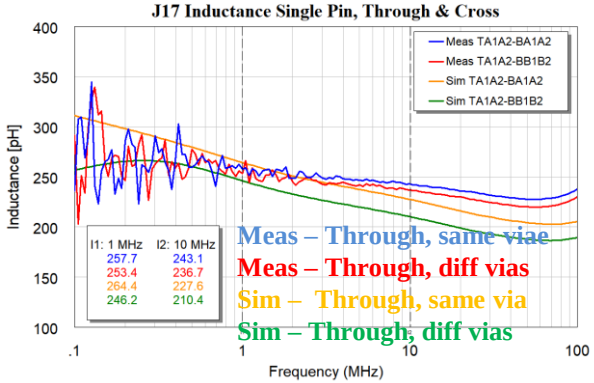
IEEE BOARD SECTOR 2 – 1MM PITCH

- Simulations mimic the lab measurement setup with J18 shorted
- Some mismatch in the predicted loop resistance because the exact properties of the plane and short conductivities are not known
  - Additional measurements have been made so that the plane and short conductivity may be determined but have not yet been implemented in the simulations
  - Using adjusted conductivities will narrow the simulation to measurement discrepancy
- Above 1MHz simulated inductance prediction is reasonably aligned



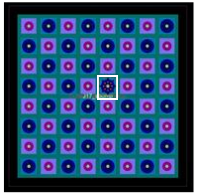




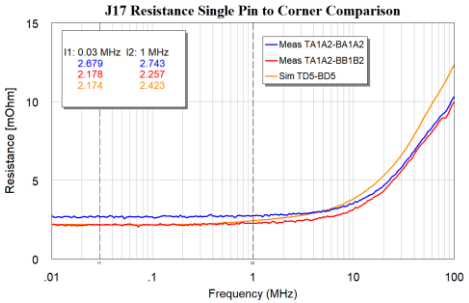


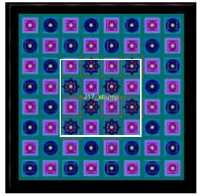
PIN GROUP STUDY

- In practical PDNs the impedance seen by the IC is through multiple paths/connections however in measurement we are restricted to using the two ports method
  - A natural question is how the measured PDN impedance using the two port method corresponds to that observed by the device itself with these multiple parallel paths.
  - By using port grouping we can emulate (within the limitations of our test board) different numbers of connections from the PCB plane to the die

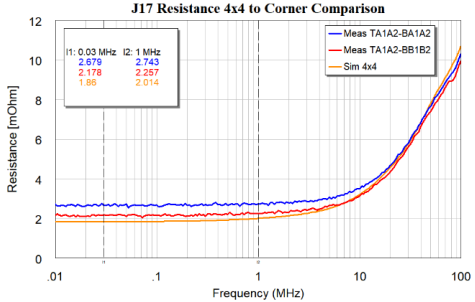


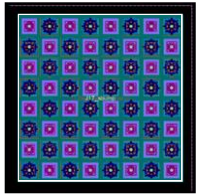
2 via pairs



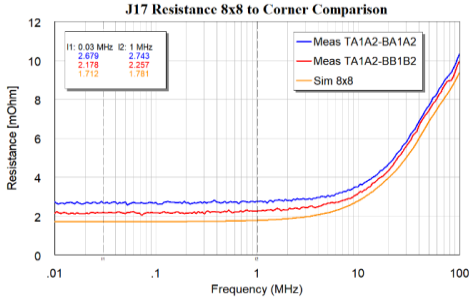


8 via pairs



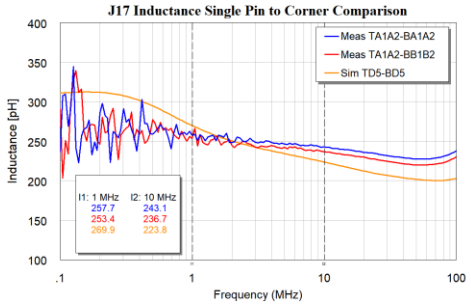


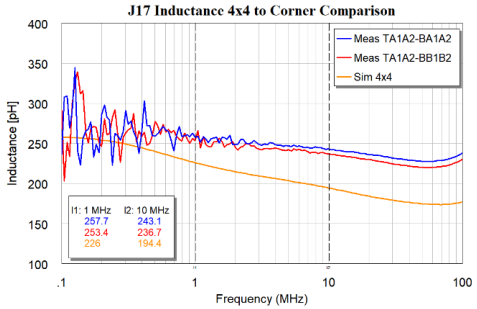
32 via pairs

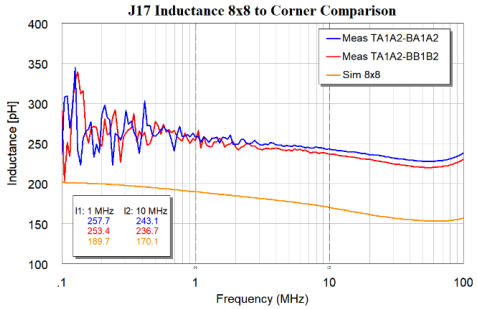


PIN GROUP STUDY – RESULTS

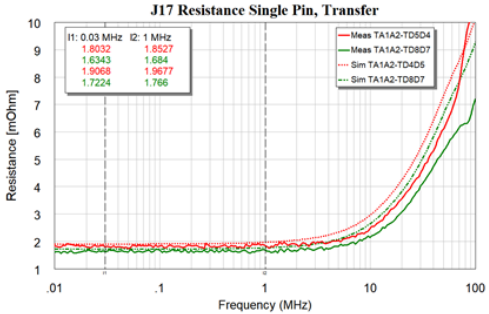
- As expected, as the number of connections to the planes increases the simulated resistance and inductance decrease and diverge from the measured results

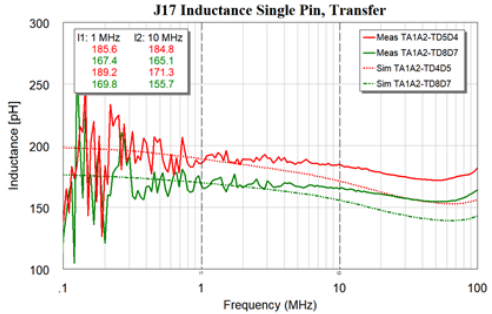






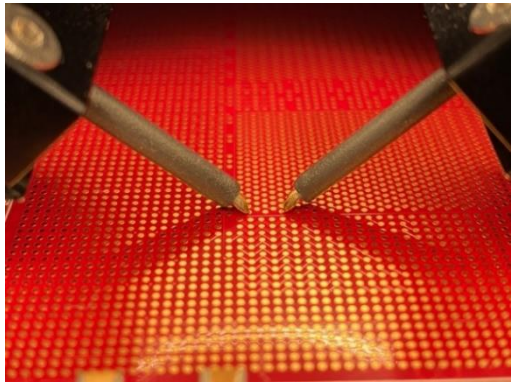
- The transfer impedance between the measurement points was also measured and simulated
  - Initially our thoughts were that we might see more loss because current must be drawn through the perforated planes.
  - This effect was not seen in measurement and the simulations confirmed the measurement results

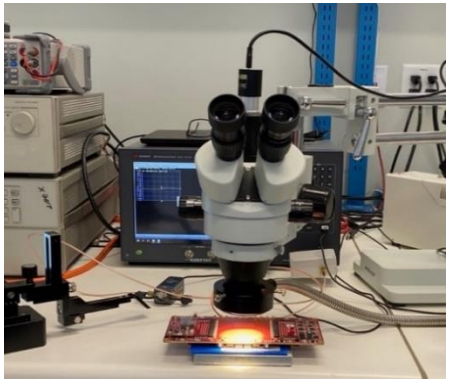




PRODUCTION BOARD

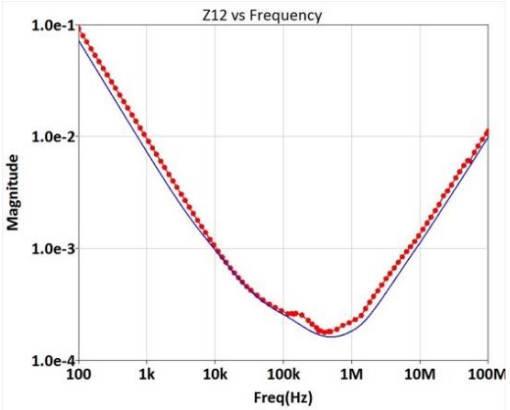
- PCB for high-powered ASICs in AI/ML applications
- Challenge here are:
  1. Probe coupling same order of magnitude as target impedance
  2. Actual impedance seen by chip distributed across BGA whereas measurement technique emulates a point impedance
- Methodology
  1. Measure with VNA in pin field with optimized setup
  2. Simulate measurement setup and correlate results
  3. Use validated simulation to explore impact of the number of P/G pins on device impedance

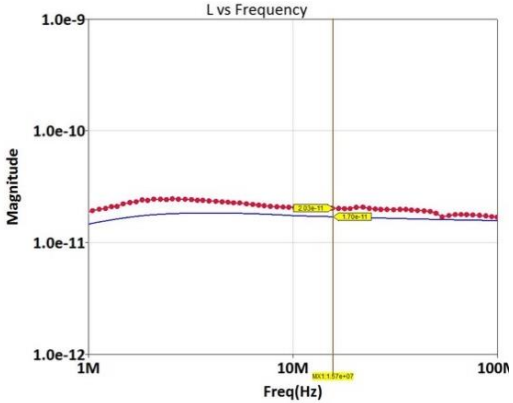




CORRELATION FOR PRODUCTION BOARD

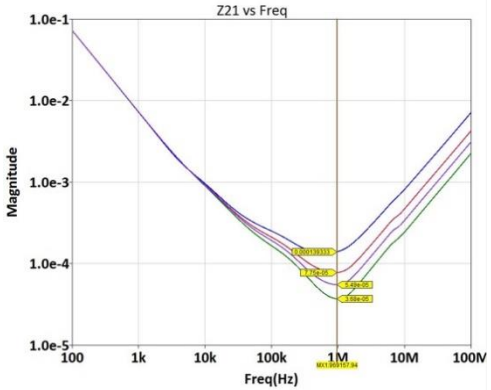
- Simulation (blue) and measurements (red)
- Good correlation over several frequency decades
- Note, the impedance is higher (simulated and measured) compared to expectations 160uΩ vs 10's of u Ω design intent
- Extracted inductance is similar to expected probe coupling inductance, potentially masking the DUT inductance

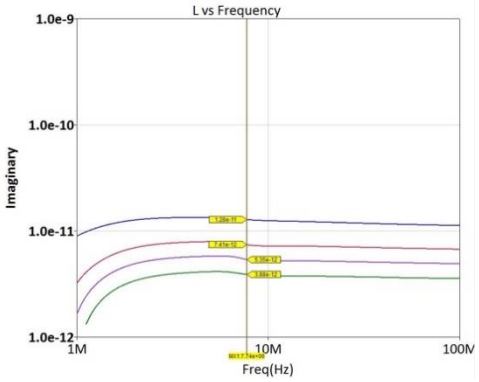


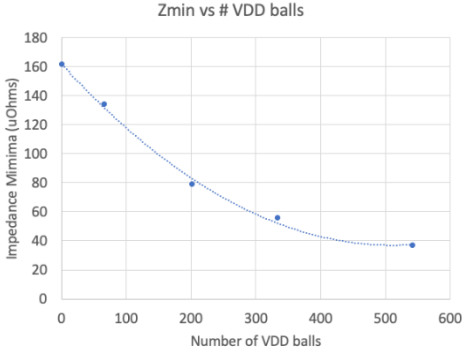


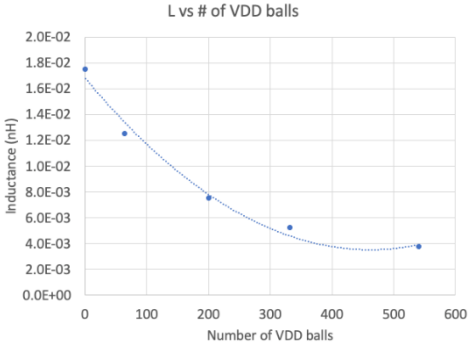
PIN GROUPING EXPLORATION

- Groupings: 25%, 50%, 75%, 100% of P/G connections
- L and Z minima follow hyperbolically decreasing trend as we increase the number of P/G balls
- Including 100% P/G connections, target impedance drops below the design impedance target (37 vs 160 micro-ohms) with the BGA pin field grouped and uniformly excited.
- Results heavily depend on structure
  - Linear scaling is valid when via impedance >> horizontal plane impedance
- Transient Load Tester sample solution to excite full BGA in measurement









Conclusions

- As we move to analyze sub-mΩ PDNs, probing artifacts strongly influence the reported impedance. We need updated measurement strategies. We recommend:
  - Continue to ignore the reflection coefficients in our s-parameter PDN measurements and focus on transfer s-parameters.
  - For PDN measurements up to 10MHz, only calibrate to the end of coax cables as wafer probes add negligible error.
  - Two-port probing off the same P/G via pair from opposite sides of the board is still the preferred measurement configuration.
  - Careful instrument setup is critical to achieving a low-noise floor. This includes IFBW, managing cable braid error, etc.
  - Probe tip coupling can mask the measured inductance by either adding or subtracting from the real value.
- We also identified two specific additional challenges in realm of sub-mΩ in terms of aligning the measured impedance with the actual impedance seen by an IC having many BGA P/G pins. Specifically:
  - Small spatial differences in probe placement can result in huge impedance changes.
  - Vertical connections can mask the actual PDN impedance. Mitigation strategies for this include linearly projecting the measurement as a function of BGA P/G pins or using transient load testers to excite the full BGA P/G pin structure.
- Finally we demonstrated that measurement-simulation correlation is achievable with the two-port shunt thru technique on sub-mΩ PDNs using the recommendations and considerations above.

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Thank you!

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