Welcome to

DesignCon® 2024
WHERE THE CHIP MEETS THE BOARD

Conference
January 30 – February 1, 2024

Santa Clara Convention Center

Wednesday 1/31/2024, 4pm
Ballroom C

Expo
January 31 – February 1, 2024

PCI Express & PAM4:
The Pathway to 128GT/s and Challenges of Building Interoperable 64GT/s Capable Systems

Panel Discussion

Pegah Alavi(Keysight Technologies), Tim Wig(Intel), Steve Krooswyk (Samtec), Sam Kocsis (Amphenol)
Rick Eads (Keysight Technologies), David Bouse (Tektronix), Madhumita Sanyal (Synopsys Inc)

Speakers

Pegah Alavi

Senior Solutions Engineer
Keysight Technologies

Pegah is a Senior Applications Engineer at Keysight Technologies, where she focuses on Signal Integrity and High Speed Digital Systems and Applications. Prior to joining Keysight Technologies, Pegah worked on system level modeling of analog and mixed signal circuits in order to best predict the overall systems performance and accurately represent each component.

Tim Wig

Signal Integrity Engineer
Intel Corporation

Tim Wig joined Intel in 2001, where he works as a signal integrity engineer in a pathfinding and spec development group whose charter includes PCIe and other interconnect standards. Tim coordinates the Card ElectroMechanical (CEM) Spec document for Gen 4.0 and 5.0, and has contributed many of the signal integrity enablers that allowed PCIe to reach 16 and 32 GT/s. His primary focus is passive component, PCB, and channel level modeling, measurement, and optimization for PCIe CEM, though he also supports the M.2, U.2, and OCuLink standards. He holds a PhD in Engineering Science from Washington State University; and and a MS and BS in Electrical Engineering and a BS in Engineering Physics from the University of North Dakota. He delivered a tutorial on PCIe Gen 4.0 to DevCon 2016.

Speakers

Steve Krooswyk

New Product and Standards SI

Samtec

Steve is involved in new high-speed connector development and PCIe standards at Samtec. His 20 years of signal integrity experience has had a focus on the design, simulation, and correlation of PCIe interconnect and I/O. Previously, Steve was the PCIe tech lead for SI in Intel's data center division during Gen3 and Gen4 development. He is an author of the book High Speed Digital Design: Design of High Speed Interconnects and Signaling and holds a MS degree from the University of South Carolina.

Sam Kocsis

Director of Standards and Technology

Amphenol

Sam Kocsis currently holds the role of Director of Standards and Technology at Amphenol, focusing on the proliferation of innovative interconnect solutions. Sam coordinates Amphenol's engagement strategies in various industry standards and consortiums across networking, server/storage, optics, and commercial markets. He is active in IEEE 802.3, OIF, and OCP projects, and is currently a co-chair of the OSFP MSA and chairman of the PCI-SIG Cabling Workgroup. Sam holds BSEE and MSEE degrees from the University of Rochester, in Rochester, New York.

Speakers

Rick Eads

Principal PCIe Program Manager

Keysight Technologies

Rick Eads is a principal program manager at Keysight Technologies with expertise in technical/industrial marketing of test and measurement tools and electronic design automation software in the computer, semi-conductor, communications, and storage industries worldwide. Rick's specialty is precision product and solution definition. He provides technical leadership in driving standards within industry organizations for PCI Express, CXL, CCIX, GenZ, OCP, NVM Express, CEI 4.0, IEEE 802.3, ExpressCard, DDR, SATA, and InfiniBand. He markets test and measurement products covering oscilloscopes and associated compliance software tools, vector network analyzers, bit error ratio testers (BERTs) and EDA tools. Rick earned a MBA from the University of Colorado and holds a BSEE from Brigham Young University with an emphasis on digital design and computer architecture.

David Bouse

PCI Express Principal Technology Lead

Tektronix

David Bouse is the PCI Express Principal Technology Lead at Tektronix and has been heavily involved in PCIe Physical layer pathfinding and specification development within the PCI-SIG. His areas of focus include transmitter and receiver test methodology, test fixture design, and waveform post-processing algorithms for NRZ & PAM4. David is an active participant in the Electrical Work Group and Serial Enabling Group where he helps accelerate the pace of technology development and adoption across multiple market segments.

Speakers

Madhumita Sanyal

Senior Staff Technical Marketing Manager

Synopsys Inc

Madhumita Sanyal is a Senior Staff Technical Marketing Manager for Synopsys' high-speed SerDes PHY IP portfolio. She has over 16 years of experience in design and application of ASIC WLAN products, logic libraries, embedded memories, and mixed-signal IP. Madhumita holds a Master of Science degree in Electrical Engineering from San Jose State University and LEAD from Stanford Graduate School of Business.

PCI Express and PAM4,
Simulation challenges and considerations

Pegah Alavi

Keysight Technologies

Simulation needs

- **Multi-Level Signaling Challenges**
- **Modeling Challenges for PAM4 and high data rates**
- **Simulation must haves, designer's needs**
- **PCIe 6.0 End to End Simulation**
- **PCIe 7.0: What is coming**

Multi-Level Challenges

- Some aspects of Multi-Level Signaling design are new and/or more challenging:

  - The S/N is reduced as the number of Levels increases
    - Higher raw error rates -> FEC
  - Multiple transitions between Levels will reduce Eye widths
    - Asymmetric Eyes
  - All Levels/Eyes should be treated equally
    - Levels must be maintained linearly in amplitude (linearity)
    - Timing should be the same for all decision points (skew)
  - Equalization and Clock/Data Recovery must work for multiple decision levels
  - Additional Processing and Linearity requirements increase power consumption
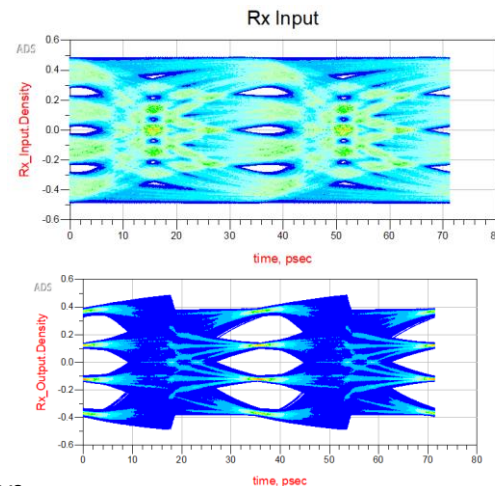
- In other words, we can go faster but we have also created new challenges…

Modeling Challenges and Simulation Must Haves

- Comprehensive Simulation Capability
  - **SER** (Up to millions per minute)
    - Eye measures
    - Bathtubs
    - Mask tests
  - **Diagnostics** for design development
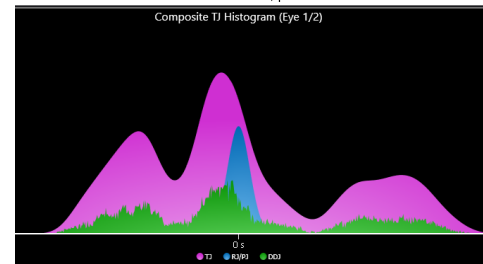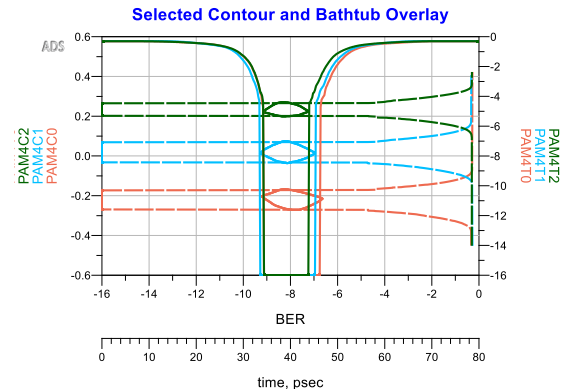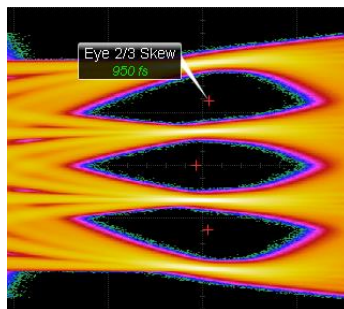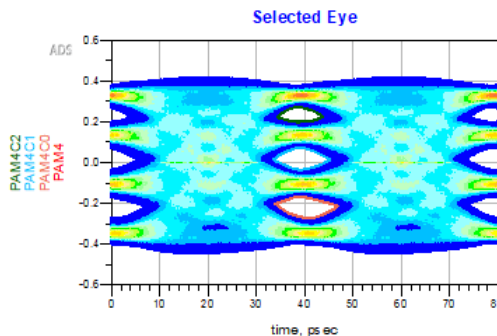   - Waveforms
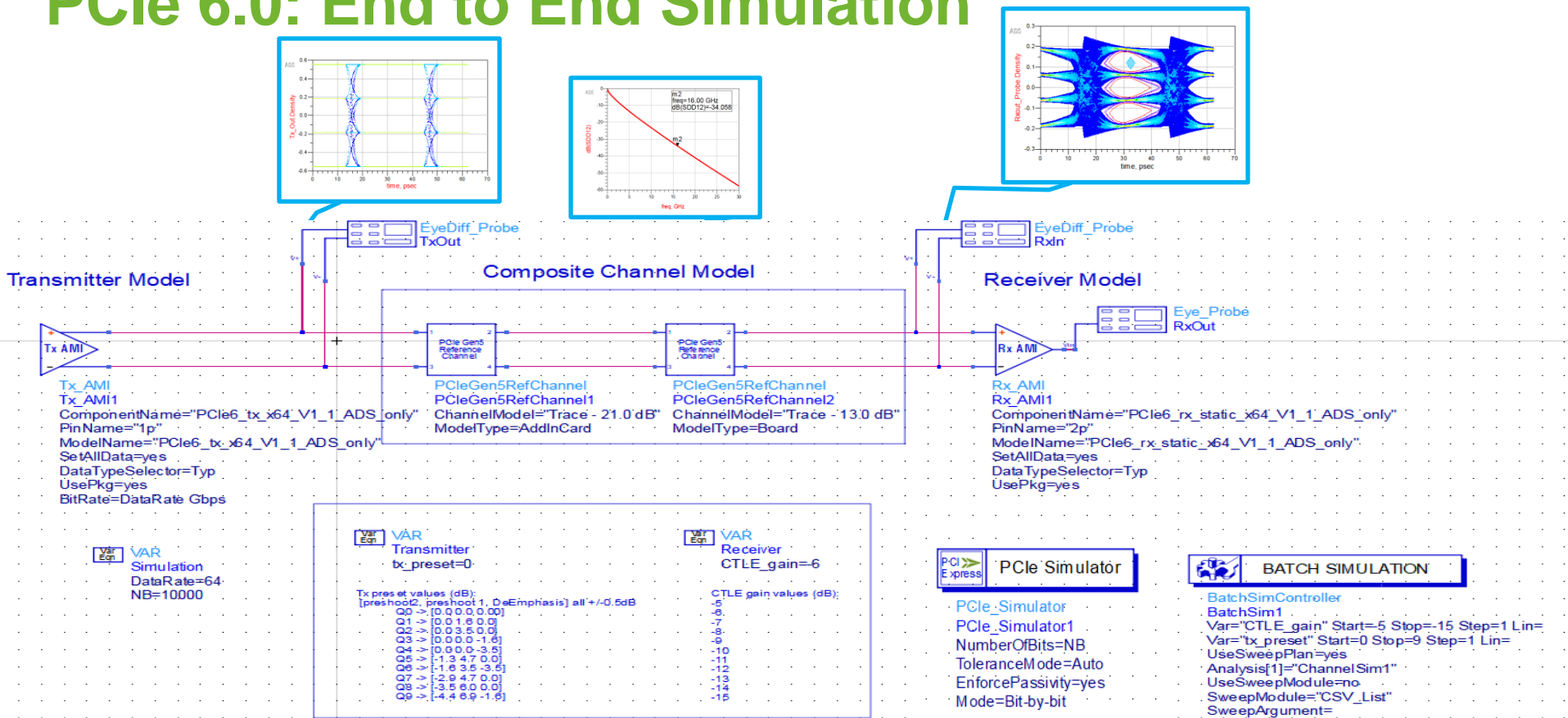   - Linearity
    - Skew
    - Jitter
  - Models
    - Channel, Pre and Post layout
    - Tx and Rx, IBIS-AMI, PAM capable, Standard Specific
  - Statistics, Swept Measurements;
    - for design space exploration and case studies

PCIe 6.0: End to End Simulation

Transmitter Model

Tx_AMI
Tx_AMI1
ComponentName="PCIe6_tx_x64_V1_1_ADS_only"
PinName="1p"
ModelName="PCIe6_tx_x64_V1_1_ADS_only"
SetAllData=yes
DataTypeSelector=Typ
UsePkg=yes
BitRate=DataRate Gbps

Composite Channel Model

EyeDiff_Probe
TxOut

PCIe Gen5 Reference Channel

PCIeGen5RefChannel
PCIeGen5RefChannel1
ChannelModel="Trace - 21.0 dB"
ModelType=AddInCard

PCIe Gen5 Reference Channel

PCIeGen5RefChannel
PCIeGen5RefChannel2
ChannelModel="Trace - 13.0 dB"
ModelType=Board

Receiver Model

EyeDiff_Probe
RxIn

Eye_Probe
RxOut

Rx_AMI
Rx_AMI1
ComponentName="PCIe6_rx_static_x64_V1_1_ADS_only"
PinName="2p"
ModelName="PCIe6_rx_static_x64_V1_1_ADS_only"
SetAllData=yes
DataTypeSelector=Typ
UsePkg=yes

VAR
Simulation
DataRate=64
NB=10000

VAR
Transmitter
tx_preset=0

Tx preset values (dB):
[preshoot2, preshoot 1, DeEmphasis] all +/-0.5dB
Q0 -> [0.0 0.0 0.00]
Q1 -> [0.0 1.6 0.0]
Q2 -> [0.0 3.5 0.0]
Q3 -> [0.0 0.0 -1.6]
Q4 -> [0.0 0.0 -3.5]
Q5 -> [-1.3 4.7 0.0]
Q6 -> [-1.6 3.5 -3.5]
Q7 -> [-2.9 4.7 0.0]
Q8 -> [-3.5 6.0 0.0]
Q9 -> [-4.4 6.0 -1.6]

VAR
Receiver
CTLE_gain=6

CTLE gain values (dB):
-5
-6
-7
-8
-9
-10
-11
-12
-13
-14
-15

PCIe Simulator

PCIe_Simulator
PCIe_Simulator1
NumberOfBits=NB
ToleranceMode=Auto
EnforcePassivity=yes
Mode=Bit-by-bit

BATCH SIMULATION

BatchSimController
BatchSim1
Var="CTLE_gain" Start=-5 Stop=-15 Step=1 Lin=
Var="tx_preset" Start=0 Stop=9 Step=1 Lin=
UseSweepPlan=yes
Analysis[1]="ChannelSim1"
UseSweepModule=no
SweepModule="CSV_List"
SweepArgument=

PCIe 7.0: What is coming

- **Data Rate: 128 Gb/s (PAM4)**
- **BER: 1e-6**
- **SNDR: 34 min (same as PCIe 6.0)**
- **RLM: 0.95 min (same as PCIe 6.0)**
- **Channel: 4" – 14" (similar to PCIe 6.0)**
  - Loss -36dB to -40dB
- **Tx equalization (Proposed)**
  - 4-tap FIR
- **Rx equalization (Proposed)**
  - Reference CTLE (6poles, 3 zeros, gain range 0 to -20dB)
  - ADC based Rx Architecture (FFE with 24 post-cursor and 4 pre-cursor taps, + 1-tap DFE)
  - $h1/h0 < 0.5$
- **Rx eye mask (TBD)**

PCIe 7.0: Get Ready!

- **Simulation more important than ever!**
- **Preliminary models are ok**
  - Represent as many imparities as possible
- **Both Statistical and bit-by-bit simulations are needed**

Card and Cable

Tim Wig

Intel Corporation

Physical Form Factor Updates – CEM Card
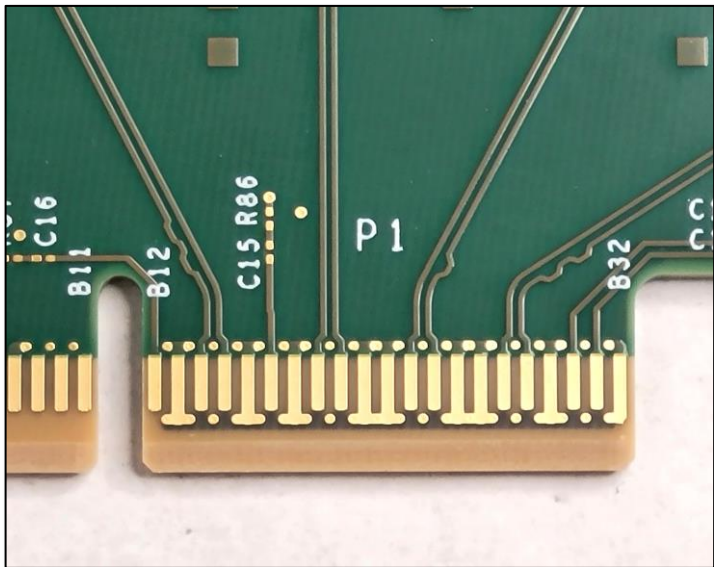
PCIe CEM 6.0 edge finger design

- Rev 6.0 of the PCIe Card Electromechanical (CEM) form factor specification reached its 0.7 maturity

- CEM 6.0 introduces updates to edge finger PCB layout for the Add-in Card edge finger geometry to improve signal integrity extending to 64.0 GT/s

- Largely extends connector baseboard footprint and Add-in Card geometry updates introduced in PCIe 4.0 and 5.0

- Early pathfinding is underway for 128 GT/s PCIe CEM 7.0

CEM Add-in Card edge finger geometry updates

- **CEM 6.0 Edge finger region introduces the "Low North" and narrower, 0.5 mm fingers**
  - Moves the geometry on the upper end of the edge finger region ↓South↓ by 0.5 mm
  - Edge finger lengths are reduced by 0.5 mm, *but the 1.8 mm stub length remains unchanged*
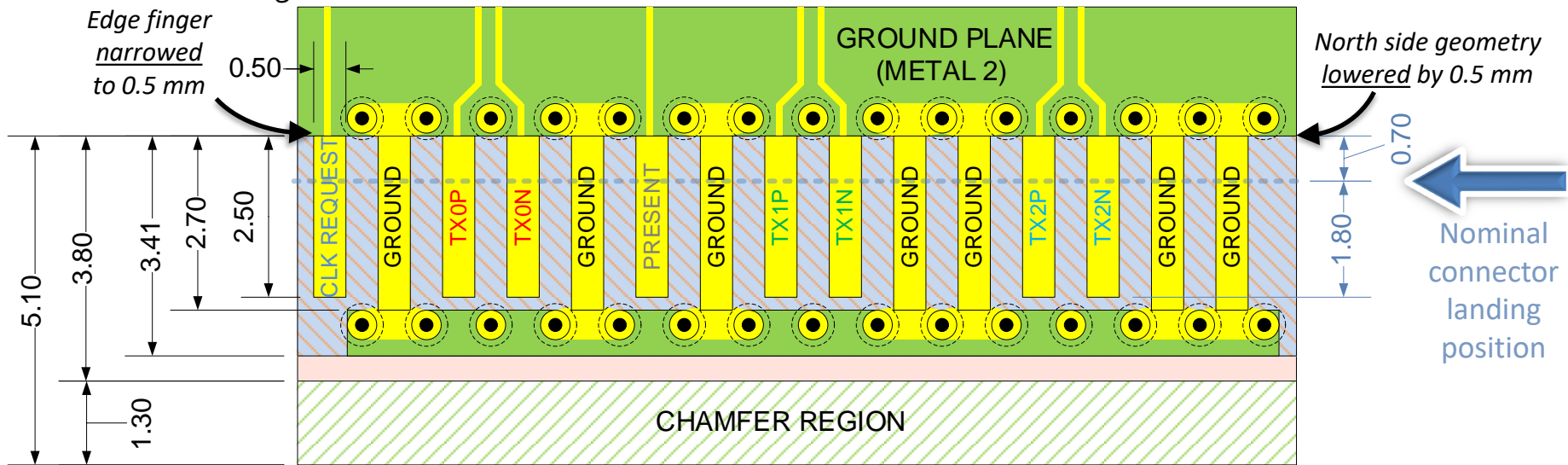
Physical Form Factor Updates – New Cables

▪ **Two new PCIe cable "CopperLink" form factors have been defined**
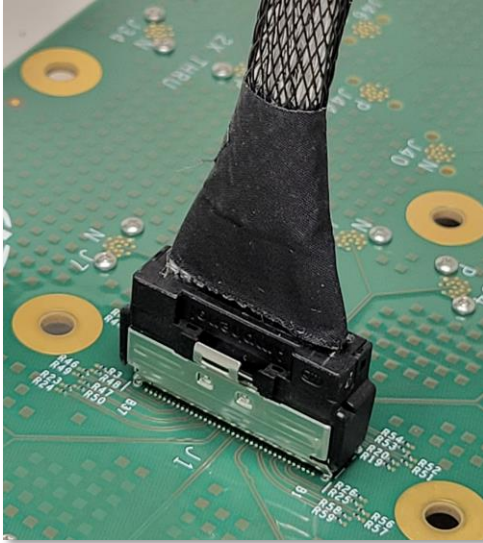
PCIe Internal Cable
Characterization fixture

▪ **An *Internal* cable, based on the EDSFF TA-1016 cable system targeting PCIe 5.0 and 6.0 speeds**

▪ **An *External* cable, based on the Industry Standard CDFP**

  o Introduces chassis-to-chassis interconnection

▪ **These are new form factors, distinct from earlier PCIe cable solutions**

PCIe CEM 12V 600W Power Updates

- **The 600W 12V power connector has been updated**
  - The 12V-2x6 connector replaces the 12VHPWR connector
  - Each connector carries four sideband signals for power management
  - Revised sideband pin configurations
    - *Updated pin lengths for contact sequencing*
    - *A new default Zero-Power state has been added to the pin to address reliability concerns*
  - The 12V-2×6 connector may be configured for 600, 450, 300, and 150-Watt power levels
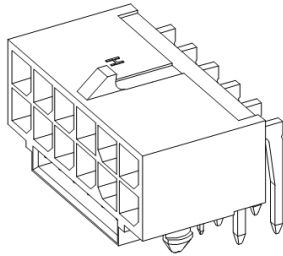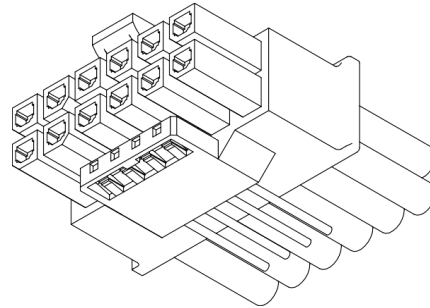
12V-2x6 PCB Header   12V-2x6 Cable Plug

Connectors and Cables

Steve Krooswyk

Samtec

PCIe 6.0 Interconnect Testing

- **Ready to test 6.0… but not sure about the interconnect…**

- **Can I use 5.0 CLB\CBB as a stop-gap for lossy channel until 6.0 is ready?**

- **Could I use 5.0 Connectors?**

- **How about 5.0 loopback cables at 6.0 speeds?**
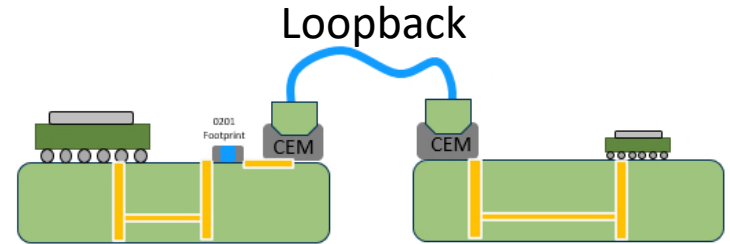
Yes! While 6.0 improves performance, 5.0 CEM is still capable to pass signals.

Remember 6.0 is more sensitive to noise, but does run at the same frequency as 5.0.

Loopback

Do I need 85 ohm cable?

Differential IL: PCIEC-G5-XXX- -XX-X-XX

100 ohm cables

85 ohm cables

- **85 ohm cable is Not required by PCI-SIG EWG or internal \ external cable spec draft**
- **Higher cable Z is lower loss (opposite of PCB)**
- **Yes there is some reflection penalty, depends on connector**
- **HF reflection is cable <> connector**
- **What does full link simulation say?**
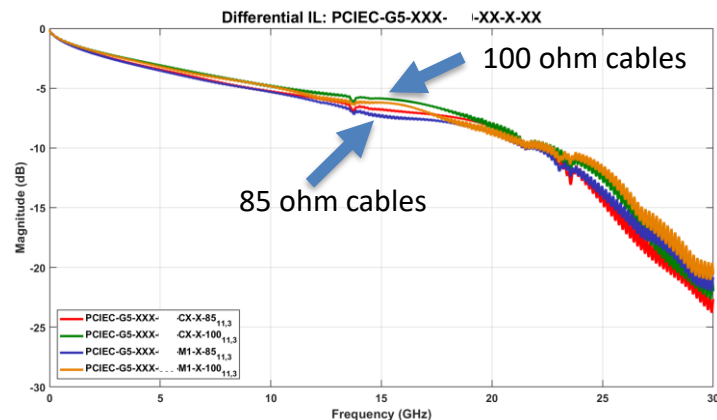
5.0 CEM Slot cables running at 64 GT/s PAM4

	Min. EH	Min. EW
M1 Extension 100 ohm	8.1mV	0.13 UI
M1 Extension 85 ohm	7.4mV	0.135 UI
CX Loopback 100 ohm	8.4mV	0.135 UI
CX Loopback 85 ohm	7.8mV	0.14 UI

Cable Pathway to Gen 7 128GT/s:

Variable air pockets induce skew

Co-extrusion for lower loss and reduced skew

Current Gen

Even lower loss
Hyper-low Skew

No wrap resonance
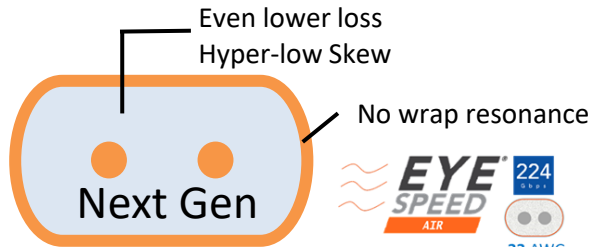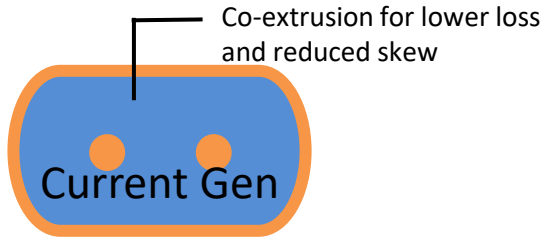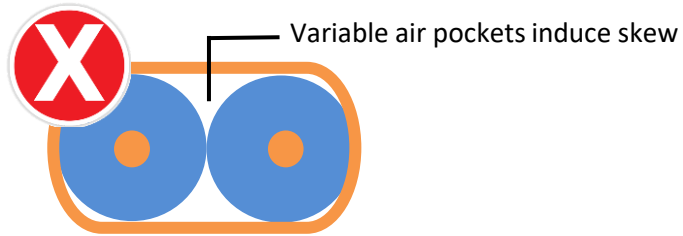
Measured Insertion Loss – Same Length

Insertion Loss - Differential

Current Gen Cable

Next Gen Cable

Magnitude (dB)

Frequency (GHz)

32 GHz
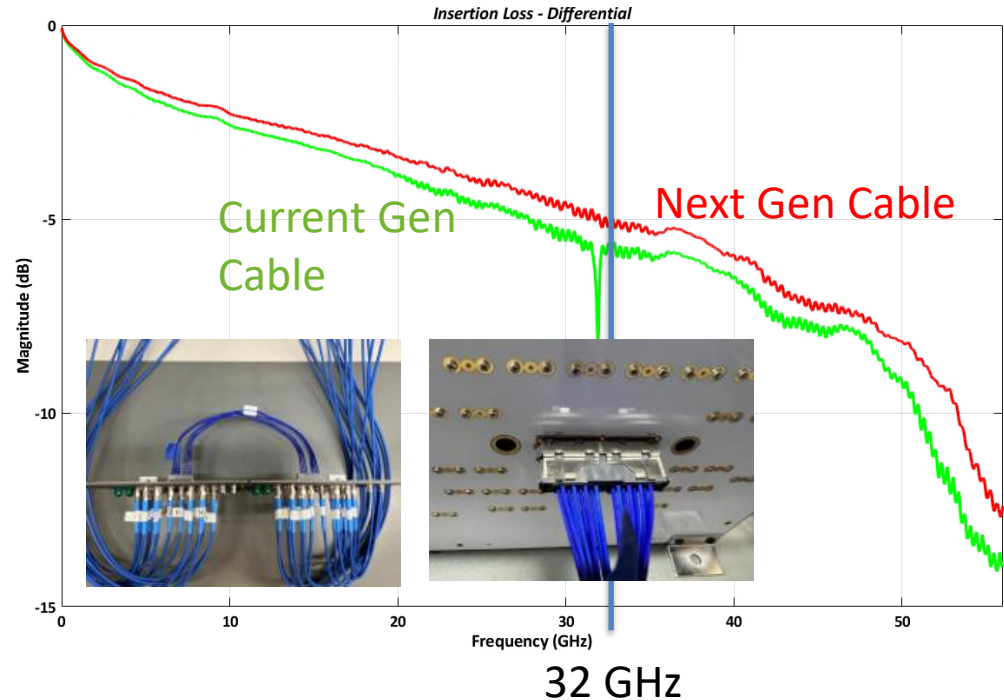
Integrated Return Loss (IRL)

The Problem

- **Connectors\Cables slightly exceed RL limit**
- **System still works**
- **False negative**

The Solution

- **IRL approves excursions that would still "work"**
- **Return Loss is filtered by W(f), and then integrated**
- **Like ICN for crosstalk**

Power Weighting Function

W(f)

16 GHz

Frequency (GHz)

Example RL and Effect of W(f)

RL_{avg}

RL_{avg} * W(f)

Frequency (GHz)
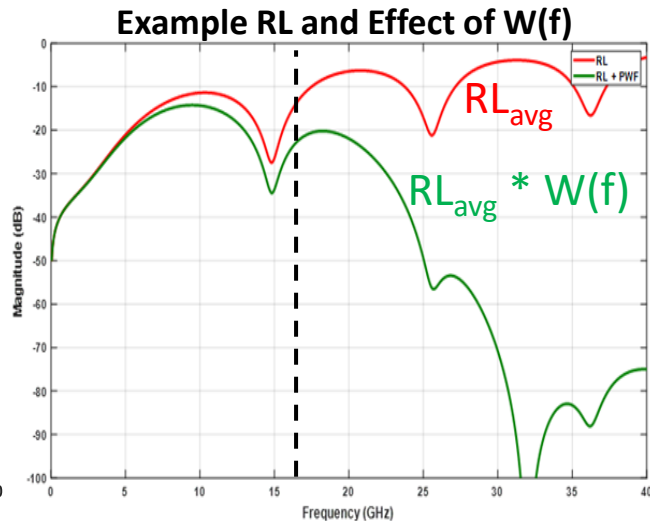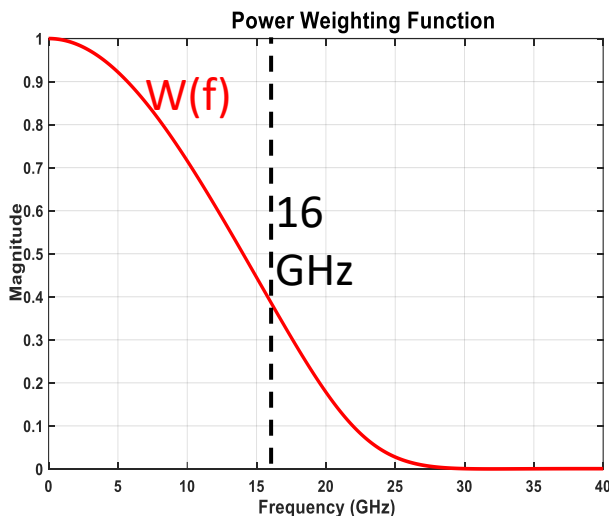
$$W(f_i) = sinc^2(f_i/f_b)\left(\frac{1}{(1 + (f_i/f_t)^4)}\right)\left(\frac{1}{(1 + (f_i/f_r)^8)}\right)$$

$$RL_{avg}(f_i) = (|RL_{11}(f_i)| + |RL_{22}(f_i)|)/2$$

$$iRL = dB\left(\sqrt{\frac{1}{N}\sum_{i=1}^{N} W(f_i) \, RL_{avg}^2(f_i)}\right)$$

May appear in CEM 6.0 and internal\external cable 5.0 and 6.0

PCI Express and Optics, Are We Ready?

Sam Kocsis

Amphenol

Evolution of Server Platforms
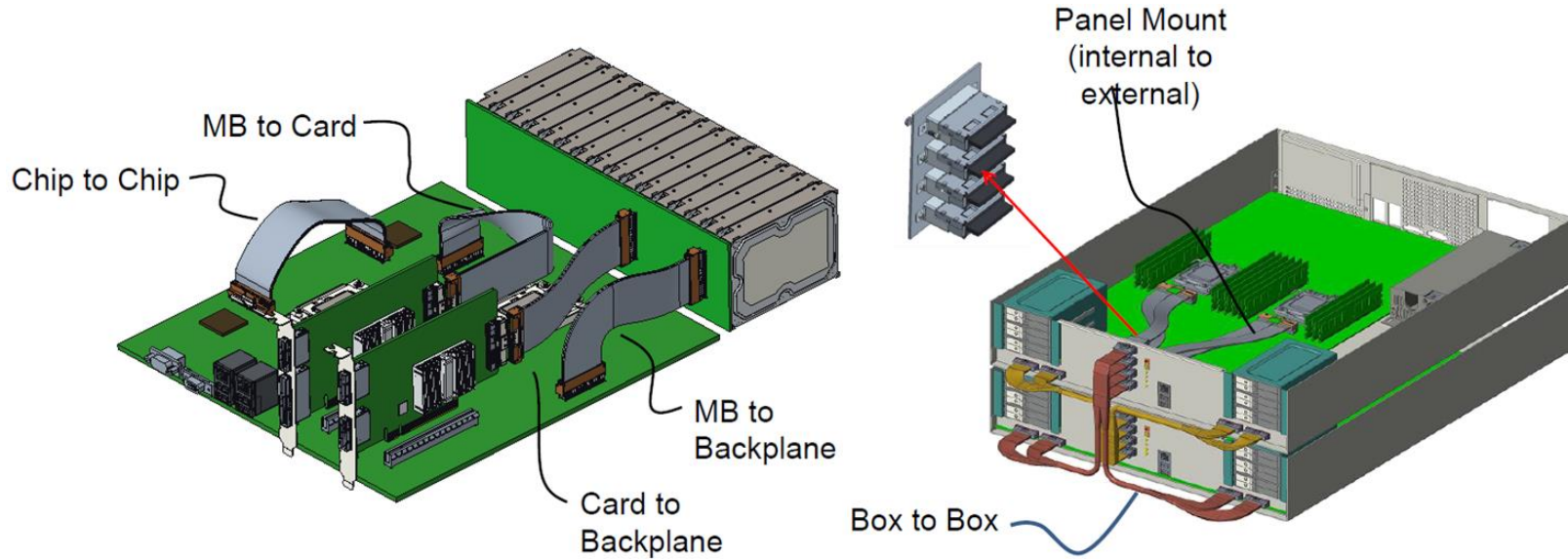
Increased system density, complexity, and demands for higher performance has resulted innovative copper interconnects and "cabled" solutions
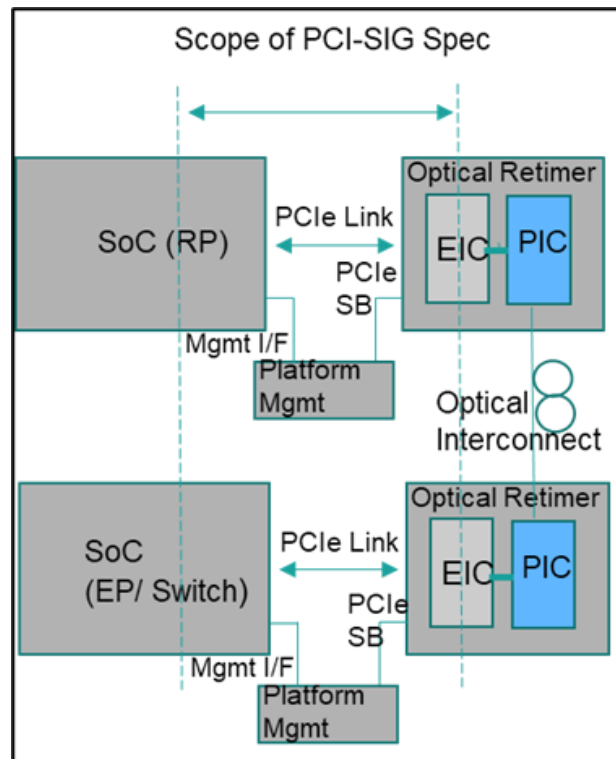
Trends in PCIe Interconnect

Server platforms trending towards modular designs

Disaggregation leads to *more* interconnect opportunities
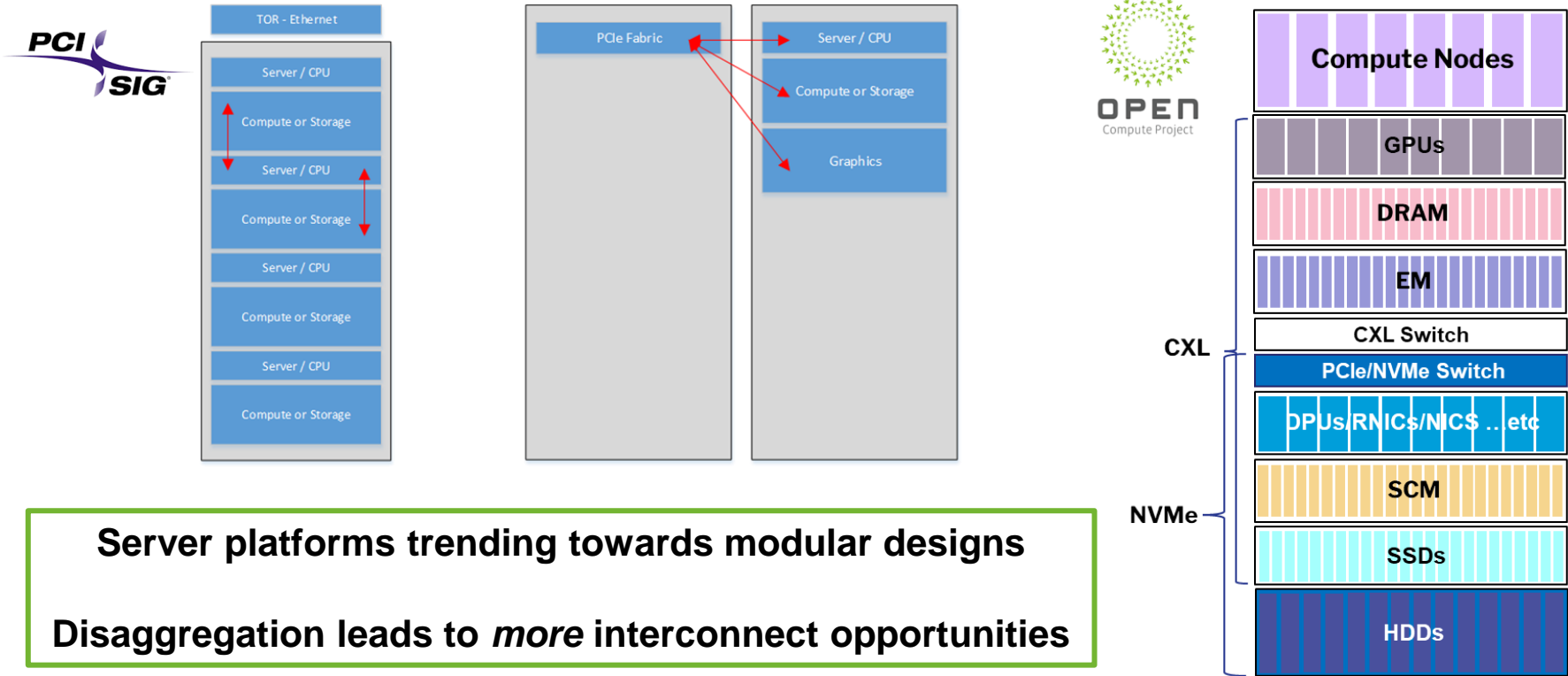
Convergence of Market Opportunities

Storage Applications
Replacing SAS/SATA systems

Pooled Memory Applications
CXL3.0

CPU-GPU Applications
Disaggregated Architectures

Networked Accelerators
Low-Latency Fabrics (EEI)
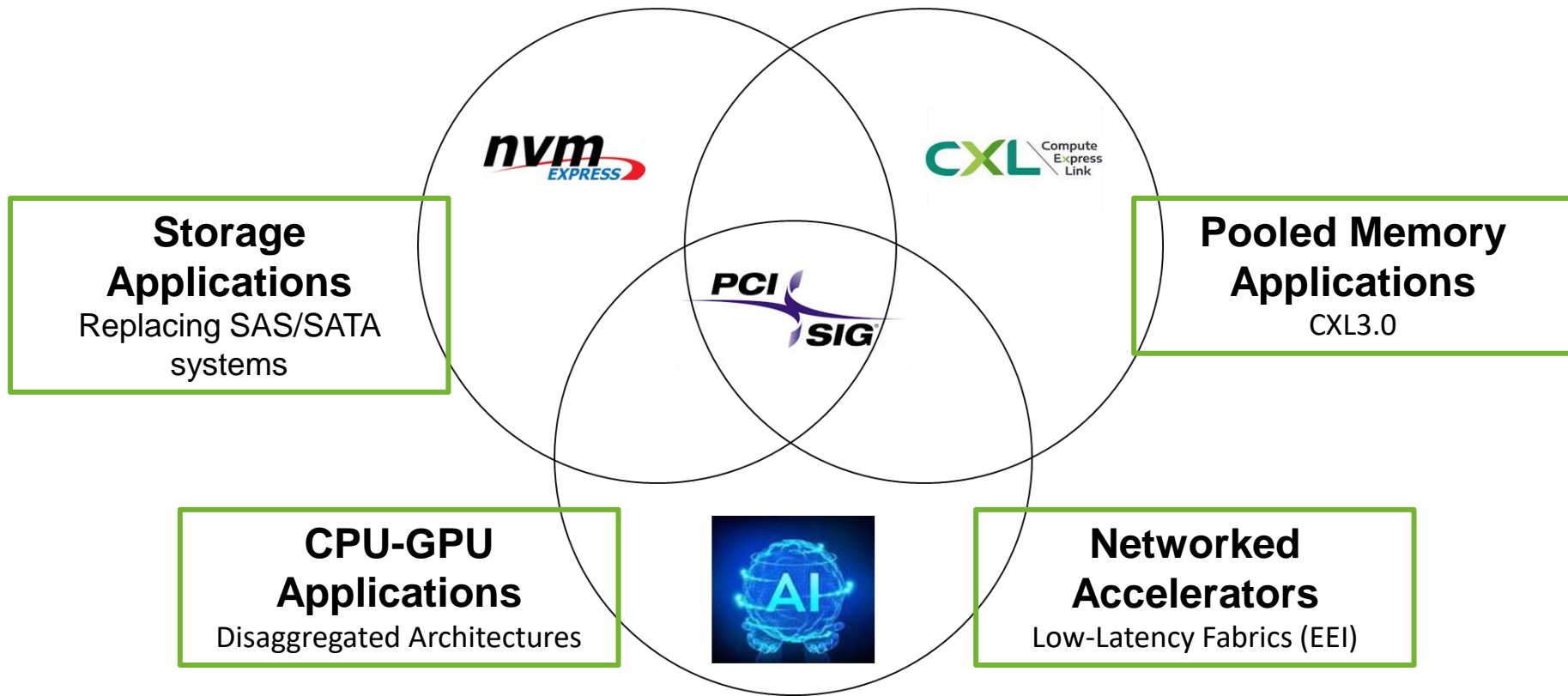
...One Giant Leap for the Industry

Optics

"August 2, 2023"

Scope of PCI-SIG Spec

SoC (RP) — PCIe Link — Optical Retimer (EIC / PIC)

PCIe SB

Mgmt I/F — Platform Mgmt

Optical Interconnect

SoC (EP/ Switch) — PCIe Link — Optical Retimer (EIC / PIC)

PCIe SB

Mgmt I/F — Platform Mgmt

Link Analysis and Topology Assessment

32dB

Example PCIe 6.0 Link, 64GT/s, 32dB electrical budget, die-to-die, no retimers, 1E-6 BER

1E-6
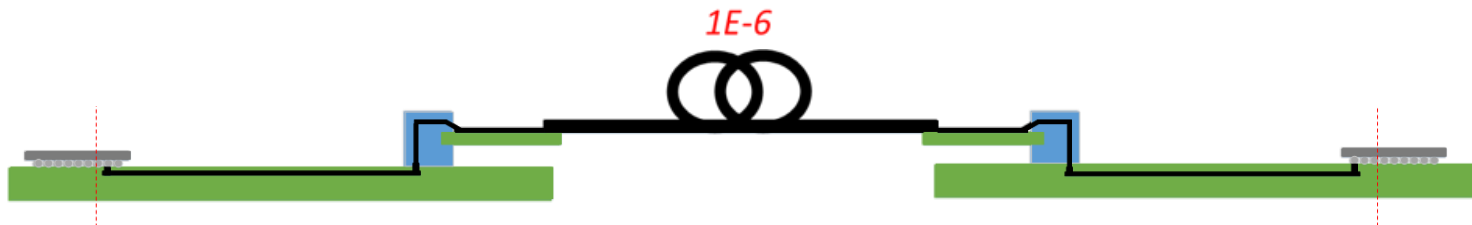
Topology Considerations
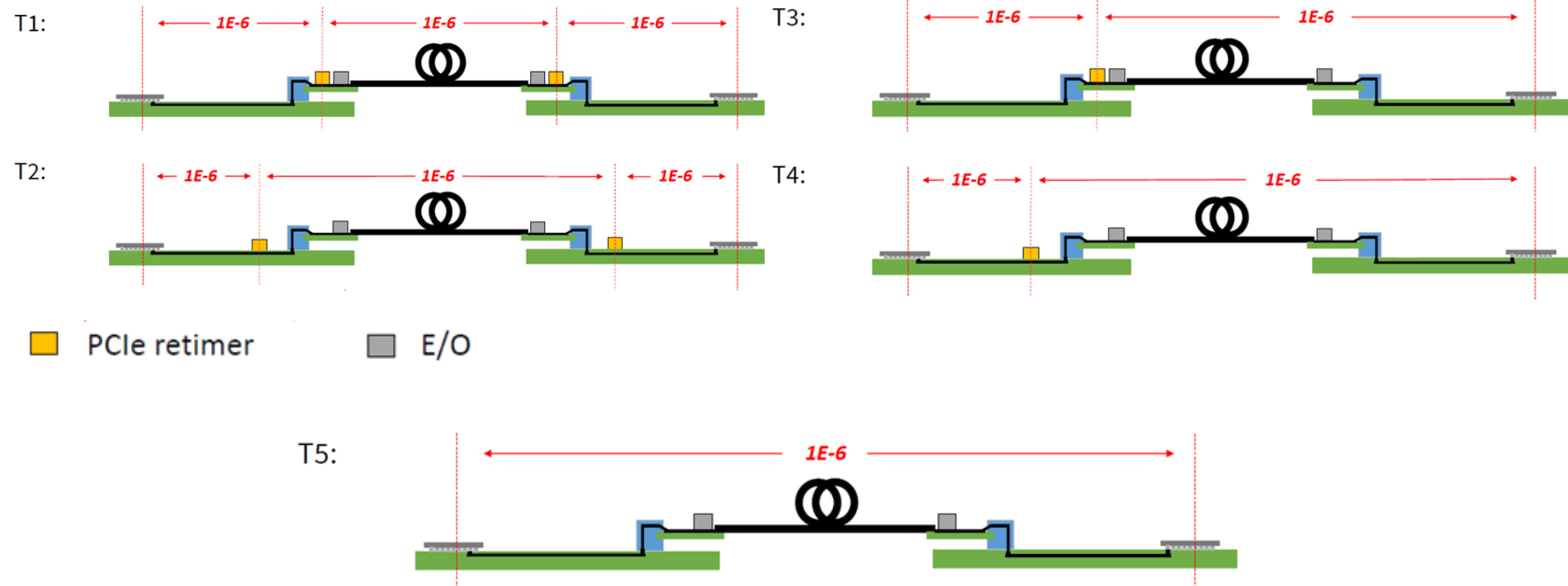
What's Next?
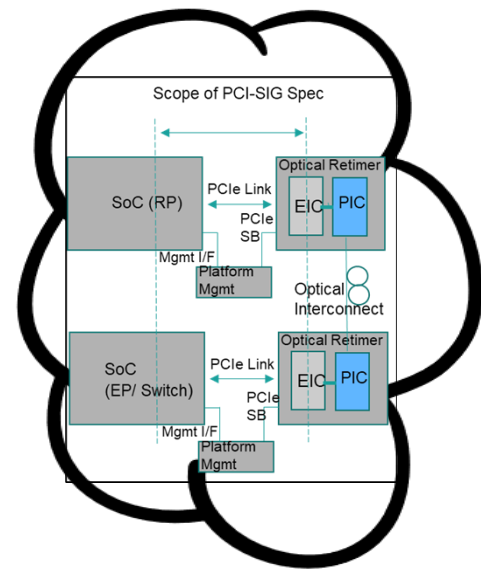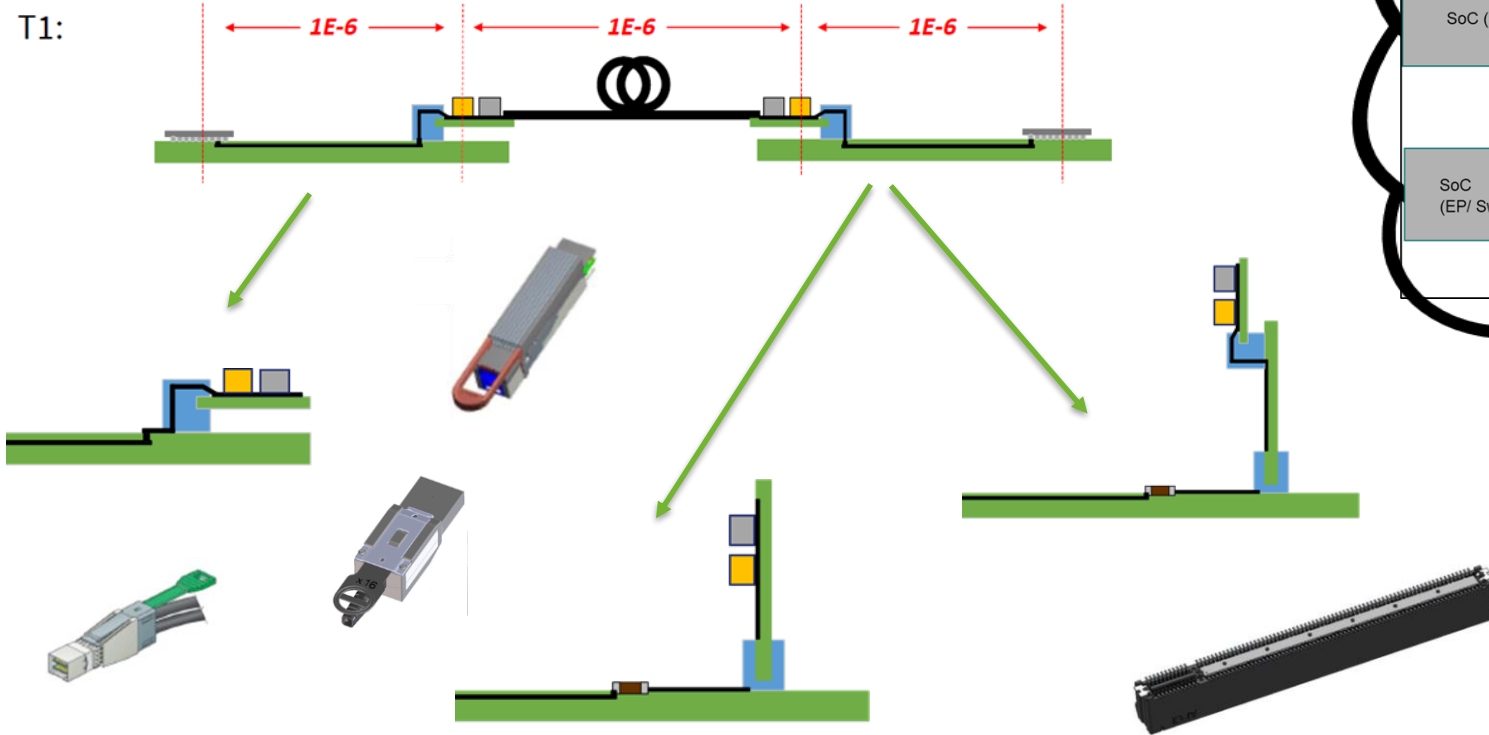
PCIe 7.0 64 Gbaud Transmitter Characterization

Rick Eads

Keysight Technologies

PCIe 7.0 Transmitter Measurements

- **Key Considerations at 64GBaud**
- **Channel Requirements**
- **Signal-to-Noise and Distortion Ratio (SNDR)**
- **Jitter Measurements**
- **RLM**

64GBaud PAM4

- Channel BW vs PCIe 6
  - 32GHz for PCIe 7, 16GHz for PCIe 6.

- TX Equalization
  - TX EQ using a 4-tap Finite Impulse Response filter used for 32GBaud, likely sufficient for 64GBaud

- RX Equalization
  - RX EQ for 32GBaud is a combination of CTLE + 16 Tap DFE
  - For 64 GBaud, more aggressive RXEQ will be required for the target channel

- Forward Error Correction (FEC)
  - Allows First Bit Error Ratio (FBER) of 1e-6 for 32GBaud, likely sufficient for 64GBaud
  - Link BER target (post FEC) remains 1e-12 for 64GBaud

- Legacy
  - Backward compatible with earlier generations of PCIe technology
  - CEM at 64GBaud -> Challenging
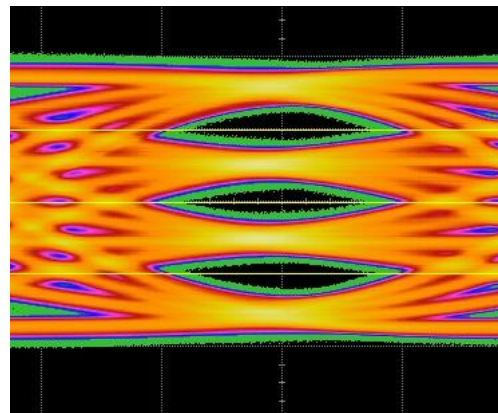
64GBaud PAM4 Signal

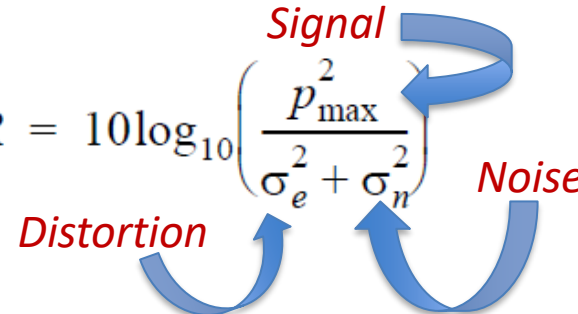# Channel Requirements

- Two types of PCIe Channel Targets
    - Client: ~25cm-35cm with 1 connector
    - Server: ~50cm with 2 connectors (2 retimers allowed)
- Concerns at 64GBaud
    - Insertion loss at 32GHz will benefit from new materials
    - CEM connector will be pushed (xtalk, SI improvements)
    - PAM4 TX Measurements will be challenging at the end of the channel (for workshop compliance)
    - Will likely see increasing use of cabled connections inc. optical

Client Use Case

Server Use Case

CEM Connector

Riser

Non-Root

AIC

AIC

Non-Root

Retimer

CEM Connector

Root Port

Motherboard
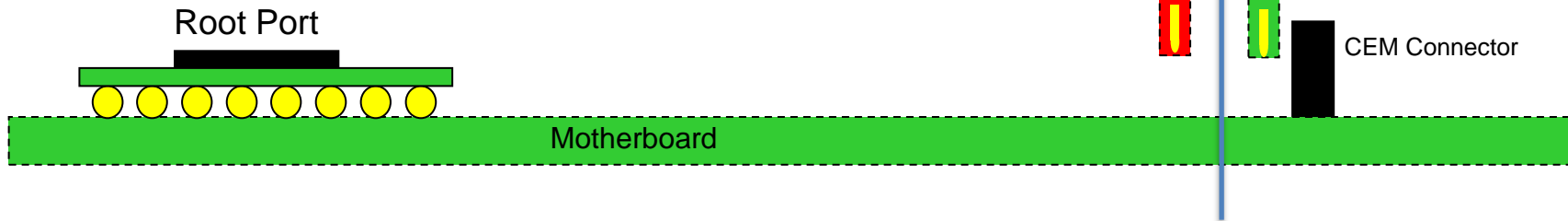
64GBaud PAM4 TX Measurements

- Signal to Noise and Distortion Ratio Measurement Improvements for 32GBaud

  - Pmax
    - Pmax2 is replaced with the sum of squares of linear fit pulse response p(k) and P0(k) for both even symbols and odd symbols in TX Compliance
    - More consistent with lossy channels than Pmax alone

  - Sigma-n
    - Measured on symbol #61, 250 repeats per level
    - Average computed for each level
    - Noise compensation applied

  - Sigma-e
    - Computed using linear fit pulse response for even and odd symbols
    - Only computed on PRBS sections of the TX Compliance pattern

$$SNDR = 10\log_{10}\left(\frac{p_{max}^2}{\sigma_e^2 + \sigma_n^2}\right)$$

Signal

Noise

*Distortion*

64GBaud PAM4 TX Measurements

- Lab Measurements at 64GBaud
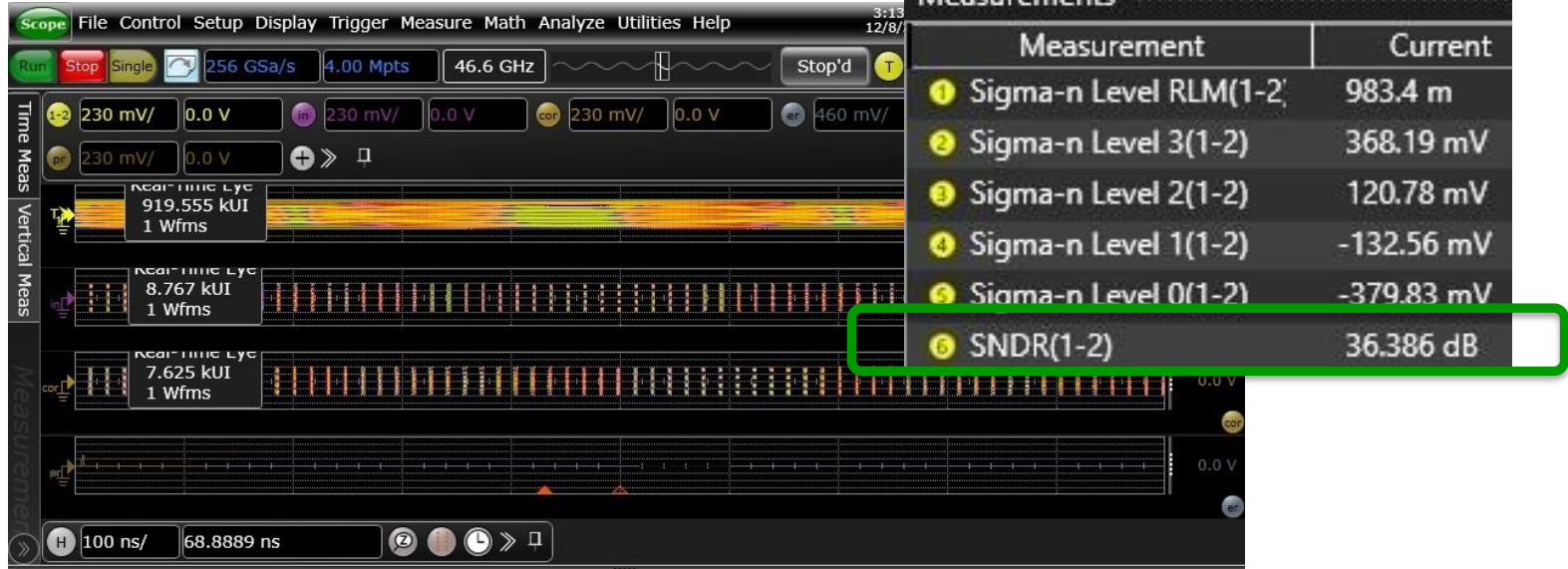
64GBaud PAM4 TX Jitter Measurements

- 48/12 edge Jitter Measurements @64GBaud

| Level Start	Level End	Random Jitter	TTX-UTJ 1e-6	J6U
3	0	100.1E-15	1.0E-12	985.8E-15
0	3	100.1E-15	976.8E-15	963.9E-15
2	0	137.7E-15	1.4E-12	1.4E-12
0	2	140.4E-15	1.4E-12	1.4E-12
3	1	123.9E-15	1.3E-12	1.3E-12
1	3	125.4E-15	1.3E-12	125.4E-15
1	0	270.6E-15	2.7E-12	2.7E-12
0	1	265.2E-15	2.7E-12	2.6E-12
2	1	268.5E-15	2.7E-12	2.6E-12
1	2	282.1E-15	2.9E-12	2.9E-12
3	2	225.3E-15	2.3E-12	2.2E-12
2	3	237.1E-15	2.4E-12	2.3E-12
	Average	189.7E-15	1.9E-12	1.8E-12
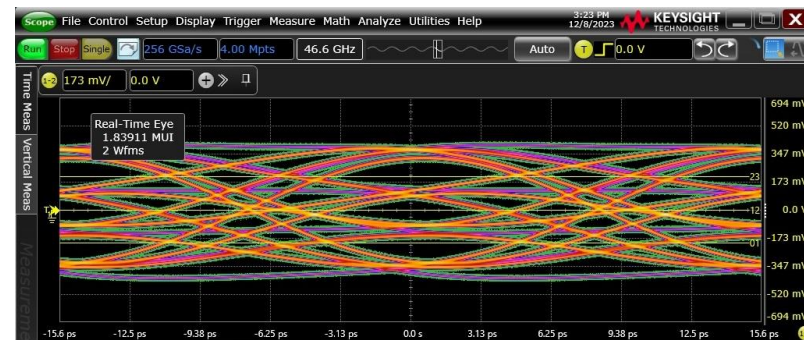
64GBaud PAM4 52UI Jitter Signal

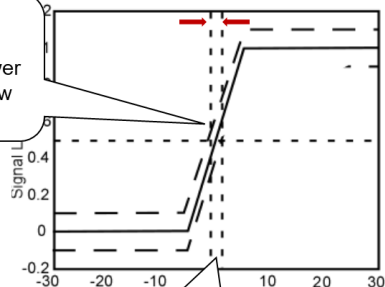Noise Compensation
Improves TTX-UTG by 26.6%
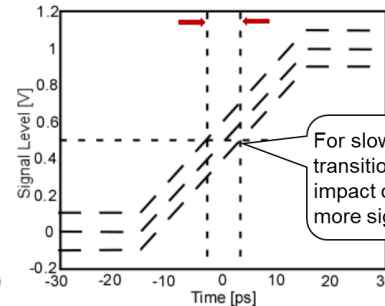TTX-UTJ = 1.4E-12s

64GBaud PAM4 TX Jitter Measurements

- PCIe PAM4 Jitter Measurements require Noise Compensation
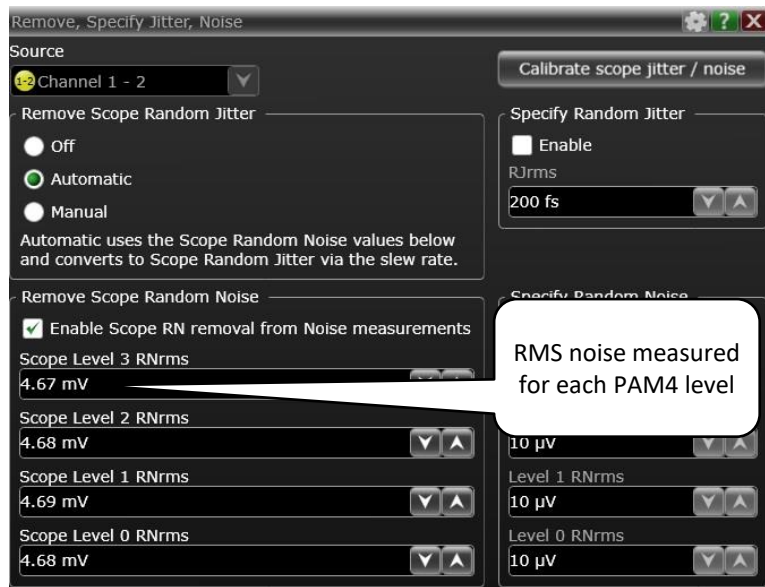
64GBaud TX Linearity

- Verify linear spacing of the PAM4 levels
- Benefits from robust clock data recovery
  - With SSC enabled, CDR average frequency changes
- VL is based on the Sigma-n Measurement Method @64GBaud

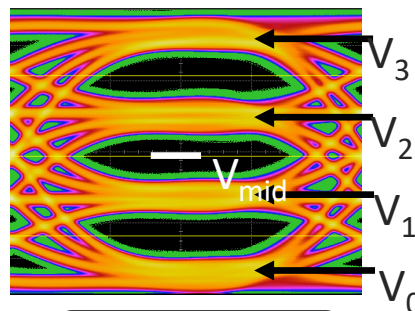$$V_L = \frac{\sum_{i=1}^{8} \mu_{L,i}}{8} \qquad \mu_{L,i} = \frac{1}{N_k}\sum_{k=1}^{N_k} V_{L,i,k}$$

$$V_{mid} = \left(V_0 + V_3\right) / 2$$

$$ES_1 = \left(V_1 - V_{mid}\right) / \left(V_0 - V_{mid}\right)$$

$$ES_2 = \left(V_2 - V_{mid}\right) / \left(V_3 - V_{mid}\right)$$
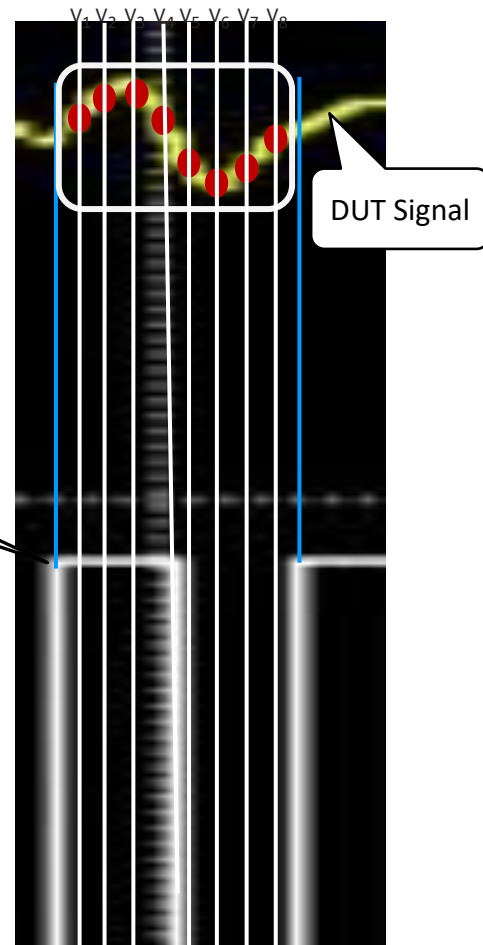
$$R_{LM} = min\left(\left(3 \times ES_1\right),\ \left(3 \times ES_2\right),\ \left(2 - 3 \times ES_1\right),\ \left(2 - 3 \times ES_2\right)\right)$$

Recovered Clock (rising edge) for Symbol 61

DUT Signal

Results (Measure All Edges)	
Measurements	
Measurement	Current
① Sigma-n Level RLM(1-2'	983.4 m
② Sigma-n Level 3(1-2)	368.19 mV
③ Sigma-n Level 2(1-2)	120.78 mV
④ Sigma-n Level 1(1-2)	-132.56 mV
⑤ Sigma-n Level 0(1-2)	-379.83 mV
⑥ SNDR(1-2)	36.386 dB

RLM>= 950.0m

PCIe 6.0 CEM & 7.0 Base Receiver Status

David Bouse

Tektronix Principal Technology Lead

PCIe 6.0 CEM & 7.0 Receiver Status

- **Receiver Validation Evolution**
- **For Factor Calibration – CEM 6.0**
- **128 GT/s (PAM4) Stressed Eye**
- **Form Factor Rx Test - CEM 6.0**
- **128 GT/s Eye Diagram**
- **Pulse Width Jitter**
- **64 GT/s Exhaustive Sweep**

Receiver Validation Evolution

|	PCIe 5.0	PCIe 6.0	128 GT/s (TBD)
Max data rate	32Gb/s	64GT/s (32Gbaud PAM4)	128GT/s (64Gbaud PAM4)
Channel loss range	-34 to -37dB @ 16GHz	-30 to -33dB @ 16GHz	~ 36dB @ 32GHz
Add-in card loss	9.5dB @ 16GHz	8.5dB @ 16GHz	~ 9dB @ 32GHz
Reference CTLE	4 poles, 2 zero, DC gain range -5 to -15dB	6 poles, 3 zero, DC gain range -5 to -15dB	6 poles, 3 zero, DC gain range 0 to -15dB (gain)
Reference DFE / FFE	3-tap DFE	16-tap DFE	~ 28-tap FFE & 1-tap DFE
Eye width (RX test)	9.375 ps	3.125 ps (top eye)	TBD
Eye height (RX test)	15 mV	6 mV (top eye)	TBD
Lane margining	Timing and voltage	Timing and voltage	Expected

Form Factor Calibration – CEM 6.0
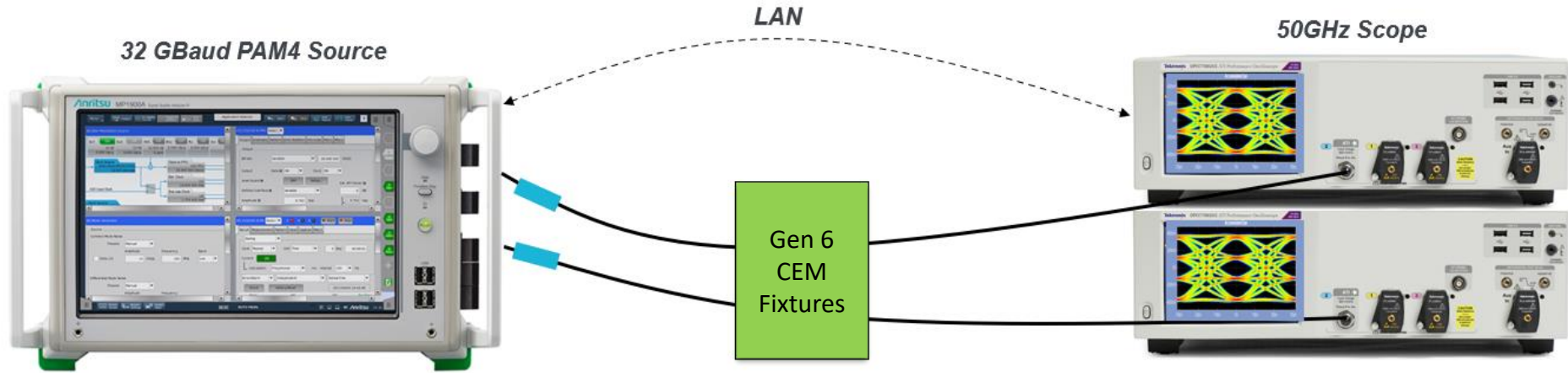
- **Source:** PAM4 PPG (Anritsu MP1900A)
  - 64 GT/s (32 GBaud PAM4) – <mark>Comp Pattern?</mark>
  - New Tx EQ Presets: <mark>Q0 – Q10 (optimal?)</mark>
- **Channel:** 30 to 33 dB @ 16 GHz
  - <mark>Gen6 CEM Fixtures (Prototypes Q3/Q4 2024?)</mark>

- **Scope:** Tektronix Real Time (DPO75004SX)
  - 50 GHz with 200 GS/s (package embedded)
- **Post Processing:** SigTest (waveform)
  - CTLE/DFE
  - Sj, Rj, & Crosstalk (DMI)
  - <mark>Scope Noise Compensation likely</mark>

128 GT/s (PAM4) Stressed Eye

LAN

70 GHz Scope

64 GBaud PAM4 Source

Gen 7 BASE Fixtures
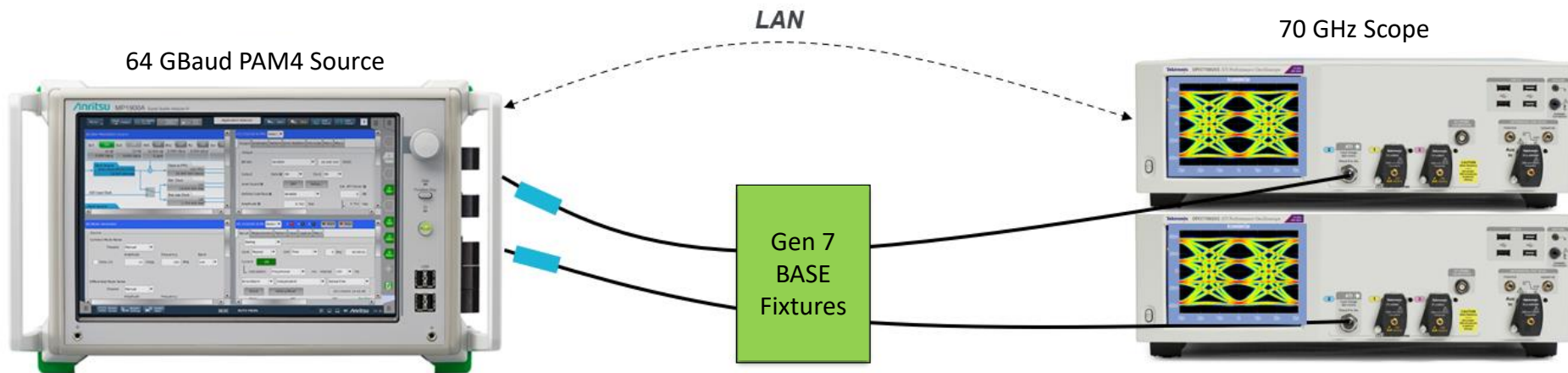
- **Source:** PAM4 PPG
  - 128 GT/s (64 GBaud PAM4) – Step Response
  - Tx EQ Presets: Gen6 Presets?
- **Channel:** ~ 36dB @ 32 GHz
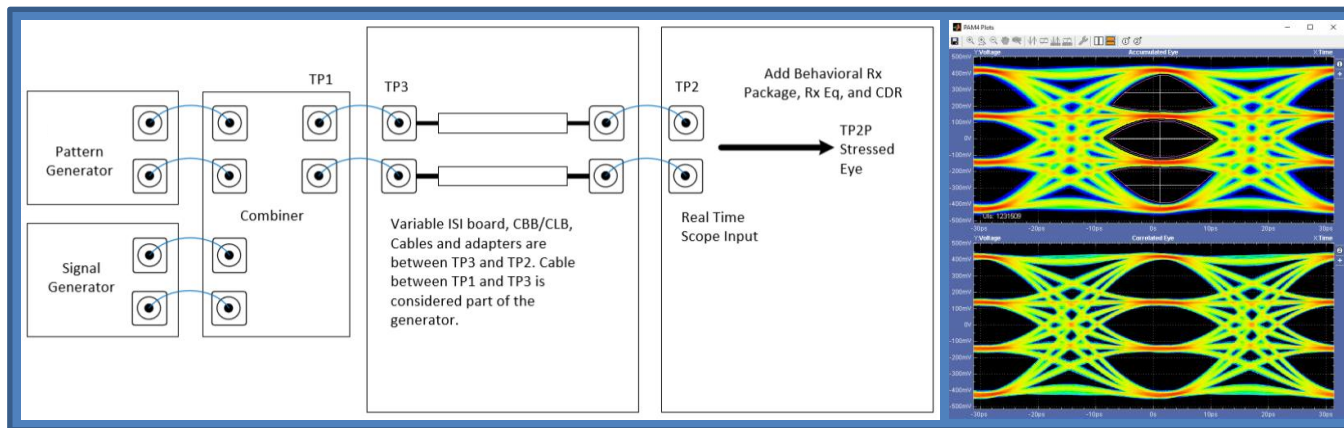 - Available Variable ISI boards

- **Scope:** Real Time Oscilloscope
  - ~65 to 70 GHz with lower BT filter expected
- **Post Processing:** Seasim 2.0.96
  - CTLE/FFE/DFE
  - Sj, Rj, & Crosstalk (DMI) to be explored
  - Instrument noise compensation likely

Form Factor Rx Test – CEM 6.0

- **Modified Compliance Pattern**
  - <mark>Adjacent lanes transmitting?</mark>
- **Tx Eq optimized during link training**
  - Loopback through Recovery
- **Spread Spectrum Clocking (SSC)**
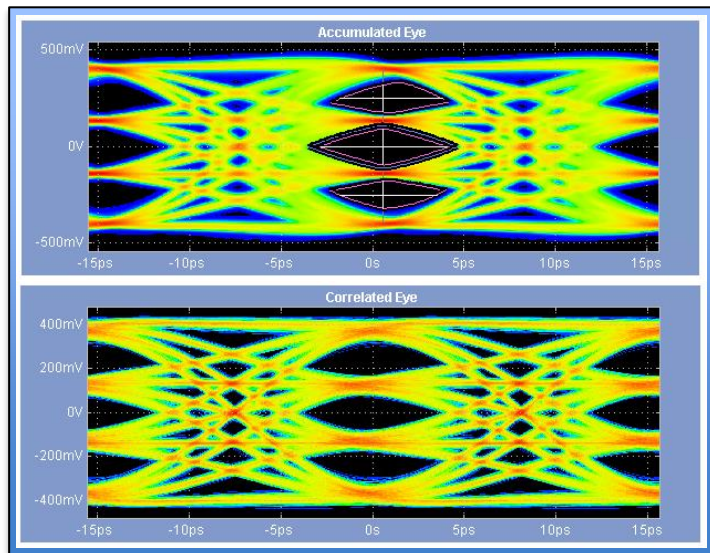 - <mark>SSC enabled? Disabled? Both cases?</mark>

- **Rx Link Equalization**
  - FBER @ E-6 (before FEC)
  - <mark>Test time TBD</mark>
- **210 MHz tone (Sj > 0.05UI)?**
- **Tx Link Equalization**
  - Extension devices (redrivers) likely needed
  - Analogous to 32 GT/s test

128 GT/s Eye Diagram (short channel)

- **Eye Height @ E-6**
  - Top: 154.9 mV
  - Mid: 207.3 mV
  - Bot: 156.9 mV
- **Eye Width @ E-6**
  - Top: 5.371 ps
  - Mid: 6.836 ps
  - Bot: 5.225 ps
- Source: 64+ GBaud Capable Tx
  - Tx Preset: Q0 (disabled)
  - Pattern: Gen6 Comp
- Scope BW: 70GHz with 4th Order BT @ 46.6GHz
- Analysis Tool: PAMJET (waveform based)
  - Rx EQ: 28 tap FFE / 1 tap DFE
  - De-embedding: Disabled
  - Noise Comp: Enabled

| Eye	Thresh	Offset	TJ@-5	TJ@-10	TJ@-15	RJ(d-d)	DJ(d-d)	H_eye	V_eye
Upper	266.5mV	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	5.371ps	154.9mV
Middle	-2.525mV	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	6.836ps	207.3mV
Lower	-268.3mV	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	5.225ps	156.9mV

Pulse Width Jitter (TP3)

- **Pulse Width Jitter** – edge to edge jitter on 1UI wide pulses
  - Tx parameter and used to characterize BERTs (TP3)
- Source: 64+ GBaud Capable Tx
  - Tx Preset: Q0 (disabled)
  - Pattern: 0303 (PWj Measurement)
- Analysis Tool: PAMJET (waveform based) – noise comp enabled
  - CDR: Type 2 PLL (10 MHz)
  - BT Filter: 4th Order / 46.6 GHz
  - Rx EQ: CTLE Rev 0.5 Optimized @ 11dB (AC/DC Gain)
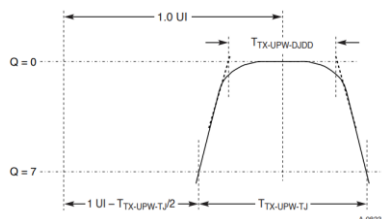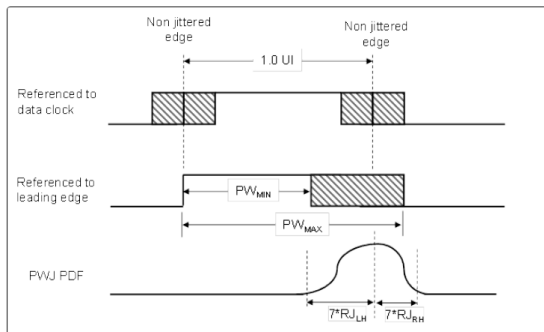
CTLE Rev 0.5 (dB)	PWJ Tj (ps)	PWJ Dj_dd (fs)	PWj Rj RMS (fs)
Disabled	1.199	257.2	126.9
0	1.096	127.8	99.0
1	1.111	164.3	96.8
2	1.108	184.4	94.4
3	1.103	197.7	92.5
4	1.079	185.5	91.4
5	1.042	167.3	89.5
6	1.022	158.7	88.3
7	0.983	137.9	86.3
8	0.967	129.9	85.6
9	0.959	131.4	84.6
10	0.954	133.5	83.9
11	0.954	135.1	83.7
12	0.956	137.2	83.7
13	0.958	143.2	83.3
14	0.963	150.4	83.0
15	0.983	170.5	83.0

64 GT/s Exhaustive Sweep (33.4dB)
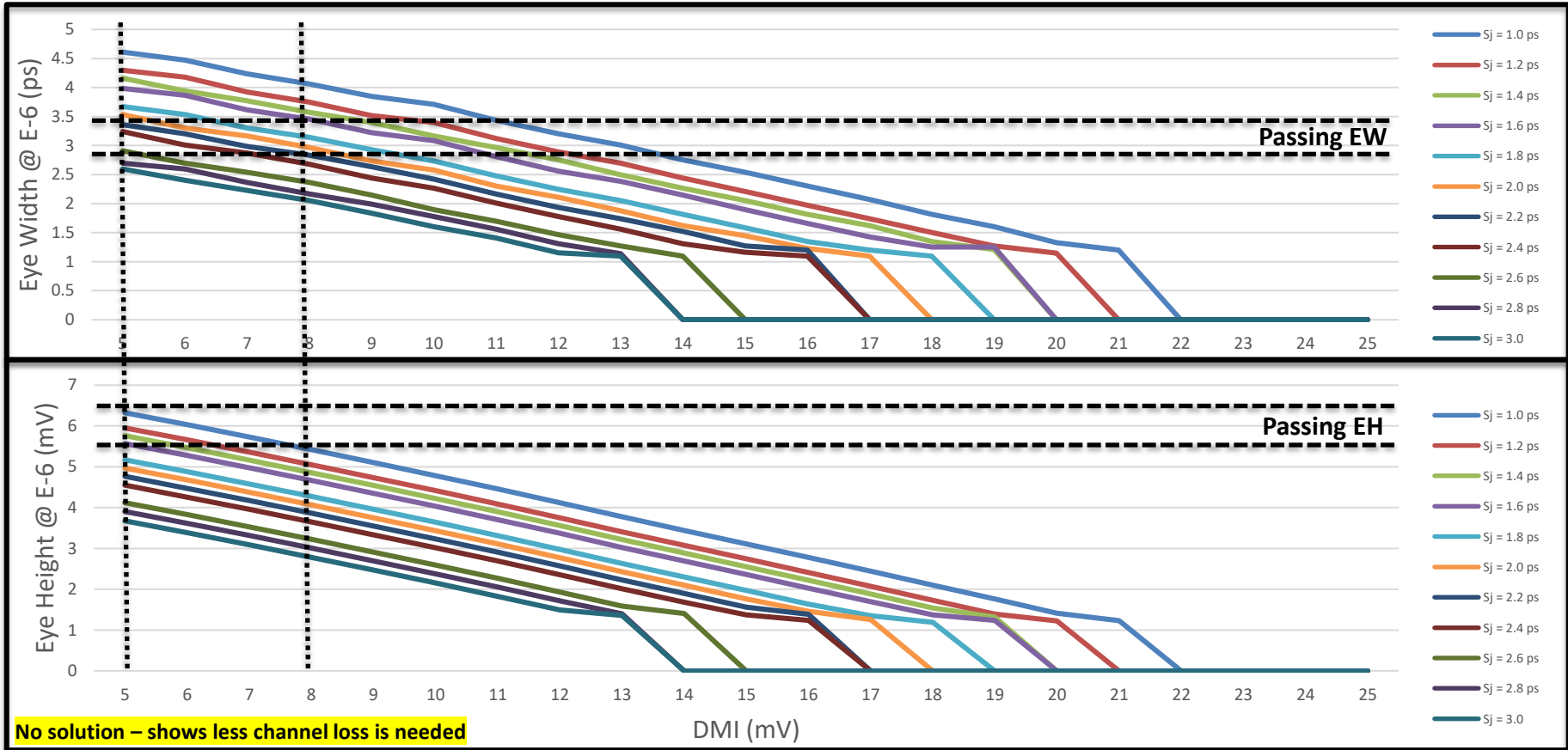
No solution – shows less channel loss is needed

PCIe 6.0 System Consideration facilitating Innovation in 128 Gbps Capable Devices
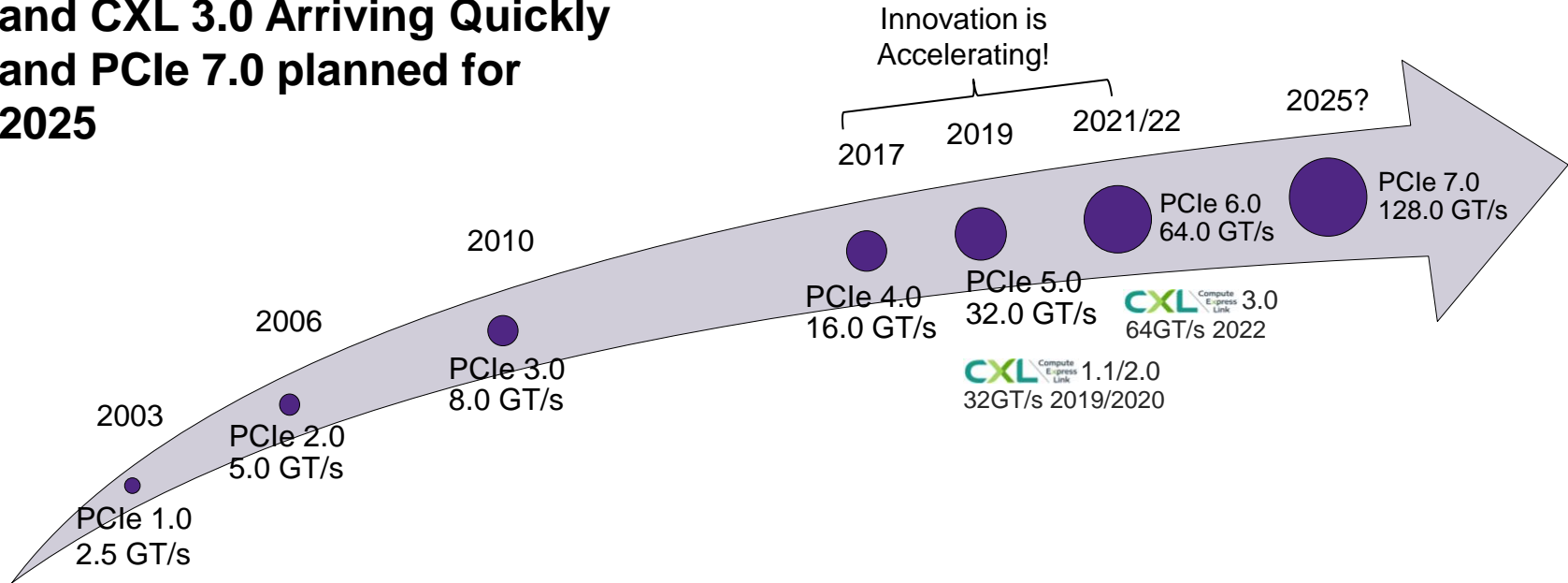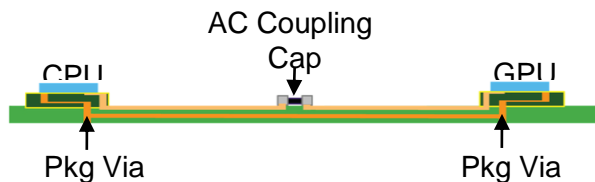
Madhumita Sanyal

Synopsys Inc

PCI Express Specifications are Accelerating

- **Innovation is Accelerating since PCIe 3.0, with PCIe 6.0 and CXL 3.0 Arriving Quickly and PCIe 7.0 planned for 2025**
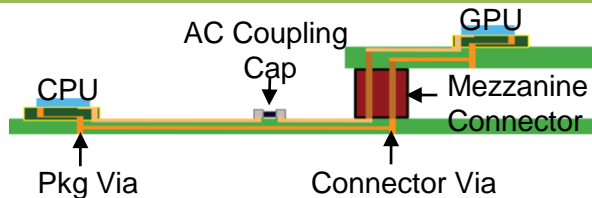
Innovation is Accelerating!

2017   2019   2021/22   2025?

2003

2006

2010

PCIe 1.0
2.5 GT/s

PCIe 2.0
5.0 GT/s

PCIe 3.0
8.0 GT/s

PCIe 4.0
16.0 GT/s

PCIe 5.0
32.0 GT/s

CXL Compute Express Link 1.1/2.0
32GT/s 2019/2020

CXL Compute Express Link 3.0
64GT/s 2022

PCIe 6.0
64.0 GT/s

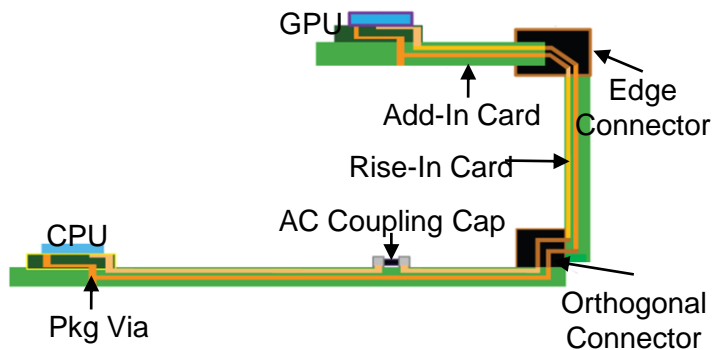PCIe 7.0
128.0 GT/s

PCIe 6.0 & PCIe 7.0 Challenging Channels

Chip-to-Chip No Connector
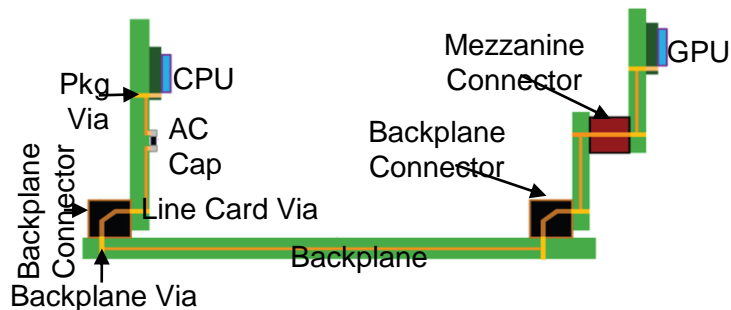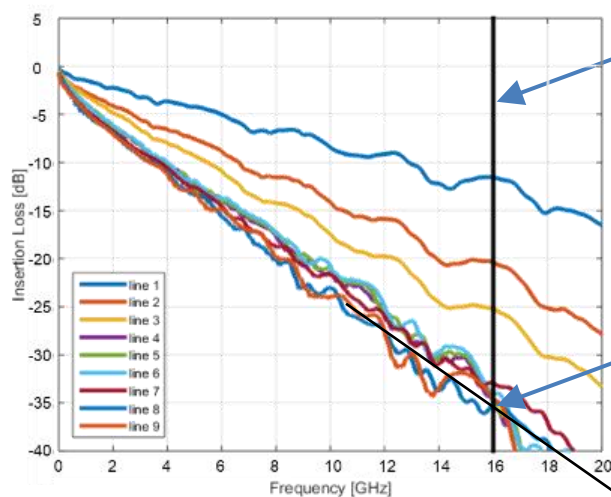
1 Mezzanine Connector

Riser & Add-in card Connectors

Backplane with 2+ Connectors

The Challenge for PCIe 7.0

Example 5.0/6.0 Channels with a Range of Channel Losses & Ripple (ILD) Values

16GHz Nyquist for
32GT/s data rate (Gen5)

PCIe 7.0 @ 128GT/s
- Still using PAM4
- Nyquist goes to 32GHz

A reliable 32G Link needs to
work on worst case channels

32GHz Nyquist for 128GT/s data rate
-70dB Loss = Virtually Impossible!
(1V becomes 0.45mV)

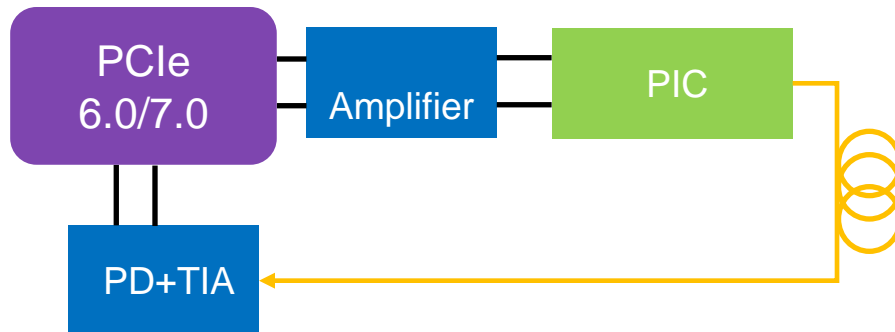# PCIe Technology Over DAC Cables & Optics

Industry Efforts for PCIe External Connectivity

- PCISIG Electrical Working Group (EWG) defines PCIe Base and Cable specifications for Gen 5/6/7
- PCISIG Cable Working Group defines PCIe Cable specification historically focused on MiniSAS HD
- PCISIG Optical Working Group (OWG) is a newly formed group
- SNIA Small Form Factor Technology Affiliate Technical Working Group
  - SFF-TA-1032 defines the mechanical FFs of PCIe External Connectors & Cables
  - INF-TA-1003 (CDFP 400G Ethernet MSA)
- OCP Extended Connectivity work stream
- Supporting Standards:
  - OIF – Common Management Interface Specification (CMIS)
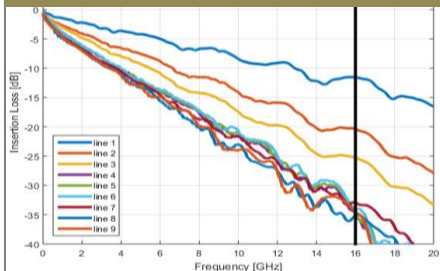 - SFF-8024 : SFF Module Management Reference CodeTables

PCI SIG

SNIA

OPEN Compute Project®

- End-to-end simulation : Check eye diagram and compliance points
- Sim to Silicon Correlation

Non-Retimed Interface

PCIe 6.0/7.0 — Amplifier — PIC

PD+TIA

DESIGNCON 2024
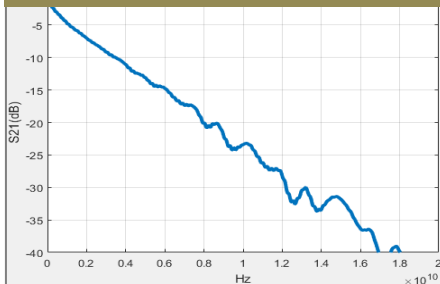WHERE THE CHIP MEETS THE BOARD

informa markets
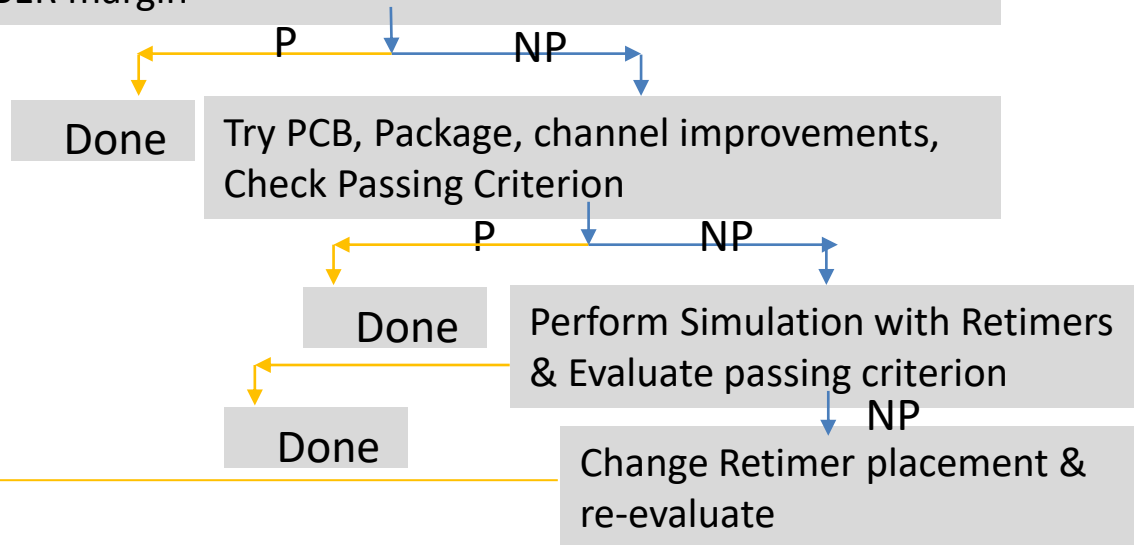
End-to-End Simulation Methodology

PHY Needs Optimization for Long/Short Channels
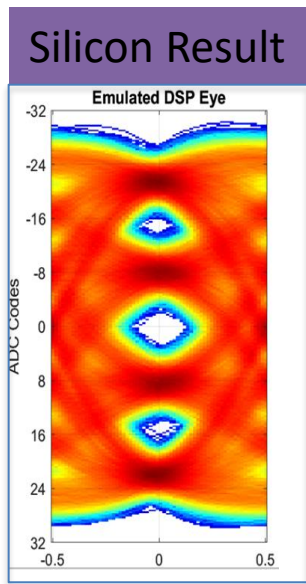
>36dB Channel Loss for Worse Case Channel with Margins

End-to-end Simulation to determine PCIe 6.0/7.0 Channel Budget < 33dB and BER margin

P   NP

Done

Try PCB, Package, channel improvements, Check Passing Criterion

P   NP

Done

Perform Simulation with Retimers & Evaluate passing criterion

NP

Done

Change Retimer placement & re-evaluate

Sim to Silicon correlation on PCIe 6.0/PCIe 7.0 Over Optics

(i) TX IBIS-AMI model -> TX package -> Replica board + Cables -> Reference RX model
(ii) Reference TX model -> Interconnect channel + Replica board -> RX package -> RX IBIS-AMI model
(iii) IBIS-AMI sim at nominal, low-gain and high-gain corners
(iv) Correlate with Silicon measured Optical/Electrical Eye and BER

Silicon Result

Emulated DSP Eye

4-level stimulus   FFE

Tx DLL/.so | Tx analog | Electrical Or Optical channel | Rx analog | Rx DLL/.so

AGC
CTLE/FFE
DFE
CDR

clock times

Thank you!

—

QUESTIONS?