Welcome to

DESIGNCON® 2024

WHERE THE CHIP MEETS THE BOARD

Conference
January 30 – February 1, 2024

Expo
January 31 – February 1, 2024

Santa Clara Convention Center

Survey on Correlation & Simulation Methodologies for PCB Structures Through 67GHz

Robert Branson, (Samtec)
Greylan Smoak, (Samtec)

Scott McMorrow (Samtec), Steve Krooswyk (Samtec)

SPEAKERS

Robert Branson

Signal Integrity Engineer, Samtec
Robert.Branson@samtec.com

Robert Branson has been a Signal Integrity Engineer at Samtec for the past 4 years. He has worked in connector/PCB design, development, and correlation for numerous Samtec products, and has experience in using 3D modelling software for the analysis of connectors.

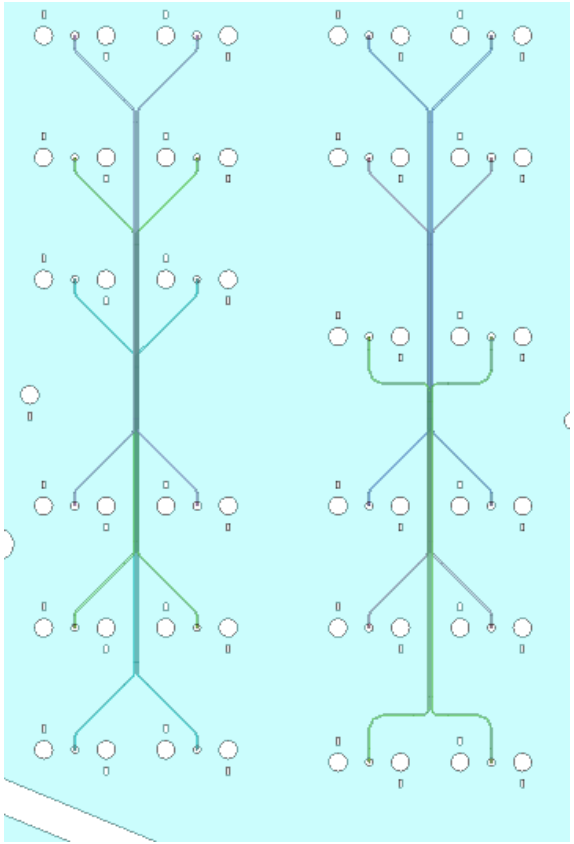
Greylan Smoak

Signal Integrity Engineer, Samtec
Greylan.Smoak@samtec.com

Greylan Smoak has been a Signal Integrity Engineer at Samtec for 3 years. He received his Master of Engineering in Electrical Engineering from the University of South Carolina in 2023. He has experience in connector/PCB design, modelling and correlation through many different projects at Samtec.

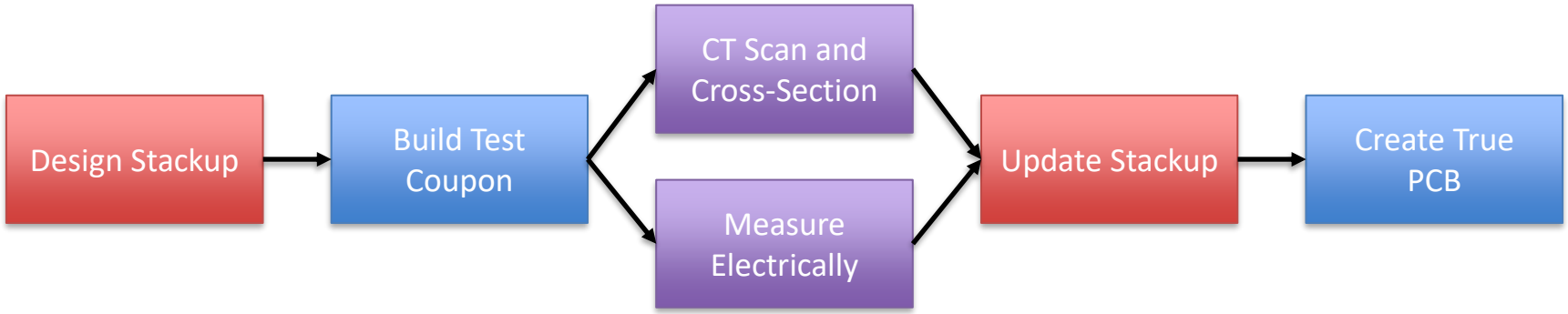
Introduction

- **Successful PCB design relies on simulation accuracy**
  - More accurate simulations lead to better optimization
  - Inaccurate simulations waste engineering hours and money
- **The end goal is to build a model that will correlate to measurements**
  - This is always a matter of degrees, with no model being perfect
- **Numerous DesignCon papers focus on PCB correlation techniques**
  - Simulation accuracy is often a key component
  - There is always ongoing research in this field



Introduction

- **Many correlation techniques require a test coupon**
  - This requires building and designing a separate PCB
  - Considerable engineering hours and funds must go into this process
- **Our survey will focus on techniques that don't need a test coupon**
  - This means the design process only has to be completed once



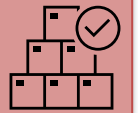
Introduction

Correlation depends on the three categories below:

Manufacturing Information

Basic PCB Information

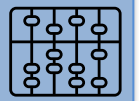
- Stackup
- Drill Size
- Trace Dimensions



Simulation Methodology

Modelling Techniques

- Surface Roughness
- Dielectric Modelling
- Etching



Manufacturing Variation

Fabrication Tolerances

- Backdrill Depth
- Impedance Variation
- Misregistration

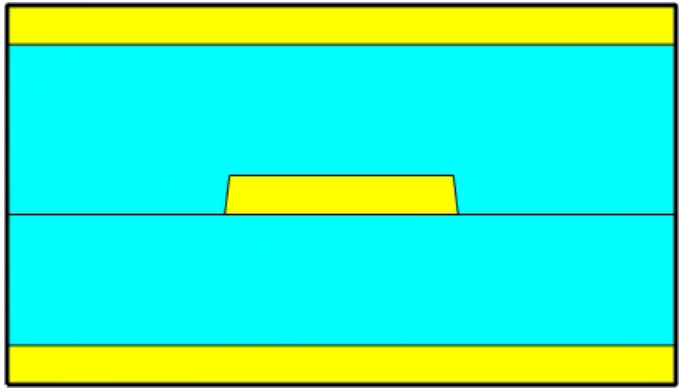
Simulation Methodology Characteristics

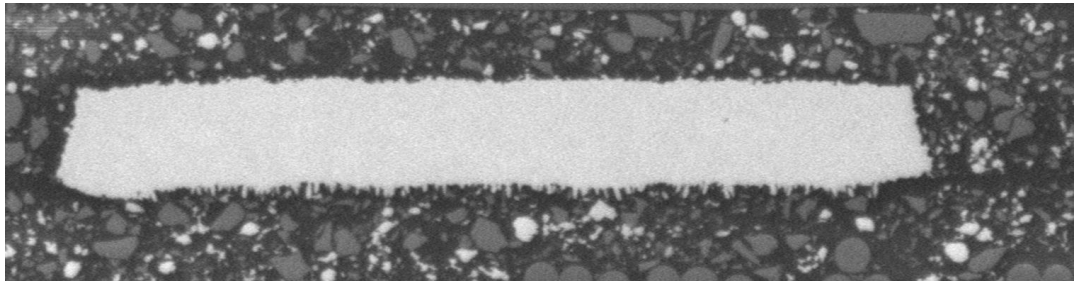
- **Characteristics are the individual simulation methodology topics**
  - They are intended to represent everything a SI engineer needs to consider in this category
- **This survey will look at each characteristics**
  - What is it?
  - How is it simulated?
- **The characteristics are split into two categories**
  - Material Characteristics
  - Environmental Characteristics

Material Characteristics

Surface Roughness

- **Describes height imperfections occurring on surface of trace**
- **A mathematical model is used in solvers to approximate**
  - There are numerous techniques for analyzing this
- **Different surface roughness profiles for drum/matte**
  - Matte is core-facing
  - Drum is prepreg-facing





Gore, Brandon. “Measurement Evaluation of PCB Electrical Performance 200 Gb/s PAM 4,” IEEE October 2022 Series of Electronic Meetings, IEEE P802.3df.

Surface Roughness Methodologies

- **Methods that can be applied:**
  - No surface Roughness
  - Surface Roughness through Dk/Df
  - Common Huray
  - Modified High-Frequency Huray

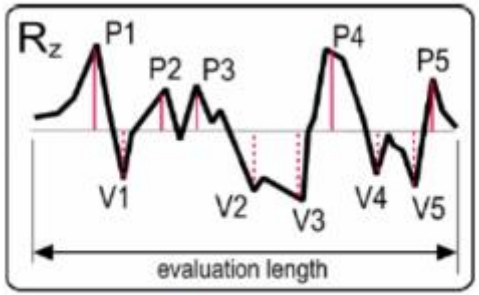


Figure 2 – Rz

- **Surface roughness can be applied separately to trace:**
  - Top
  - Sides
  - Bottom

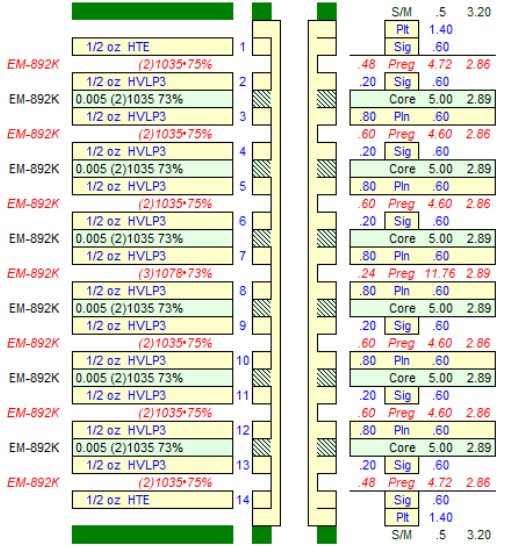
$$r \approx 0.06R_z$$

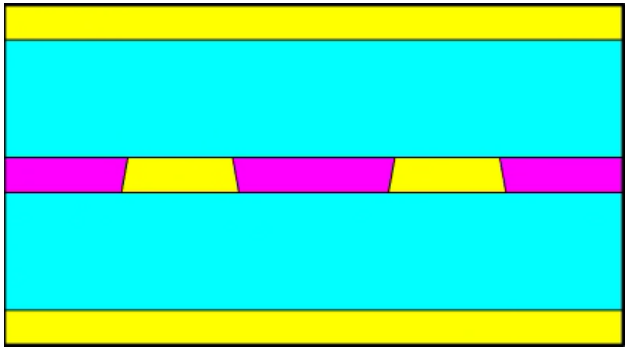
$$RF1 = 1 + \frac{3}{2}\left(\frac{N \cdot 4\pi r^2}{A_{flat}}\right) = 1 + \frac{3}{2}\left(\frac{14 \cdot 4\pi (r)^2}{36(r)^2}\right) \approx 8.33$$

J. A. Marshall, “A. F. Horn III, C. J. Caisse, et al., “Measuring Copper Surface Roughness for High Speed Applications”, IPC Proceedings.
B. Simonovich, “PCB Interconnect Modeling Demystified”. DesignCon 2019, Proceedings, Santa Clara, CA, 2019.

Dielectric Modelling

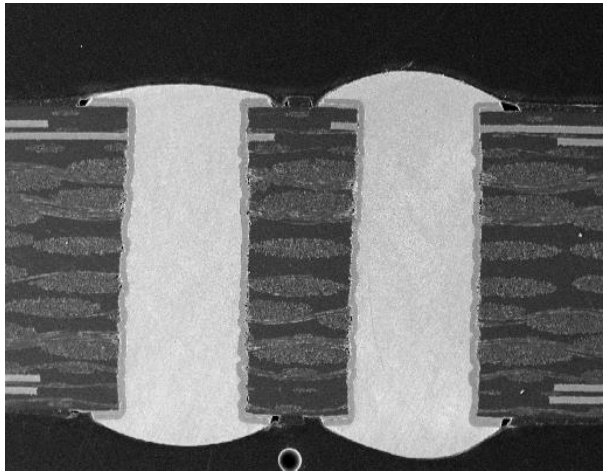
- **Involves the translation of a stackup to a 3D model**
- **There are many advanced techniques for known stackups**
  - However these can be panel/stackup specific
- **The most common approach is the Djordevic-Sarkar model**

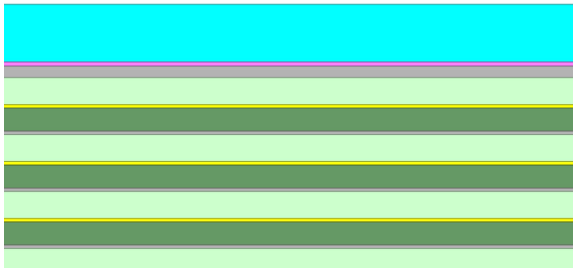




Dielectric Modelling Methodologies

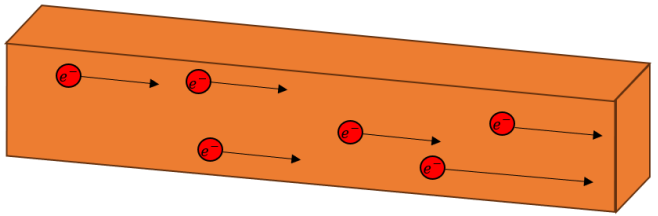
- **Methods that can be applied:**
  - Solid DK
  - Layer-by-Layer
  - Anisotropic
  - Signal Layer Resin Pocket
  - Dielectric Layers Resin-Glass-Resin
  - Dielectric with Implemented Surface Roughness





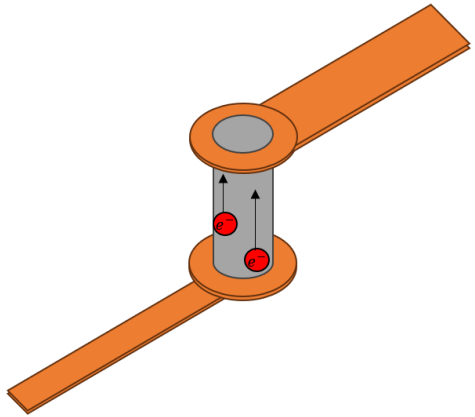
Conductivity

- **Fundamental Electric Property**
- **Conductor Conductivity varies in PCBs**
  - Not strictly that of 100% IACS copper
    - $5.8 * 10^7 (\frac{S}{m})$
- **Input into solver in S/m**
  - Alternatively, as Resistivity Ohm-m



Via conductivity

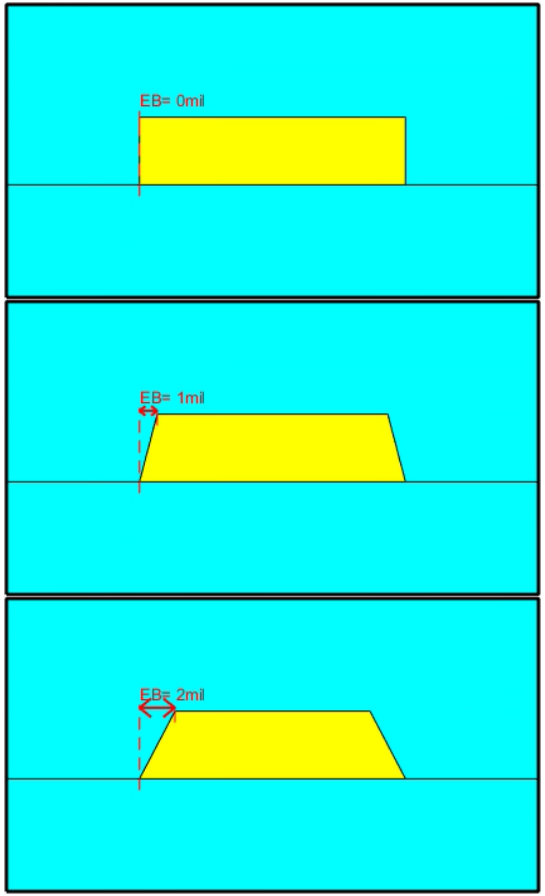
- **Fundamental Electric Property**
  - Not as well studied in vias
- **Electrodeposited in PCBs**
  - Likely not the same conductivity as copper foil
  - Not held to the same standard
- **Input into solver in S/m separately from foil**



Etching

- **Relates the process of removing unnecessary copper**
  - Done by the PCB fabricator
- **Controlled impedance vs non-impedance-controlled trace**
  - Determines whether fabricator has impedance tolerance
- **Measured with either etch factor or etch-back generally**

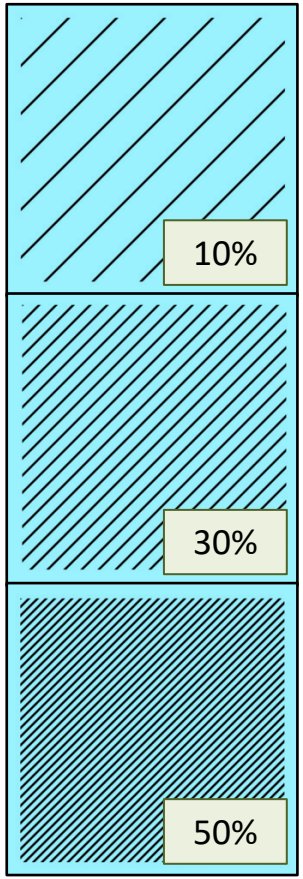
$$EF = \frac{2 * Thickness}{TW_{Bottom} - TW_{Top}}$$



Copper Utilization

- **Adjustments to prepreg dielectric height based on percentage copper on signal layer**
  - Volumetric equation
- **Dielectric height must be modified in solver**
  - Only affects prepreg traditionally

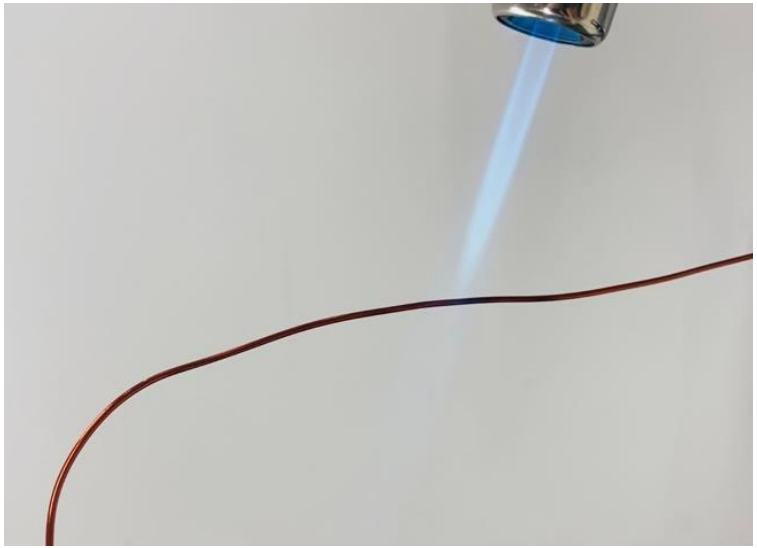
$$Thickness = Nominal\ Thickness - Foil\ Thickness * \left(1 - \frac{Copper\ Utilization\ \%}{100}\right)$$



Environmental Characteristics

Copper Temperature

- **Temperature dependence has been calculated, verified and understood**
  - $Conductivity = 5.8 \times 10^7 * \left(1 - \left(.00386 * (T - 20)\right)\right)$
- **Not uniform across PCBs**
- **Conductivity dependence can be built into solver**
  - Although most solvers assume uniform temperature across PCB



Dielectric Temperature

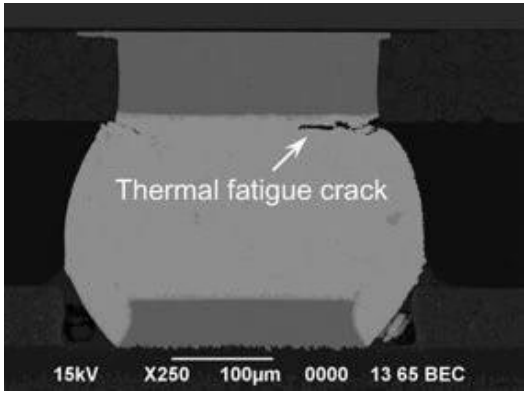
- **Temperature dependence less studied**
  - Has been shown to effect both loss tangent and dielectric constant
  - Greater impact on loss tangent
- **Dielectric dependence can be built directly into properties of dielectric material**

Humidity

- **Humidity impact on PCB not well understood**
  - Has been shown to effect both loss tangent and dielectric constant
  - In some cases, no change at all
- **Difficult to get accurate measurements**
  - PCB absorption takes a long period of time
  - Absorption likely varies across dielectrics
  - Must have well controlled environment
  - Humidity and temperature are highly related
- **Humidity dependence can be built directly into properties of the dielectric**

Lifespan

- **Relates to the degradation of the PCB over time**
  - Comes about as a result of time and heat cycling
  - Generally approximated through repeated heat cycling
- **Two types**
  - Destructive
    - *Can cause opens*
  - Dielectric decay
    - *Dielectric properties becoming worse over time*
    - *Either from air pockets or melting/settling within laminate*

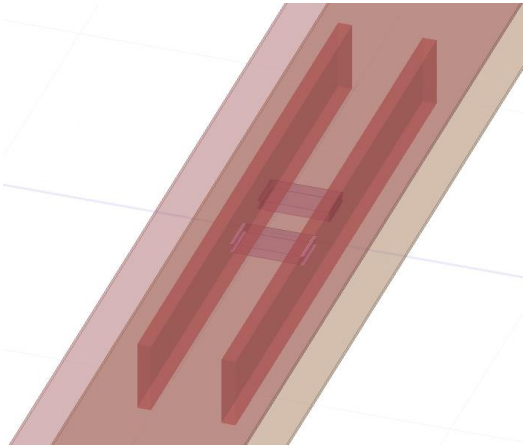


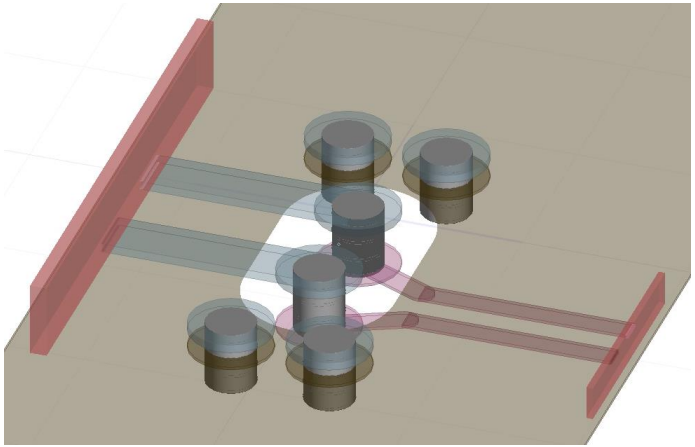
Morgan, Kelly. "Thermal Cycling Failure in Electronics." *ANSYS*, 13 July 2022.

Simulation/Measurement Analysis

DOE of Characteristics

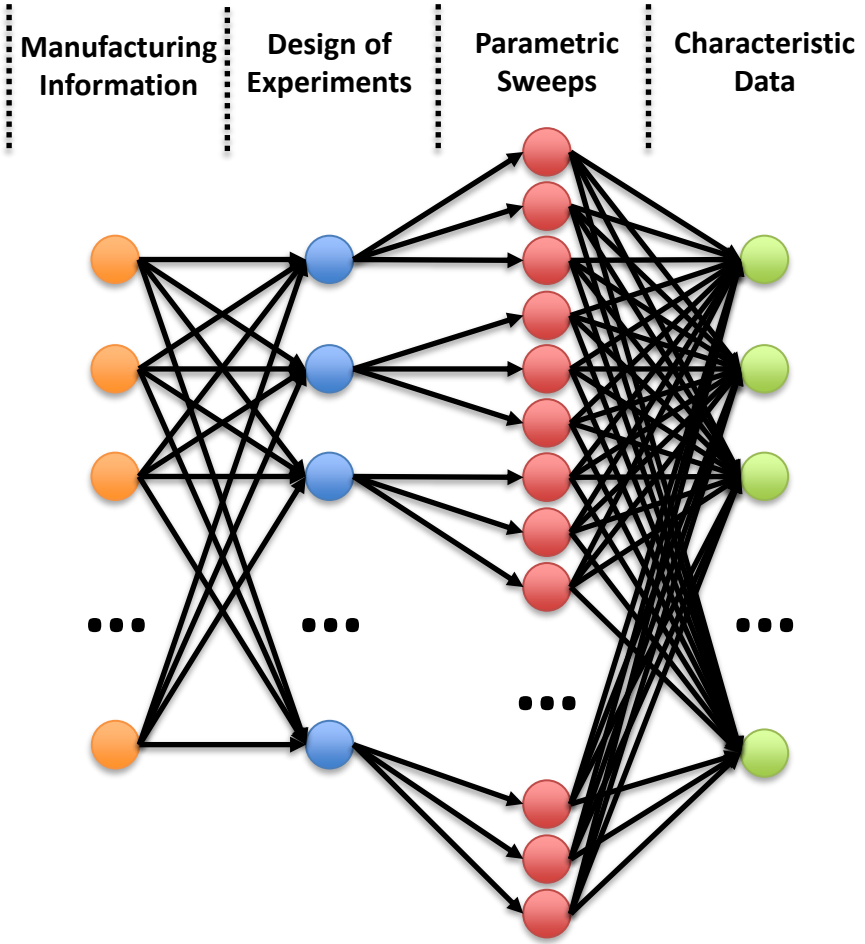
- **We performed a sensitivity analysis on the characteristics**
  - Shows the relative impact of characteristics
    - *What is worth the most time/effort*
    - *If miscorrelation occurs, what is most likely culprit*
- **Used manufacturing information as baseline**
  - Designed to be stackup agnostic
- **Only stripline and vias evaluated**
  - Due to resource constraints

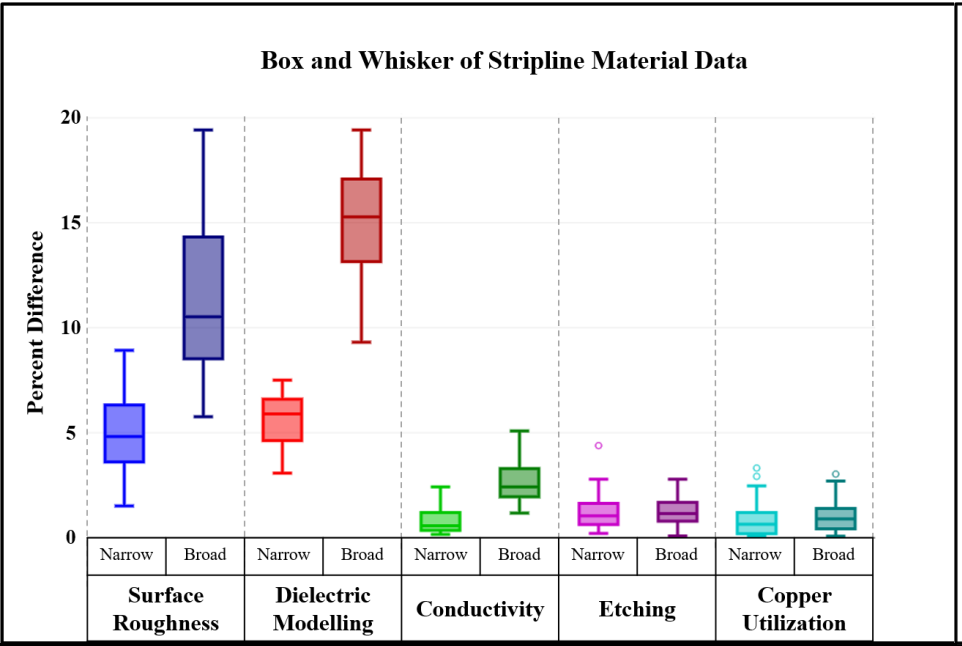


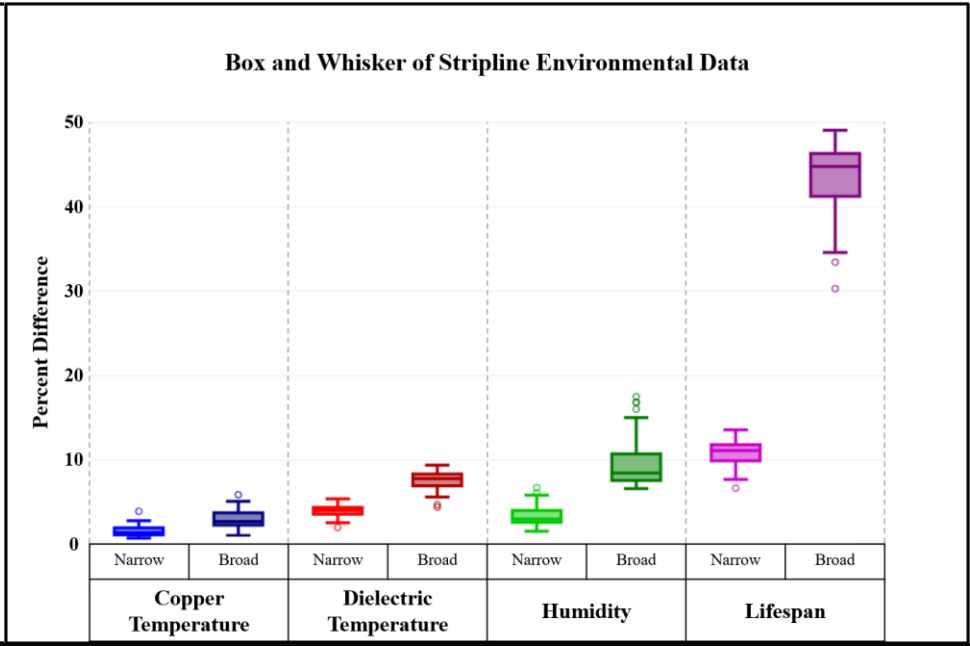


DOE of Characteristics

- **For each identified stackup from the DOE:**
  - We built a simulation to assess all characteristics
    - *A total of 100 unique models*
  - We ran a parametric sweep for each model
    - *36 variations to evaluate each characteristic*
  - Simulations ran out to 100GHz
- **This was combined into characteristic data**
  - Chart of percent difference from each characteristic
    - *Broad range*
    - *Narrow range*





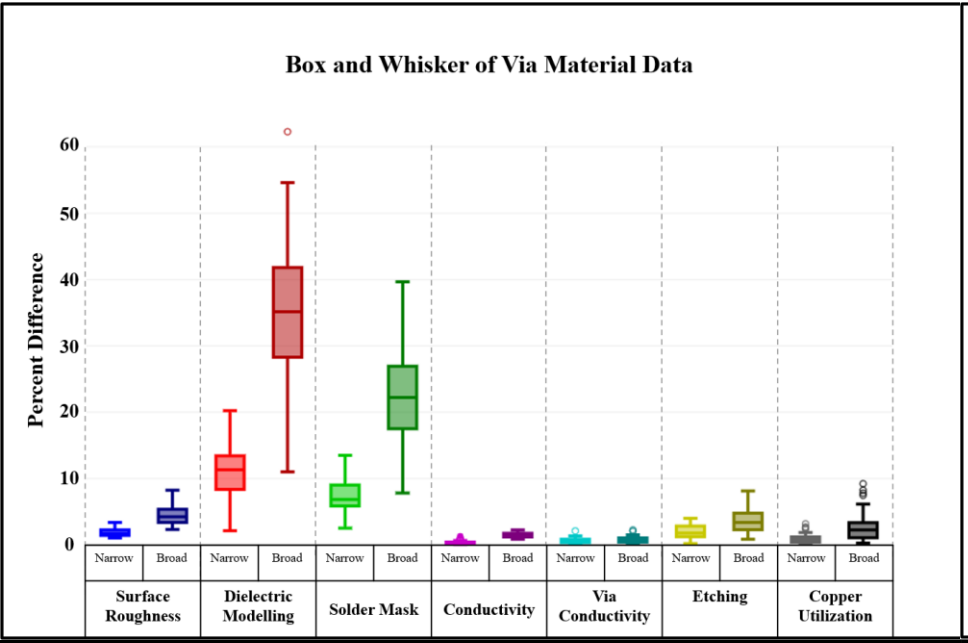


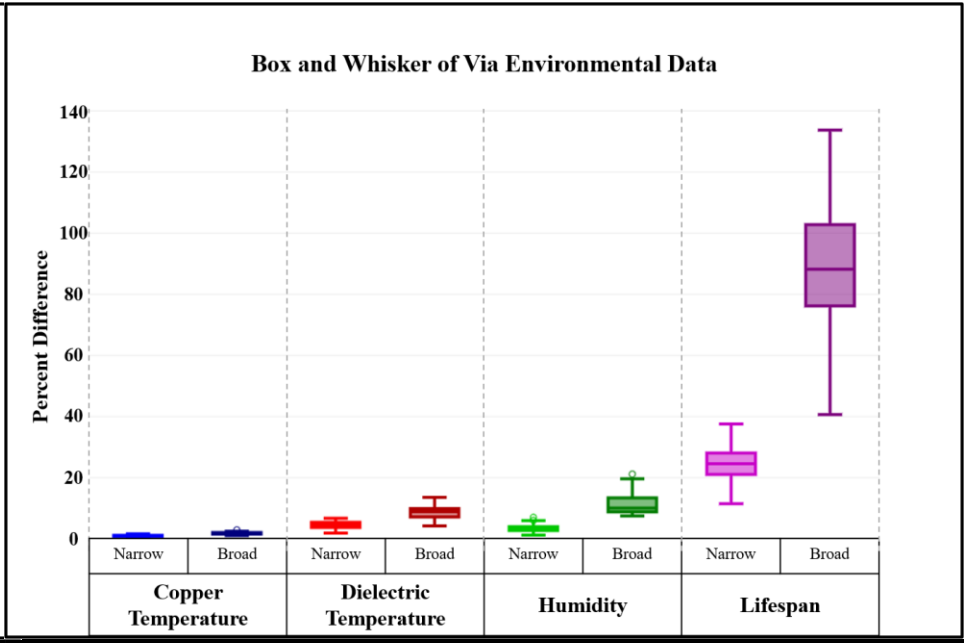
Stripline Material Data(Percent Difference Summary)

Characteristic	Average Narrow Range	Average Broad Range	Confidence
Surface Roughness	5.11%	11.41%	High
Dielectric Modelling	5.68%	15.19%	Medium
Conductivity	0.88%	2.68%	High
Etching	1.18%	1.22%	High
Copper Utilization	0.85%	1.01%	High

Stripline Enviromental Data(Percent Difference Summary)

Characteristic	Average Narrow Range	Average Broad Range	Confidence
Copper Temperature	1.60%	3.03%	High
Dielectric Temperature	3.94%	7.59%	Medium
Humidity	3.39%	9.78%	Low
Lifespan	10.72%	43.32%	Medium





Via Material Data(Percent Difference Summary)

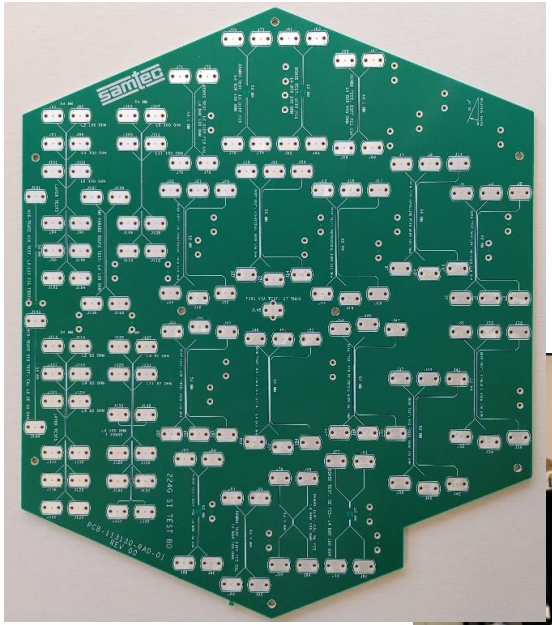
Characteristic	Average Narrow Range	Average Broad Range	Confidence
Surface Roughness	1.82%	4.41%	High
Dielectric Modelling	11.38%	35.60%	Medium
Soldermask	7.45%	22.80%	Low
Conductivity	0.37%	1.49%	High
Via Conductivity	0.65%	0.79%	Medium
Etching	2.01%	3.66%	High
Copper Utilization	0.98%	2.81%	High

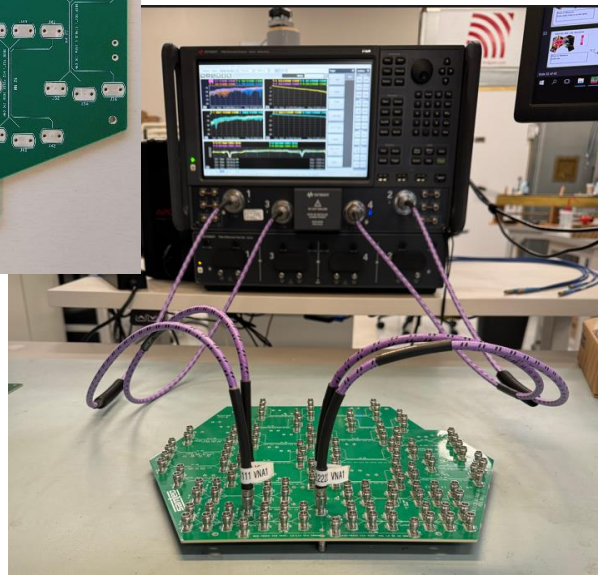
Via Enviromental Data(Percent Difference Summary)

Characteristic	Average Narrow Range	Average Broad Range	Confidence
Copper Temperature	0.93%	1.79%	High
Dielectric Temperature	4.50%	8.53%	Medium
Humidity	3.47%	11.24%	Low
Lifespan	24.42%	89.07%	Medium

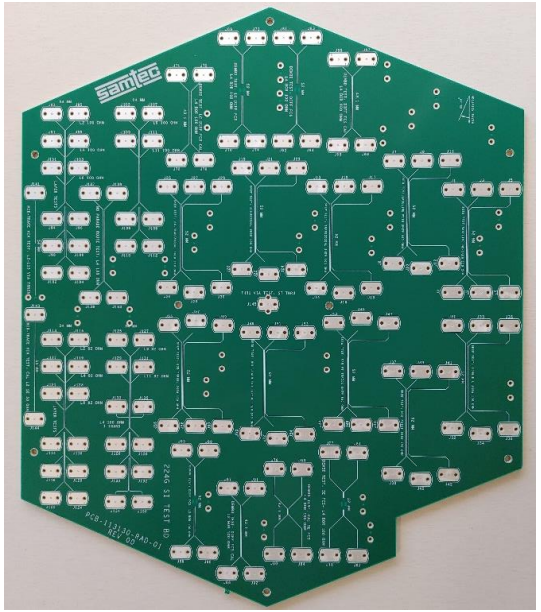
Measurements

- **A PCB was designed to verify methodology**
  - Built on numerous layers
  - Built using 224G techniques
  - Designed using the approaches within this survey
- **Goal is to demonstrate reasonable correlation**
  - Perfect correlation isn't the goal
  - Demonstrate techniques get close performance





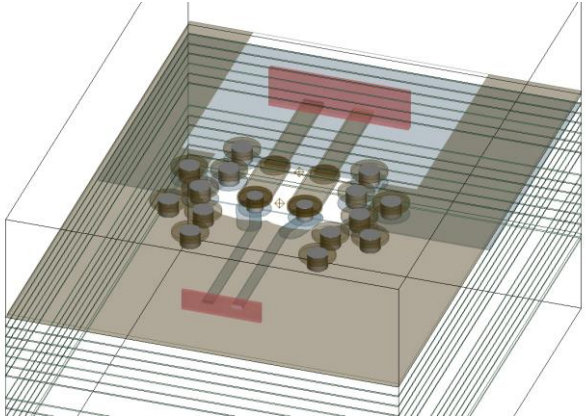
Measurements

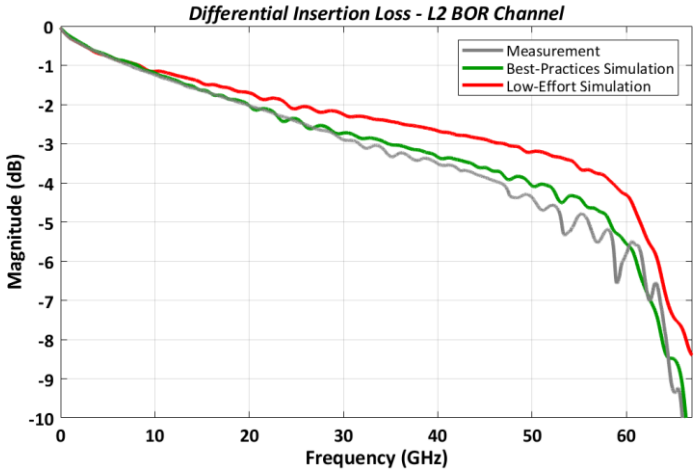


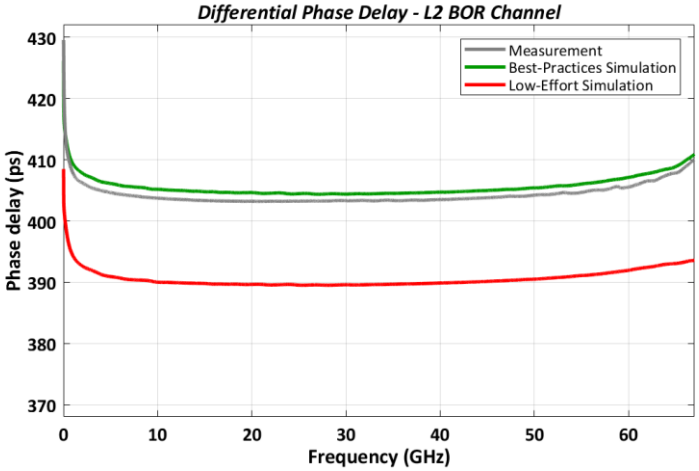
- **For these measurements, we will be showing:**
  - Measurement Data
  - Best-Practices Simulation
  - Low-Effort Simulation
- **Both simulations use:**
  - The same manufacturer information
  - The same values for characteristics
  - No manufacturer variation information
- **The difference between the simulations is how characteristics are implemented**
  - Getting the right values for characteristics isn't enough
  - How these values are implemented makes a tremendous difference in correlation
- **With just good implementation of characteristics, quality modelling can be achieved**

Measurements – L2 BOR

Characteristic	Best-Practices	Low-Effort
Surface Roughness	Modified High-Frequency Huray	Groiss
Dielectric Modelling	Layer-by-Layer with Multiplier on Manufacturer Information	Layer-by-Layer with Manufacturer Information
Conductivity	Characterized Copper Foil	Pure Copper
Via Conductivity	Characterized Via	Pure Copper
Etching	Implemented	Not Implemented
Copper Utilization	Implemented	Not Implemented

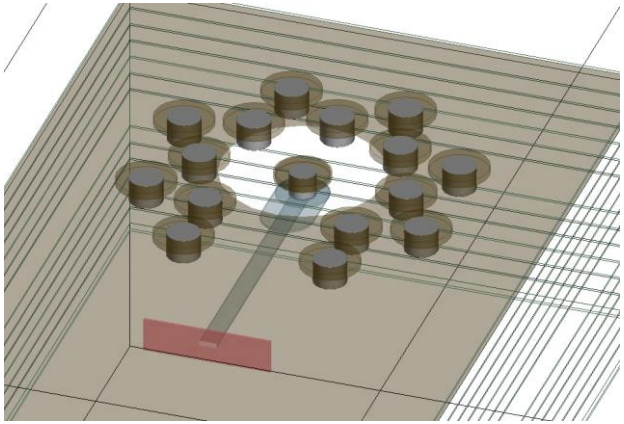


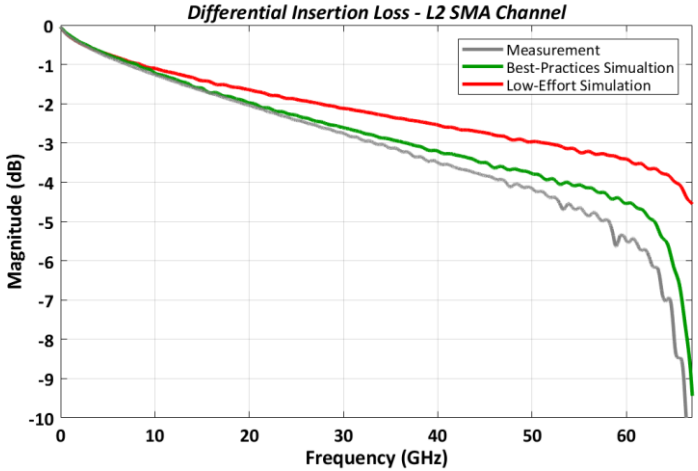


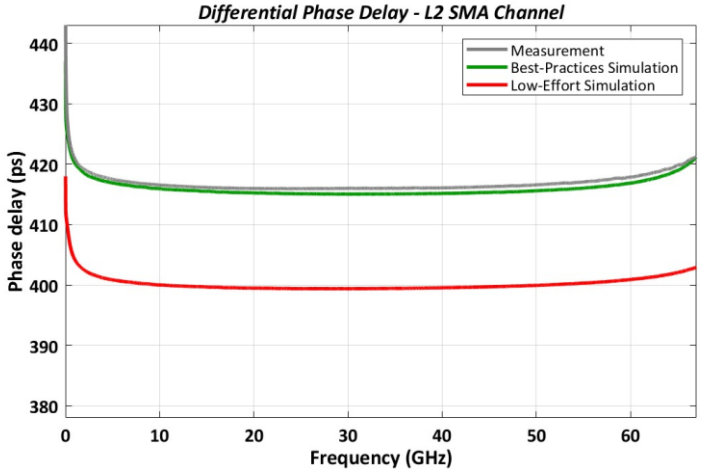


Measurements – L2 SMA Launch

Characteristic	Best-Practices	Low-Effort
Surface Roughness	Modified High-Frequency Huray	Groiss
Dielectric Modelling	Layer-by-Layer with Multiplier on Manufacturer Information	Layer-by-Layer with Manufacturer Information
Conductivity	Characterized Copper Foil	Pure Copper
Via Conductivity	Characterized Via	Pure Copper
Etching	Implemented	Not Implemented
Copper Utilization	Implemented	Not Implemented

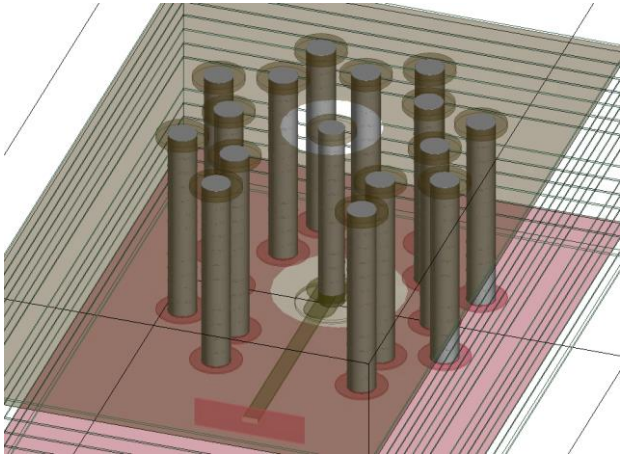


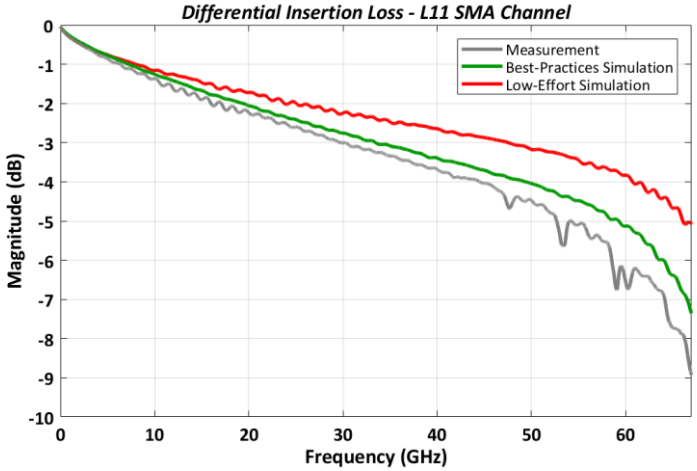


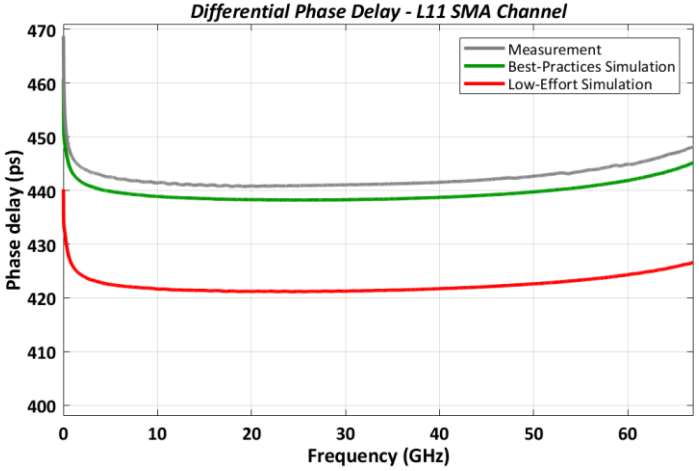


Measurements – L11 SMA Launch

Characteristic	Best-Practices	Low-Effort
Surface Roughness	Modified High-Frequency Huray	Groiss
Dielectric Modelling	Layer-by-Layer with Multiplier on Manufacturer Information	Layer-by-Layer with Manufacturer Information
Conductivity	Characterized Copper Foil	Pure Copper
Via Conductivity	Characterized Via	Pure Copper
Etching	Implemented	Not Implemented
Copper Utilization	Implemented	Not Implemented



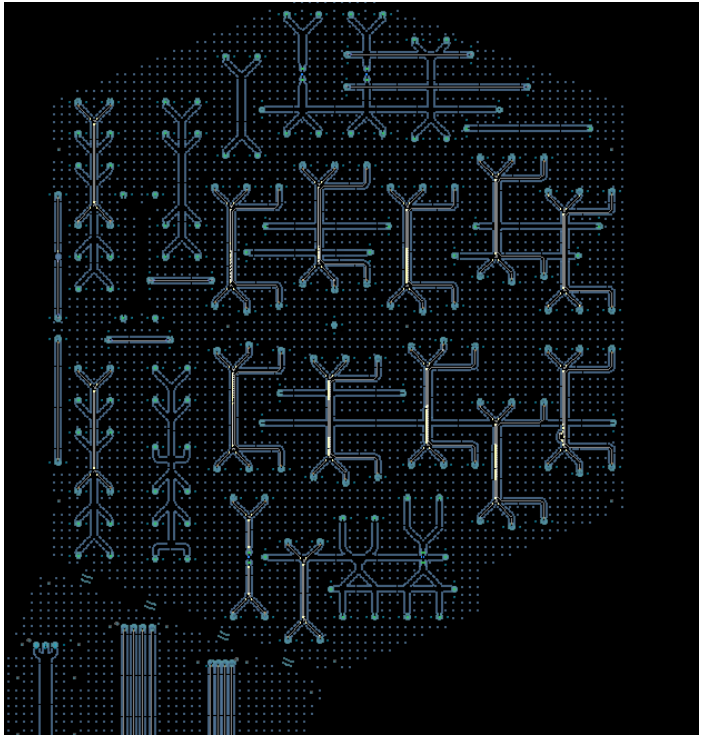




Conclusion

Conclusion

- **Our goal is to demonstrate a quicker alternative to the more complete correlation process**
- **From where our survey leaves off, more complete correlation could be completed**
  - CT scans & cross-sections
  - This work can be built upon with more advanced techniques
    - *As better data is available for a stackup, replace individual characteristics*
- **This survey is a starting point for considering these characteristics in future designs**
  - Increasing importance with 224G



More Information

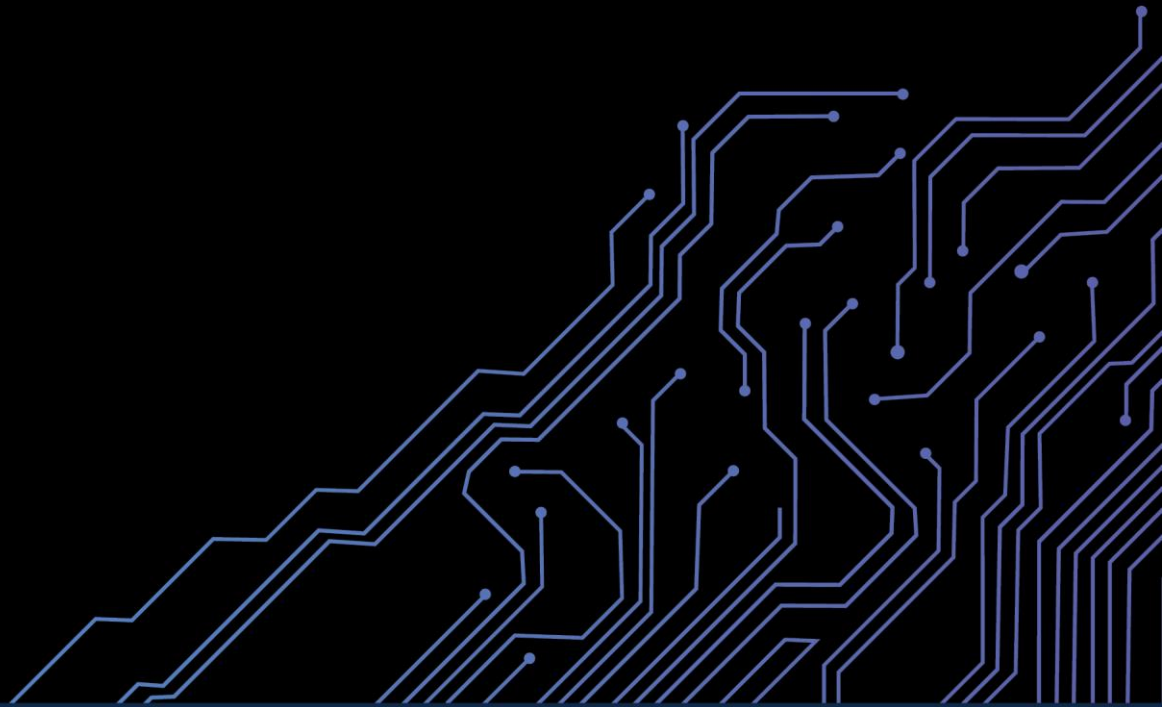
- **For more information:**
- **This slide deck has an extensive backup with more information**
  - More details on the DOE and parametric sweeps
  - How broad and narrow ranges were determined
  - Useful references for characteristics
- **The DesignCon paper on this topic also contains more details**
- **You can contact the Authors at:**
  - Robert.Branson@samtec.com
  - Greylan.Smoak@samtec.com

Thank you!

—

QUESTIONS?

Backup



DOE Further Details

Go into more details on DOE

- **The DOE was designed to cover a wide variety of stackups and board types**
  - This was intended so that the results of the sensitivity analysis best represented a variety of applications
  - The standard deviation of the data is higher as a result
  - However, the averages should be more accurate to all common 56-224G applications
- **Two different DOEs were performed**
  - One for differential stripline trace
  - One for a differential layer-to-layer via transition
- **The DOE varied based on manufacturer information**
  - One of the three categories from the introduction
  - Represents basic PCB background information

Differential Stripline Trace DOE Ranges

- **Prepreg Dk**
  - 2.8 – 4
- **Prepreg Df**
  - 0.001 – 0.02
- **Prepreg Dielectric Thickness**
  - 3mil – 6mil
- **Core Dk**
  - 2.8 – 4
- **Core Df**
  - 0.001 – 0.02
- **Core Dielectric Thickness**
  - 3mil – 6mil
- **Copper Thickness**
  - 0.25oz – 1oz
- **Trace Pitch**
  - 8mil – 15mil

Differential Via Transition DOE Ranges

- **Prepreg Dk**
  - 2.8 – 4
- **Prepreg Df**
  - 0.001 – 0.02
- **Prepreg Dielectric Thickness**
  - 3mil – 6mil
- **Core Dk**
  - 2.8 – 4
- **Core Df**
  - 0.001 – 0.02
- **Core Dielectric Thickness**
  - 3mil – 6mil
- **Copper Thickness**
  - 0.25oz – 1oz
- **Trace Pitch**
  - 8mil – 15mil
- **Via Pitch**
  - 28mil – 35mil
- **Drill Size**
  - 8mil – 12mil
- **Plating Thickness**
  - 1oz – 3oz
- **Soldermask Dk**
  - 3 – 4.5
- **Soldermask Df**
  - 0.01 – 0.025
- **Soldermask Thickness**
  - 0.5mil – 2mil

Parametric sweep

- **Parametric sweeps were run using a 3D EM Field Solver**
  - Each individual stackup was implemented from the DOE and run
- **The results were then all combined together and averaged to get the numbers shown in the DOE results table**
  - Percent difference from nominal was used for this calculation
  - This gives the fairest comparison between characteristics where nominal is 0 (such as humidity) and characteristics where nominal is in the middle of the range (like temperature)
- **Formula used for percent difference:**

$$Percent\ Difference = \frac{\left(\frac{|Nominal - RangeHigh| * 100}{\frac{|Nominal + RangeHigh|}{2}} + \frac{|Nominal - RangeLow| * 100}{\frac{|Nominal + RangeLow|}{2}}\right)}{2}$$

DOE Ranges

What Information this Section Covers:

- **This section will provide more information on the ranges that were used for characteristics in the DOE**
- **For more detailed discussion, see the DesignCon Paper on this topic**
- **For each characteristic, the information covered is:**
  - Units
    - *What units were used for that characteristic*
  - Narrow Range
    - *What were the exact numbers of the narrow range*
  - Broad Range
    - *What were the exact numbers of the broad range*
  - Basis for Ranges
    - *How were the ranges calculated*
    - *What data/resources were used to determine the ranges*

Surface Roughness Ranges

- **Unit**
  - Rz (microns)
- **Narrow Range**
  - 0.8-3.0 um
- **Broad Range**
  - 0.8-10.0 um
- **Basis for Ranges**
  - Used surface roughness numbers for common foil types in the 56-224G range
  - Identified as HVLP-HVLP5

Dielectric Modelling Ranges

- **Unit**
  - Dielectric Constant
- **Narrow Range**
  - 0 – 15% increase in Df
  - 0 – 5% increase in Dk
- **Broad Range**
  - 0 – 45% increase in Df
  - 0 – 15% increase in Dk
- **Basis for Ranges**
  - Used research papers which observed variation on dielectric properties from manufacturer datasheets

Soldermask Ranges

- **Unit**
  - Dielectric Constant
- **Narrow Range**
  - 0 – 15% increase in Df
  - 0 – 5% increase in Dk
- **Broad Range**
  - 0 – 45% increase in Df
  - 0 – 15% increase in Dk
- **Basis for Ranges**
  - The same values were used as for Dielectric Modelling due to a lack of prior research

Conductivity Ranges

- **Unit**
  - Siemens per meter (S/m)
- **Narrow Range**
  - $5.6 – 5.8 \times 10^7 (\frac{S}{m})$
- **Broad Range**
  - $4 – 5.94 \times 10^7 (\frac{S}{m})$
- **Basis for Ranges**
  - Based on experience of industry experts and outside research showing reduction in realized copper foil conductivity

Via Conductivity Ranges

- **Unit**
  - Siemens per meter (S/m)
- **Narrow Range**
  - $0.5 – 2.5 \times 10^7 (\frac{S}{m})$
- **Broad Range**
  - $0.5 – 5.94 \times 10^7 (\frac{S}{m})$
- **Basis for Ranges**
  - Based on experience of industry experts and copper conductivity ranges

Etching Ranges

- **Unit**
  - Total Width Variation on Top of Trace
- **Narrow Range**
  - +/- 10%
- **Broad Range**
  - +/- 20%
- **Basis for Ranges**
  - Speaking with PCB fabricators to determine variation that can be expected in PCBs

Copper Utilization Ranges

- **Unit**
  - Percentage Utilization on Copper Layer
- **Narrow Range**
  - 10 – 40%
- **Broad Range**
  - 0 – 100%
- **Basis for Ranges**
  - Speaking with industry experts to determine copper utilization for most ranges in 56-224G PCB designs

Copper Temperature Ranges

- **Unit**
  - Degrees Celsius (℃)
- **Narrow Range**
  - 15 – 70 ℃
- **Broad Range**
  - 0 – 105 ℃
- **Basis for Ranges**
  - Narrow range is based on ASHRAE Class A2 temperature standard
  - Broad range is based on speaking with industry experts on what gradient temperatures can be expected relative to ASIC position

Dielectric Temperature Ranges

- **Unit**
  - Degrees Celsius (℃)
- **Narrow Range**
  - 15 – 70 ℃
- **Broad Range**
  - 0 – 105 ℃
- **Basis for Ranges**
  - Narrow range is based on ASHRAE Class A2 temperature standard
  - Broad range is based on speaking with industry experts on what gradient temperatures can be expected relative to ASIC position

Humidity Ranges

- **Unit**
  - Humidity Percentage
- **Narrow Range**
  - 0 - 0.00091 increase in Df
- **Broad Range**
  - 0 - 0.00294 increase in Df
- **Basis for Ranges**
  - Used research papers which observed variation on dielectric properties from humidity

Lifespan Ranges

- **Unit**
  - Dielectric Constant
- **Narrow Range**
  - 0 – 30% increase in Df
  - 0 – 5% increase in Dk
- **Broad Range**
  - 0 – 200% increase in Df
  - 0 – 10% increase in Dk
- **Basis for Ranges**
  - Used research papers which observed variation on dielectric properties from lifespan

Additional Sources

What Information this Section Covers:

- **This section covers some of the most useful sources the authors found on the subject of each of the characteristics**
- **These resources provide a good overview of each characteristic:**
  - Talk through how the characteristic works
  - Give an overview of using the characteristic in models
- **For a complete list of sources, see the DesignCon paper on this topic**

Surface Roughness Additional Sources

- **J. A. Marshall, "A. F. Horn III, C. J. Caisse, et al., "Measuring Copper Surface Roughness for High Speed Applications", IPC Proceedings.**
  - This paper discusses the basics of surface roughness
  - Goes over notations seen on most datasheets

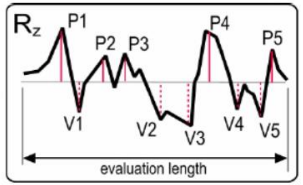


Figure 2 – Rz

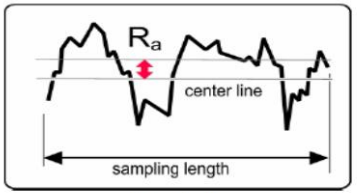


Figure 3 - Ra

- **Y. Shlepnev, "Conductor surface roughness modeling: From 'snowballs' to 'cannonballs'". 2019 Simberian.**
  - This paper discusses building a Huray Model
  - Goes over how the math behind getting accurate surface roughness models

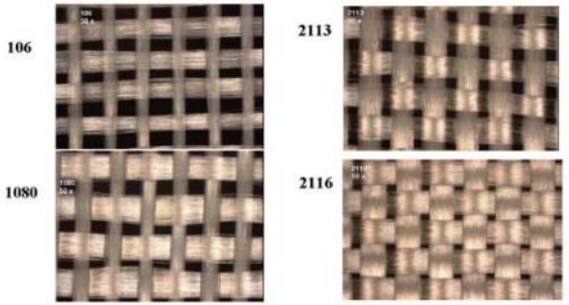
$$RF_i = 1 + \frac{3}{2} \cdot sr_i; \quad sr_i = \frac{2}{3} \cdot (RF_i - 1) \qquad (6)$$

Dielectric Modelling Additional Sources

- **A. Djordevic, R. Biljic, V. Likar-Smiljanic and T. Sarkar, "Wideband Frequency-Domain Characterization of FR-4 and Time-Domain Causality," IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, vol. 43, no. 4, pp. 662-667, 2001.**
  - This paper provides details on implementing the Djordevic-Sarkar Dielectric Model

$$\varepsilon_r = \varepsilon' - j\varepsilon'' = \varepsilon'(1 - j\tan\delta).$$

- **Altera, "PCB Dielectric Material Selection and Fiber Weave Effect on High-Speed Channel Routing".**
  - Provide a reference for selecting and implementing a dielectric material
  - Discusses basics of fiber weave effect on high-speed signals



Soldermask Additional Sources

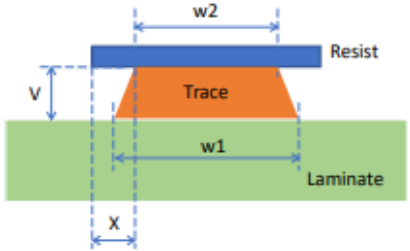
- **Y. Chen, F. Ye, Q. Hu, L. Kang, S. Zhang and J. Chen, "Research on the Influence of Solder Mask on Signal Integrity in High Speed PCB," 2021 IEEE 15th International Conference on Electronic Measurement & Instruments (ICEMI), Nanjing, China, 2021, pp. 259-263, doi: 10.1109/ICEMI52946.2021.9679657.**
  - This paper discuss the importance of soldermask in high speed signaling
  - Goes over different soldermask uses and their effects on signal integrity

TABLE I. THE MATERIAL CHARACTERISTICS OF THREE KINDS OF SOLDER MASK

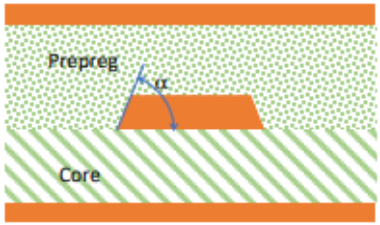
	FR-4	Common	Low Loss
Dk	4.4	3.8	3.2
Df	0.02	0.028	0.014

Etching Additional Sources

- **G. Blando, R. Bakleh, et al., "Etch Factor Impact on SI & PI", DesignCon 2019.**
  - Looks at the impact of etching on crosstalk and impedance
  - Goes over the basics on how etching can be determined



Etch factor = V / X



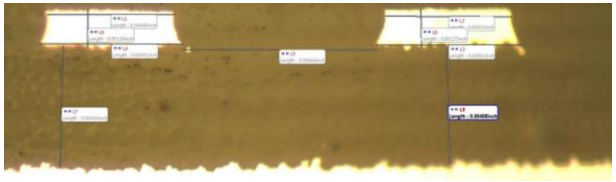
Copper Temperature Additional Sources

- **J. Miller, Y. Li, K. Hinckley, G. Blando, B. Guenin, I. Novak, A. Dengi, A. Rebelo and S. McMorrow, "Temperature and Moisture Dependence of PCB and Package Traces and the Impact on Signal Performance," in DesignCon, Santa Clara, 2012.**
  - Goes over transmission line losses with respect to temperature

- **J. Loyer, R. Kunze and G. Brist, "Humidity and Temperature Effects on PCB Insertion Loss," in DesignCon, Santa Clara, 2013.**
  - Similar to previous paper, also looks at transmission line losses with respect to temperature

Dielectric Temperature Additional Sources

- **J. Loyer, A. Burkhardt, R. Kunze and R. Attril, "Accurate Insertion Loss and Impedance Modelling of PCB Traces," in Design Con, Santa Clara, 2013.**
  - Looks at copper and dielectric side-by-side and tries to separate out the impacts



- **J. Miller, Y. Li, K. Hinckley, G. Blando, B. Guenin, I. Novak, A. Dengi, A. Rebelo and S. McMorrow, "Temperature and Moisture Dependence of PCB and Package Traces and the Impact on Signal Performance," in DesignCon, Santa Clara, 2012.**
  - Goes over the impact of dielectric in regards to temperature

Humidity Additional Sources

- **J. Miller, Y. Li, K. Hinckley, G. Blando, B. Guenin, I. Novak, A. Dengi, A. Rebelo and S. McMorrow, "Temperature and Moisture Dependence of PCB and Package Traces and the Impact on Signal Performance," in DesignCon, Santa Clara, 2012.**
  - Explains how humidity measurements are performed
  - Looks at the interrelationship between temperature and humidity

Lifespan Additional Sources

- **T. Rovensky, A. Pietrikova, O. Kovac and I. Vehec, "Influence of accelerating ageing on LTCC and PCB substrates' dielectric properties in GHz area," 2016 39th International Spring Seminar on Electronics Technology (ISSE), Pilsen, Czech Republic, 2016, pp. 189-192, doi: 10.1109/ISSE.2016.7563186.**
  - Goes into the background on lifespan
  - Explains how tests are conducted and looks at the resulting data