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Conference

January 30 – February 1, 2024

Santa Clara Convention Center

Expo

January 31 – February 1, 2024

Tutorial – How to Develop Advanced PCB Component Launches

SPEAKERS

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Scott McMorrow serves as a Strategic Technologist for Samtec, Inc. As a consultant for years too numerous to mention, Scott has helped many companies develop high performance products, while training signal integrity engineers. Today he works for "the man," where he continues being a problem solver, a change agent and "betting his job" every day.

Matthew Commens

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Responsible for the strategic product direction of the Ansys electronics software portfolio; including products HFSS, Maxwell, SIwave, and Icepak, and is a recognized expert in the application of computational electromagnetics.

Part 1 – Periodically Loaded Transmission Line Design and Optimization (a.k.a Via Launches)

Whereby We Discuss the Systematic Process of Optimizing Launches with Vias in Six "Simple" Steps

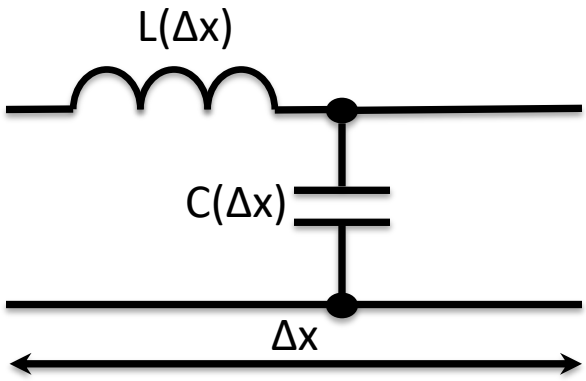
Table of Contents

- **Simplified Theory of Periodically Loaded Transmission Lines**
- **Trace Design**
- **Zones of Control**
- **Step-by-Step near-optimal optimization process**
- **Step 1 – Create a thru design with launch on top and bottom.**
  - Signal Via Drill Size
  - Antipad Diameter for thick and thin plane layers.
  - Ground Via Drill Size (optional).
- **Step 2 – Create trace escapes on selected layers**
  - Optimize plane antipads above and below trace layers.
  - Fine tune via pitch.
  - Fine tune thick and thin plane antipad diameters.

Table of Contents - continued

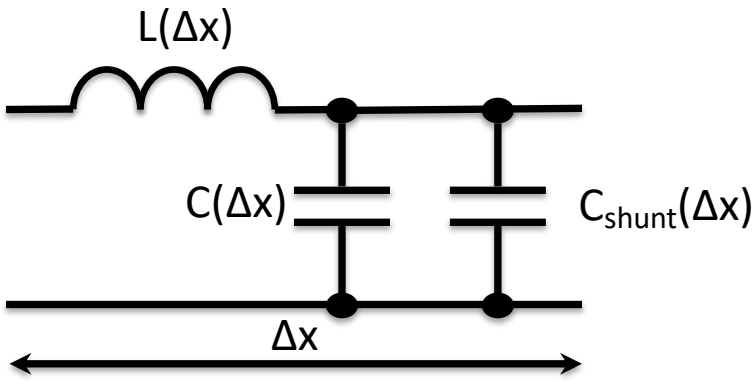
- **Step 3 – Simulate FEXT and NEXT**
  - Utilize 1 Row by 2 column array of launches to simulate in-row FEXT.
  - Utilize 2 Row and 1 Column array of launches to simulation row-to-row NEXT
- **Step 4 – Evaluate Potential Patterns for Routing**
  - Generate representative arrays of launches to visualize the various ways in which full package/connector routing may be accomplished.
- **Step 5 – Additional Ground Stitch Via Placement**
  - After evaluating and choosing an appropriate launch pattern for routing, visually determine locations for additional ground stitch vias for reduction of crosstalk.
- **Step 6 – Simulate Final Launch Array Design**
  - Document final results and transfer s-parameters to other tools for end-to-end channel simulation.
  - Or export/copy final design into comprehensive model of PCB BORs and Package/Connector 3D Models.

Simple Incremental LC Transmission Line



$$Z = \sqrt{\frac{L(\Delta x)}{C(\Delta x)}} \qquad Td = \sqrt{L(\Delta x) * C(\Delta x)}$$

Periodically Shunt Loaded Transmission Line



Distributed capacitive loading of planes:

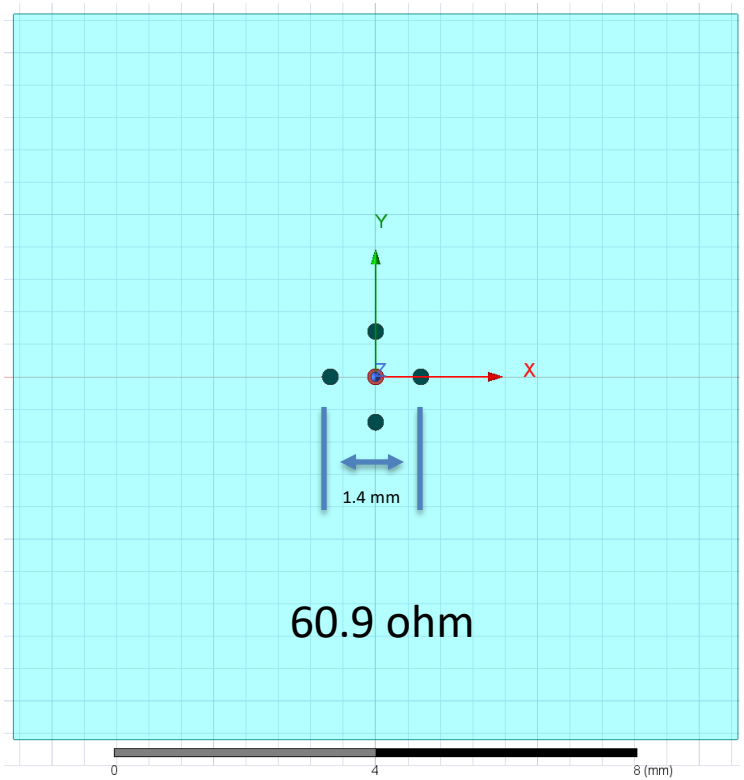
- reduces impedance
- Increases Delay
- Increases Loss

Coupled planes are orthogonal to the transmission line.

$$Z = \sqrt{\frac{L(\Delta x)}{C(\Delta x) + Cshunt(\Delta x)}}$$

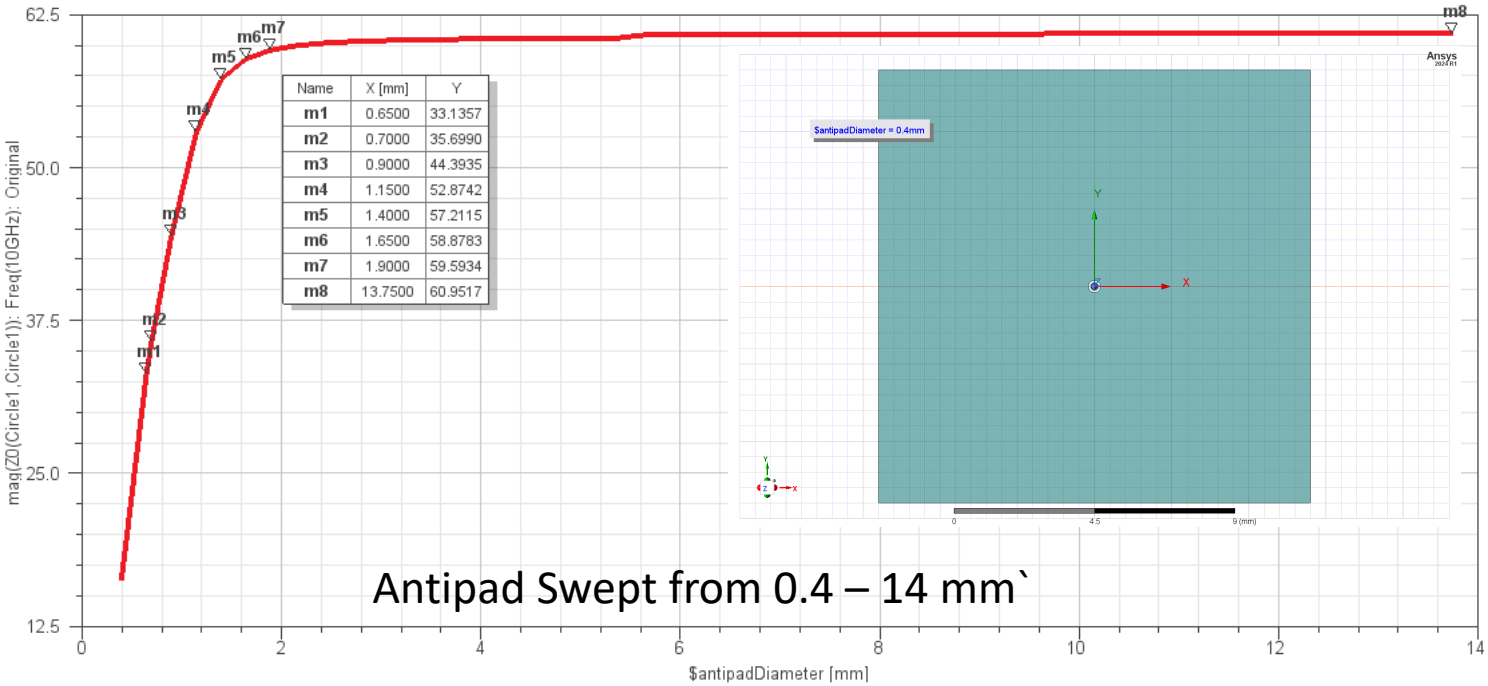
$$Td = \sqrt{L(\Delta x) * (C(\Delta x) + Cshunt(\Delta x)}$$

2D SE Impedance – Signal plus 4 Ground Vias



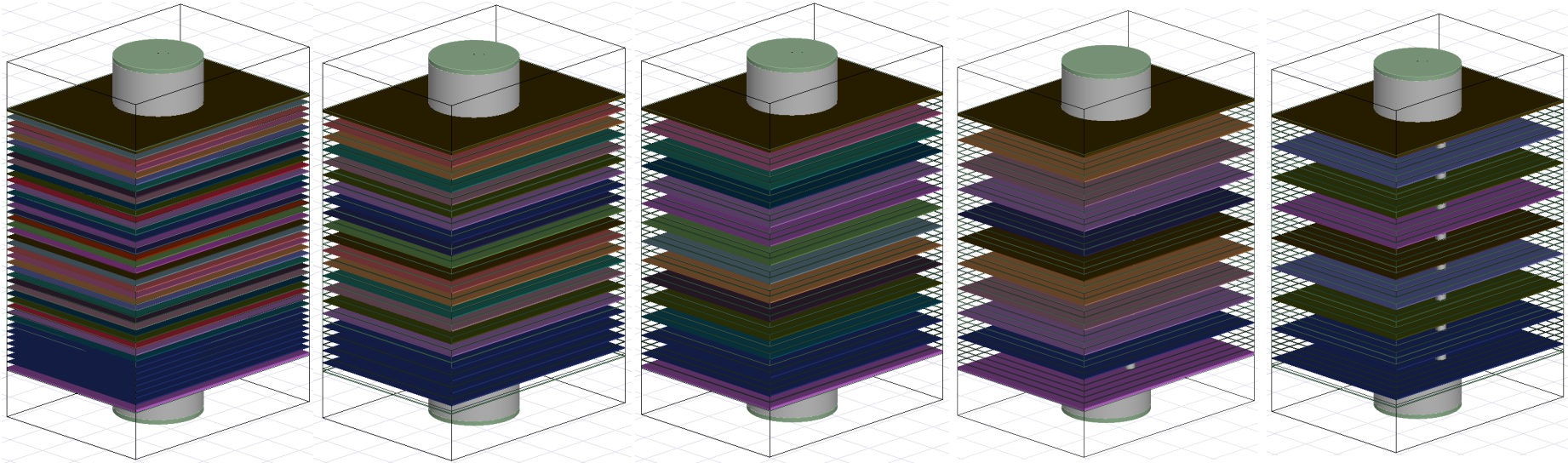
0.25 mm vias
0.7 mm space
Dielectric Dk - 3.0

2D SE Impedance – Signal plus 4 Ground Vias and Plane with Antipad



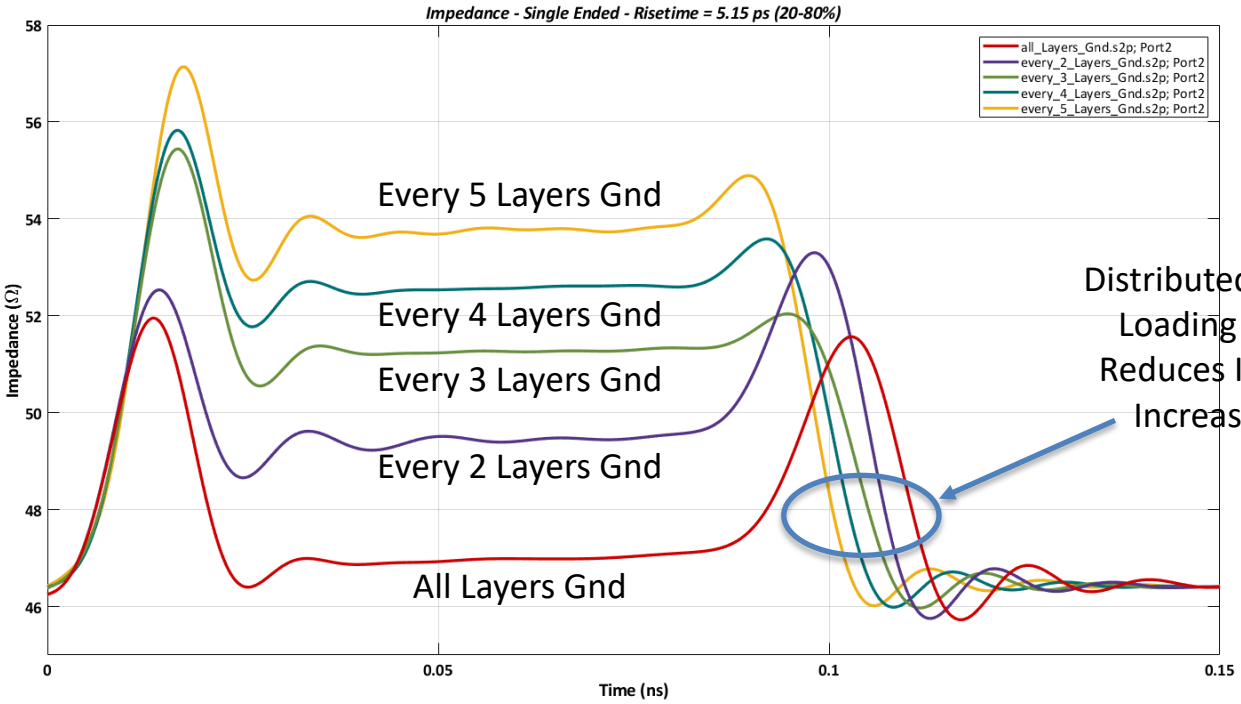
Name	X [mm]	Y
m1	0.6500	33.1357
m2	0.7000	35.6990
m3	0.9000	44.3935
m4	1.1500	52.8742
m5	1.4000	57.2115
m6	1.6500	58.8783
m7	1.9000	59.5934
m8	13.7500	60.9517

Impedance Variation vs Frequency of Ground Layers



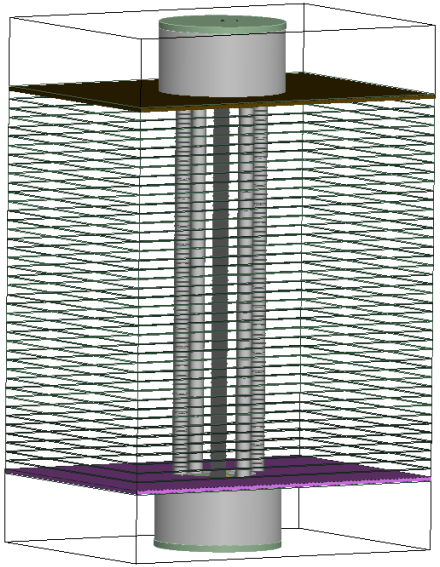
All Layers Gnd | Every 2 Layers Gnd | Every 3 Layers Gnd | Every 4 Layers Gnd | Every 5 Layers Gnd

Impedance Variation vs Frequency of Ground Layers

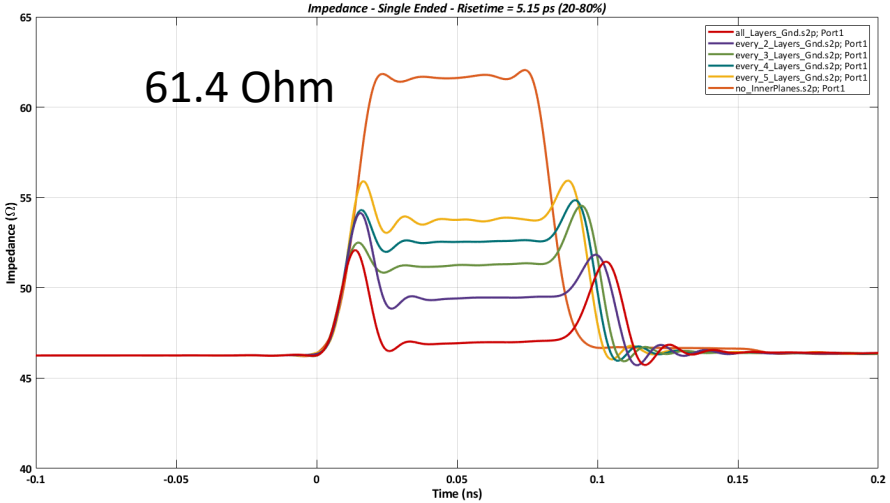


Distributed Capacitive Loading of Planes Reduces Impedance Increases Delay

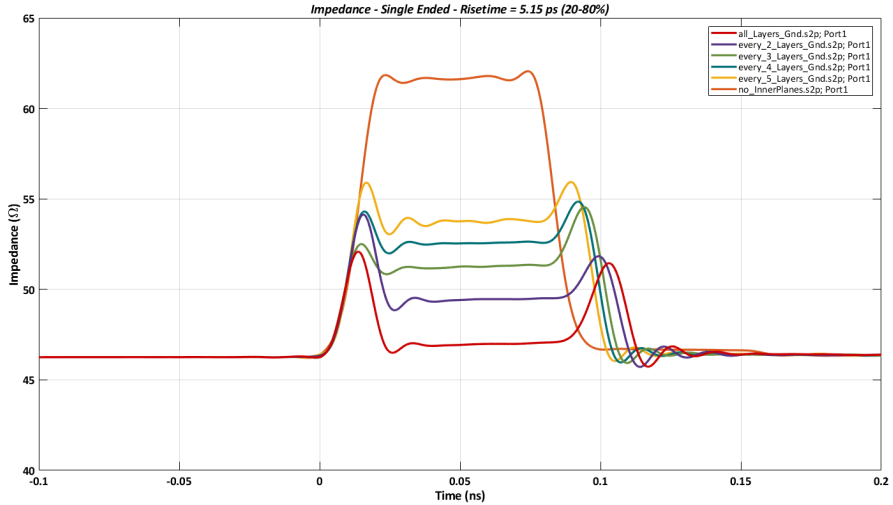
SE Via Surrounded by 4 Gnd Via
No Ground Planes



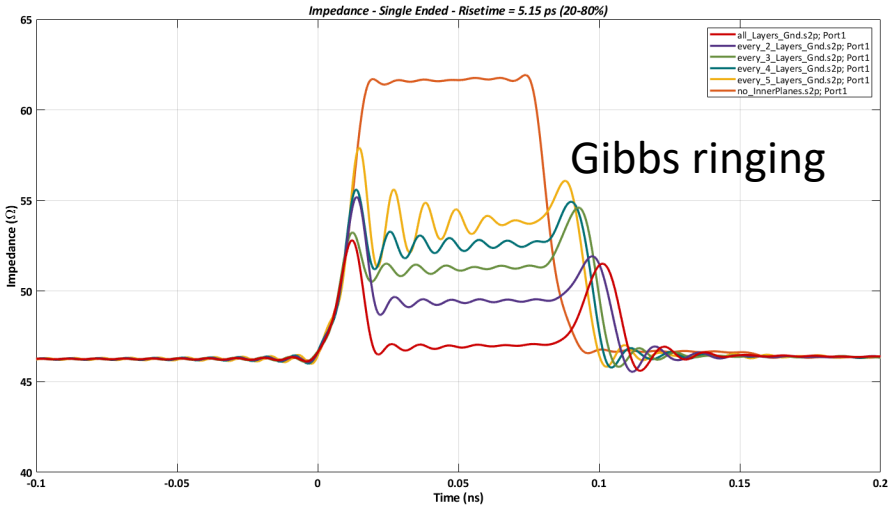
0.25 mm Vias
0.7 mm Space
0.7 mm Antipad
Dielectric Dk - 3.0
42 Layer



Filtered vs Unfiltered TDR

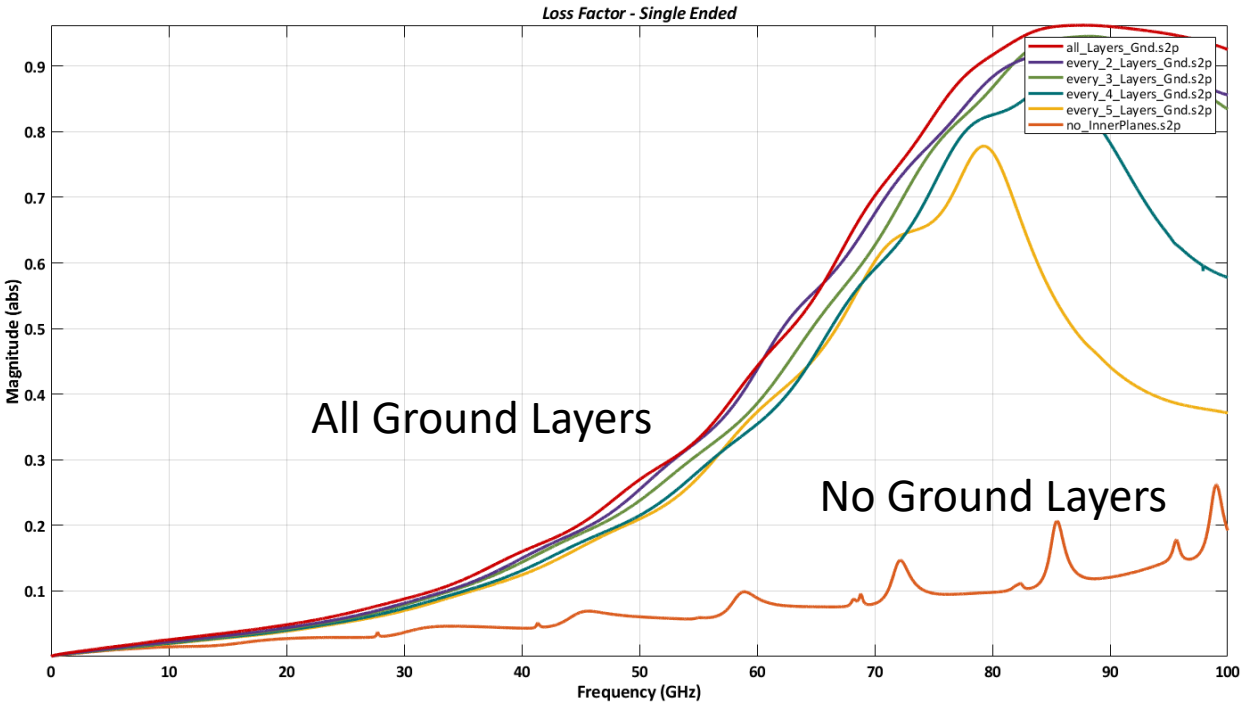


Sin response with driver BW filter



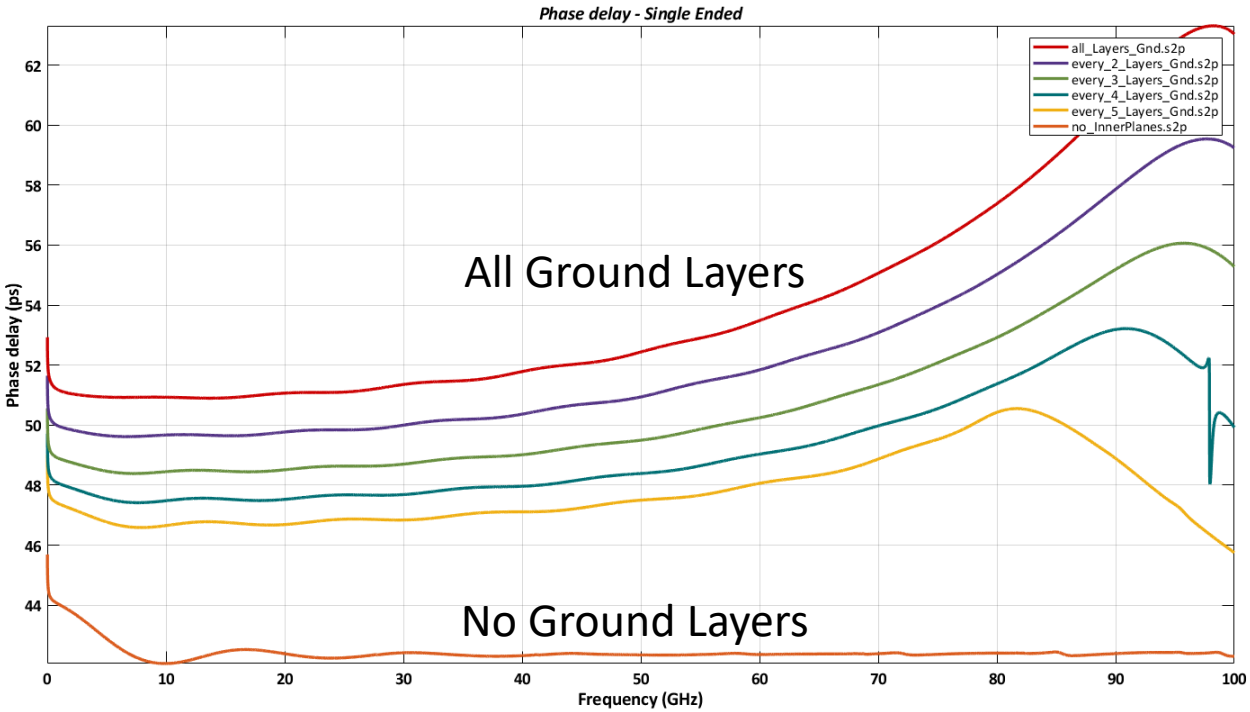
Ramp with Tukey brickwall filter

Loss Factor vs Frequency of Ground Layers



Loss Factor increases with the number of plane layers.

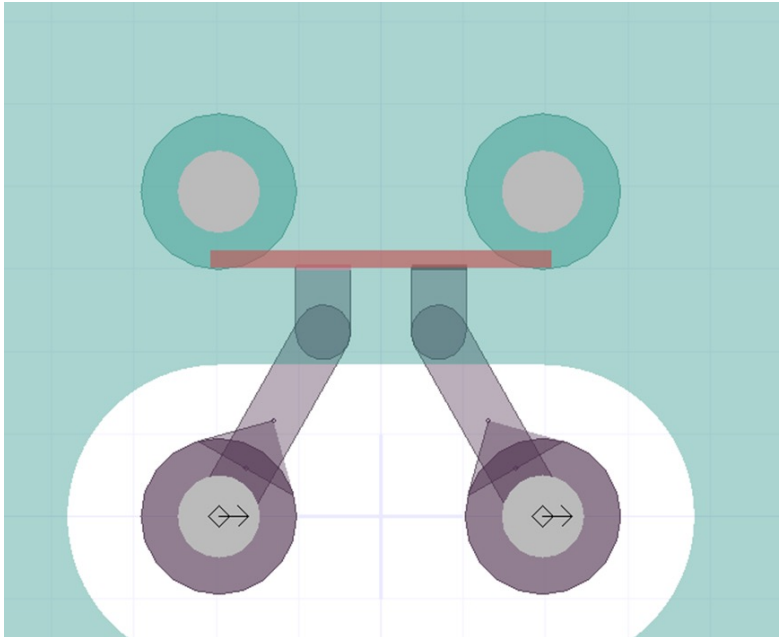
Phase Delay vs Frequency of Ground Layers



Breakout (BOR) and Trace Design

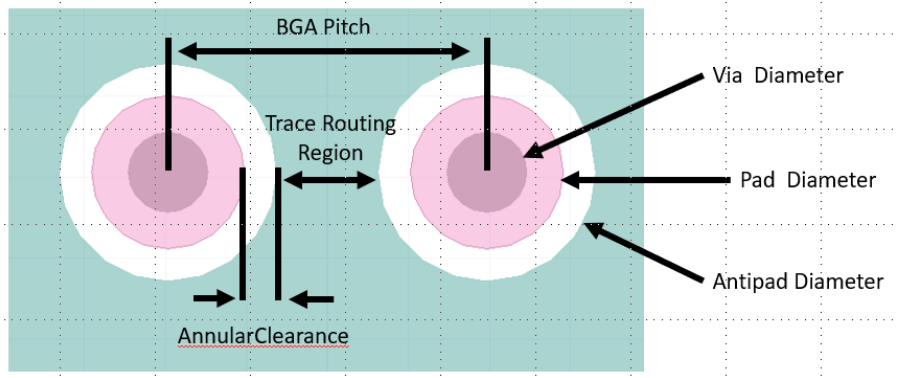
SIBORG™
SIGNAL INTEGRITY BREAK OUT REGION GURU

- **Important parameters**
  - $viaDiameter_SigVia - 0.2, 0.225, 0.25 mm (8, 9,10 mil)
  - $padAnnularRing - 0.115, 0.127 mm (4.5, 5 mil)
  - $minAnnularClearance – 0.1 mm (4 mil)
  - Pad Diameter = $viaDiameter_SigVia + 2 * $padAnnularRing
- **Important! - For signal integrity modeling, all vias are drawn at the drill size, not the plated hole size.**
  - Failure to check this will lead to significant performance penalties from incorrect modeling.



Routing Region

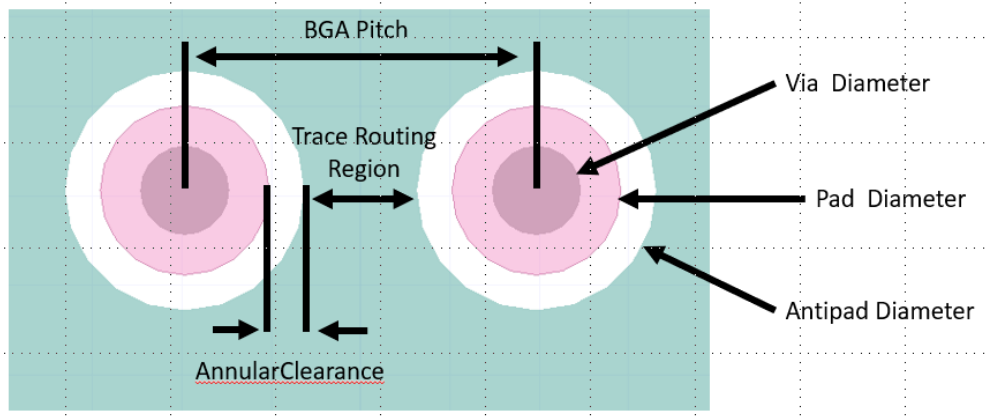
- **Remember!**
- **Even if the layer is a ground layer will full contact ground vias, an annular clearance from trace metal to the ground pad/via must be provided**
- **A via pad defines the via capture region that is the circular probability of error of the drill strike location.**
- **An annular clearance is created to account for manufacturing tolerances in placement of the via and the trace etch.**

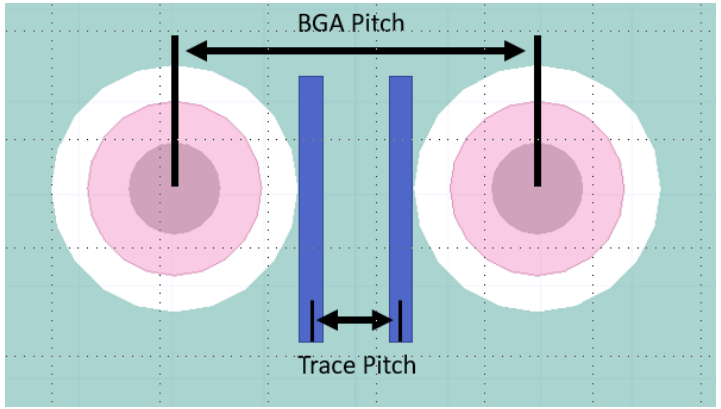


Available Trace Routing Space = BGA_Pitch – Antipad_Diameter

Antipad_Diameter = ViaDiameter + 2 x PadAnnularRIng+ 2 x MinimumAnnularClearance

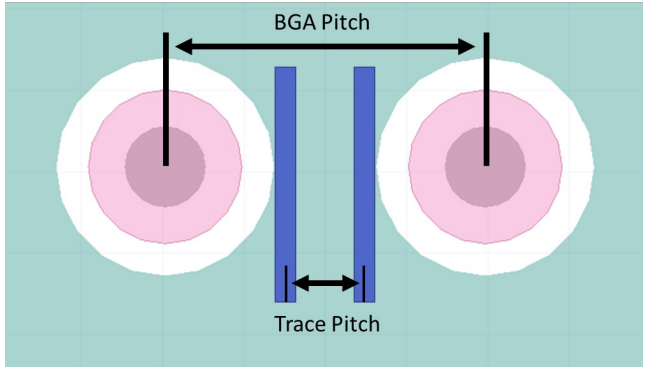
Minimum Trace to Via Spacing

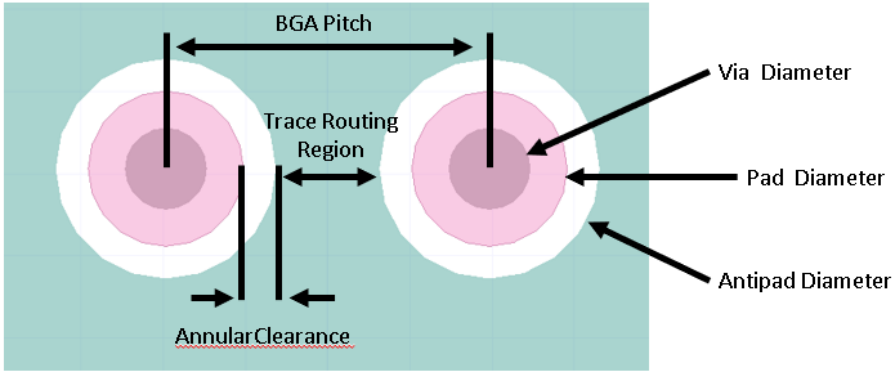




Trace Routing Space = TracePitch + TraceWidth
More space for fringe fields is always better.

Routing Space for 1 mm Pitch BGA



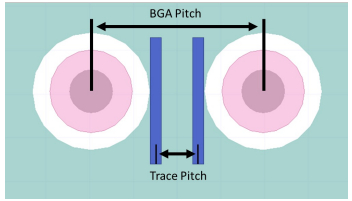


BGA Pitch (mm)	Via Diameter (mm)	Pad Annular Ring (mm)	Min Annular Clearance (mm)	Available Routing Space (mm)	Available Routing Space (mi)
1	0.2	0.115	0.1	0.37	14.57
1	0.2	0.127	0.1	0.346	13.62
1	0.225	0.115	0.1	0.345	13.58
1	0.225	0.127	0.1	0.321	12.64
1	0.25	0.115	0.1	0.32	12.60
1	0.25	0.127	0.1	0.296	11.65

Trace Design for 92.5 Ohm Impedance
Dk = 3.0, 0.25 mm Drill, 0.115 mm Clearance

Allowable Trace Routing Range
@92.5 ohm

Trace Width (mil)	Pitch (mil)	Route Space (mil)
3.75	6.1	9.85
4	6.6	10.6
4.25	7.1	11.35
4.5	7.6	12.1
4.75	8.1	12.85
4.8	8.2	13
4.9	8.5	13.4
5	8.7	13.7



27_metal	signal	copper	programmableAnisotropicMaterial	0.6mil
27_die	dielectric	programmableAnisotropicMaterial		5mil
28_metal	signal	copper	programmableAnisotropicMaterial	0.6mil
28_die	dielectric	programmableAnisotropicMaterial		5.39mil
29_metal	signal	copper	programmableAnisotropicMaterial	0.6mil

BGA Pitch (mm)	Via Diameter (mm)	Pad Annular Ring (mm)	Min Annular Clearance (mm)	Available Routing Space (mm)	Available Routing Space (mi)
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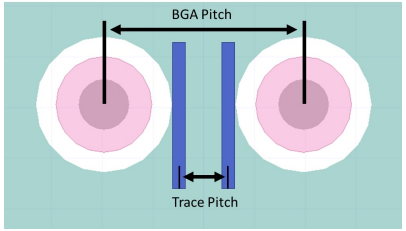
1	0.25	0.115	0.1	0.32	12.60
1	0.25	0.127	0.1	0.296	11.65

Trace Design for 92.5 Ohm Impedance
Dk = 3.0, 0.225 mm Drill, 0.115 mm Clearance

Trace Width (mil)	Pitch (mil)	Route Space (mil)
3.75	6.94	10.69
4	7.5	11.5
4.25	8.2	12.45
4.5	8.9	13.4
4.75	9.7	14.45
4.8	9.9	14.7
4.9	10.3	15.2
5	10.7	15.7



27_metal	signal	copper	programmableAnisotropicMaterial	0.6mil
27_die	dielectric	programmableAnisotropicMaterial		5mil
28_metal	signal	copper	programmableAnisotropicMaterial	0.6mil
28_die	dielectric	programmableAnisotropicMaterial		5.39mil
29_metal	signal	copper	programmableAnisotropicMaterial	0.6mil

BGA Pitch (mm)	Via Diameter (mm)	Pad Annular Ring (mm)	Min Annular Clearance (mm)	Available Routing Space (mm)	Available Routing Space (mi)
1	0.2	0.115	0.1	0.37	14.57
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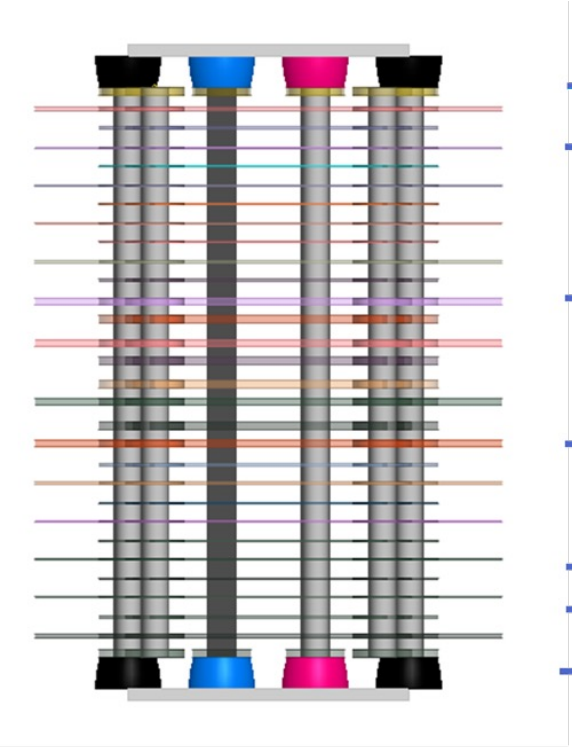
Zones of Control



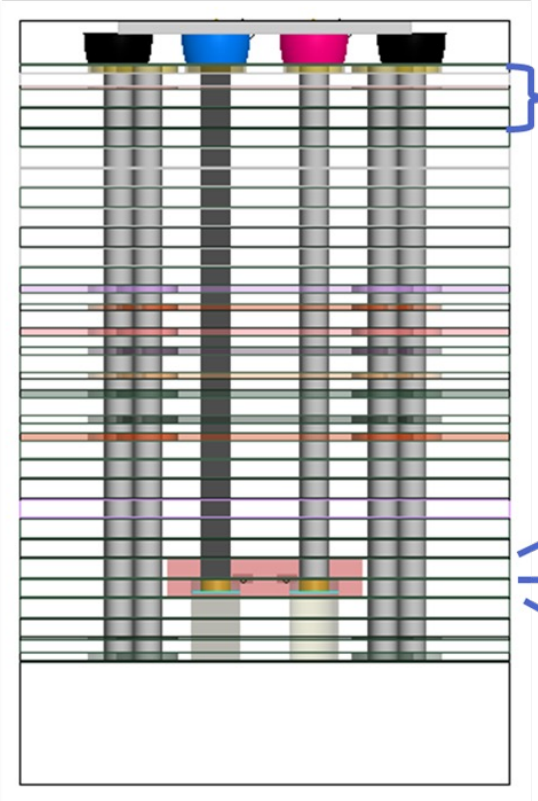
PlanesBelowTop

ThinTraceLayers

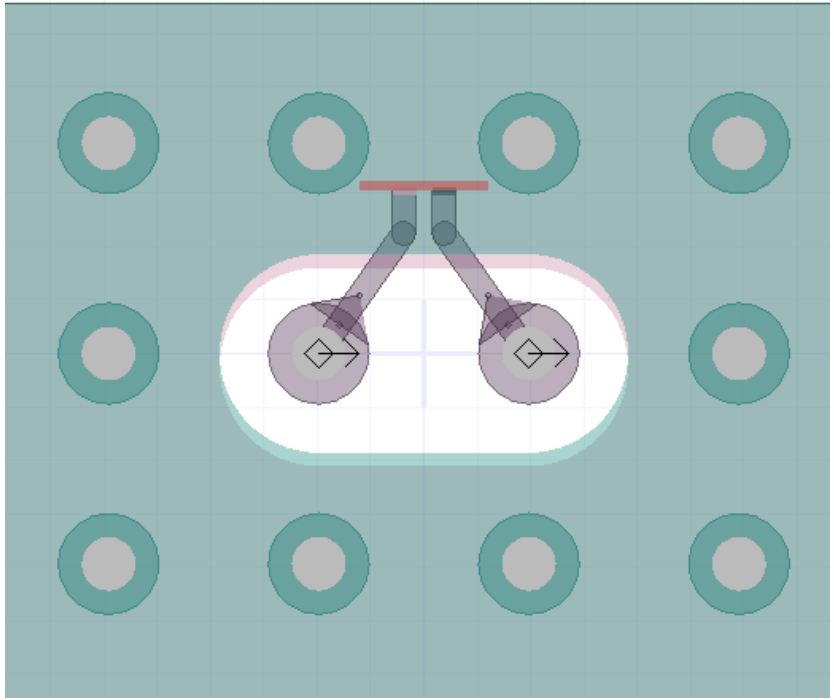
ThickPowerPlaneLayers

ThinTraceLayers

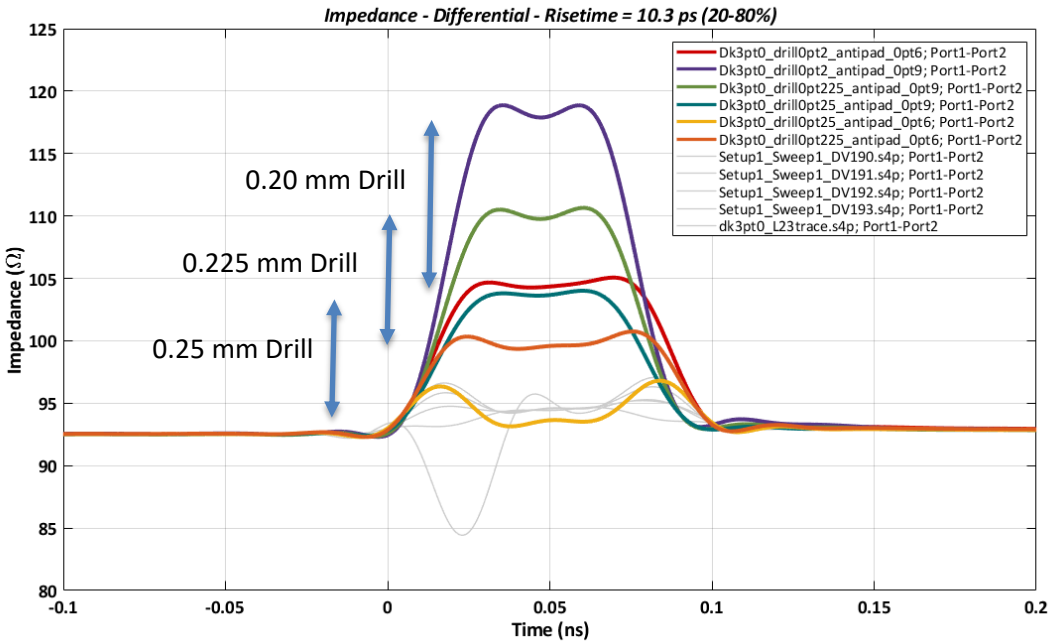
BackdrillLayers

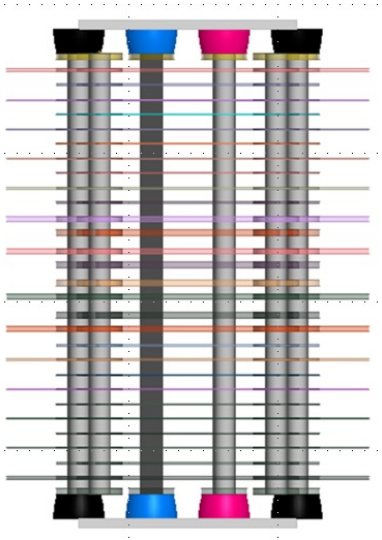


1 mm Pitch BGA Via-in-Pad



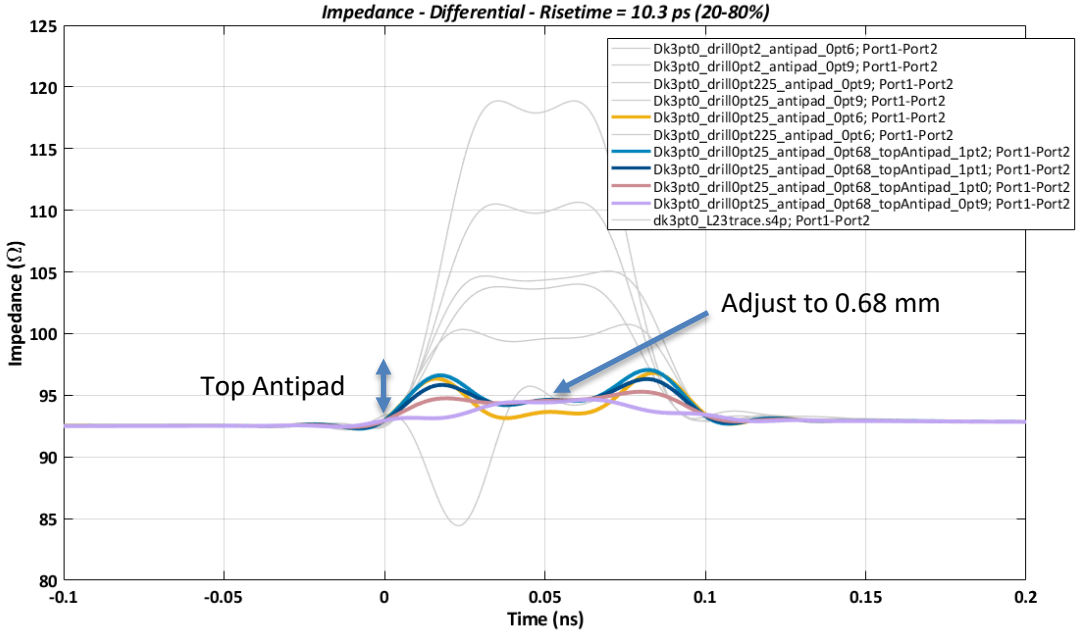
Dk 3.0
Vary Drill Size (0.2, 0.225, 0.25 mm)
Vary Antipad (0.6, 0.9 mm)

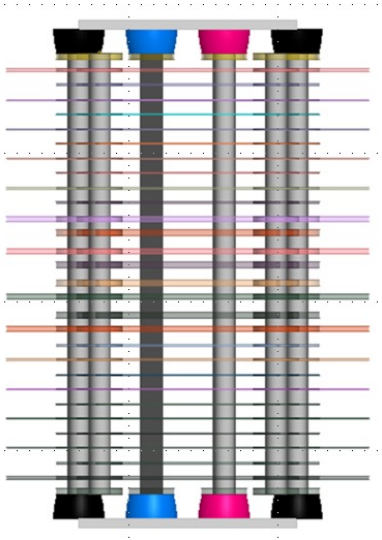




Thru Design

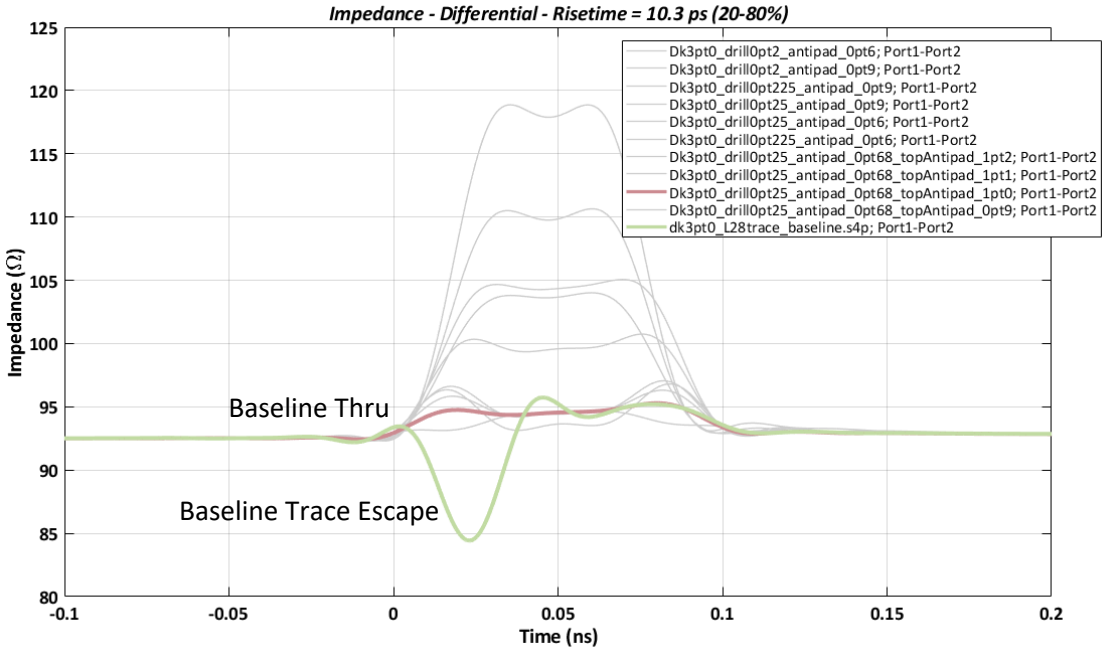
Dk 3.0
Drill Size (0.25 mm), Thin Layer Antipad (0.68 mm)
Vary Top Antipad (0.9 to 1.2 mm)

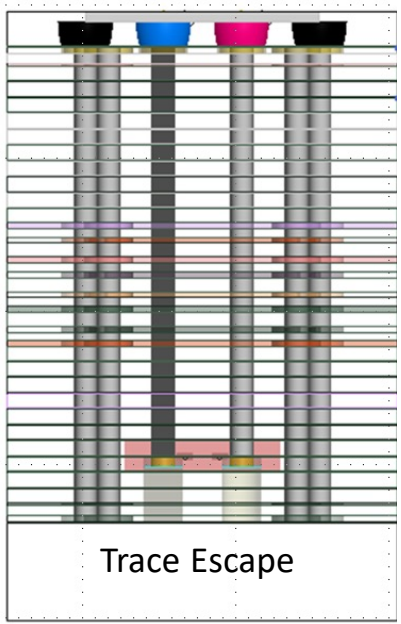




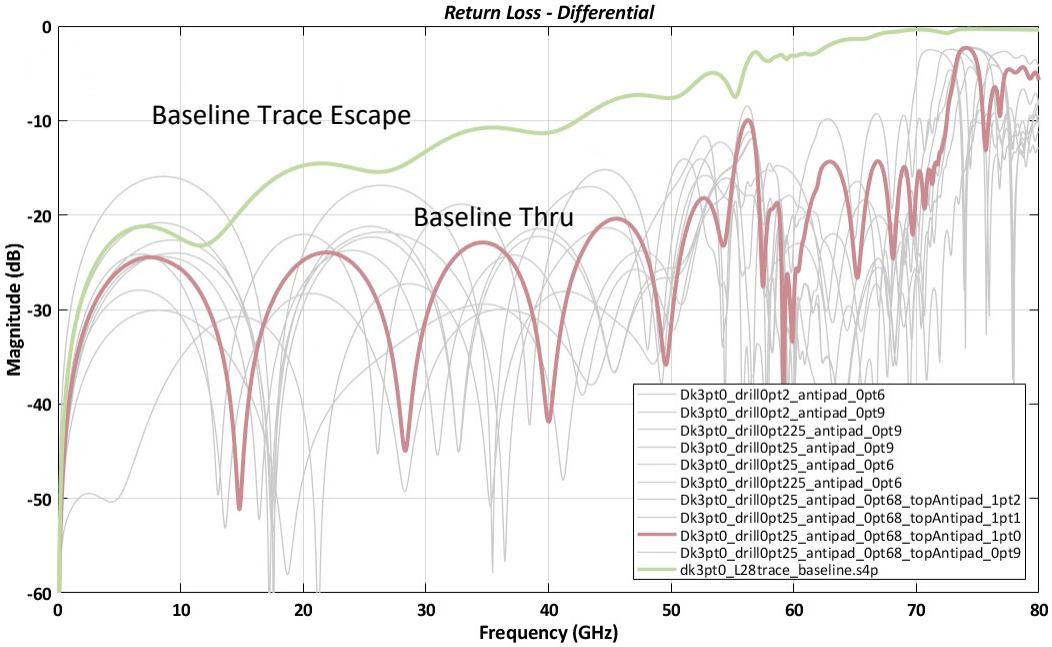
Thru Design

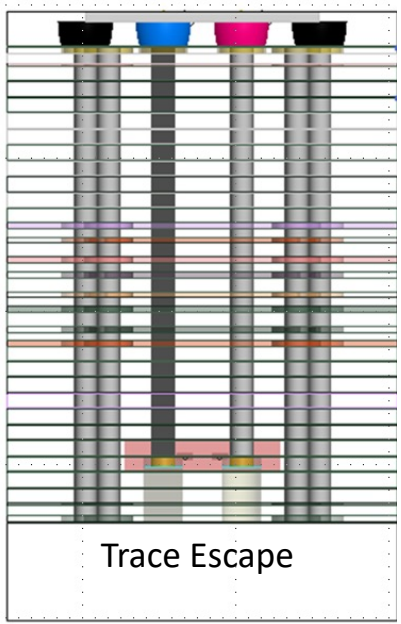
Baseline Trace Escape
Drill (0.25 mm), Top Antipad (1 mm)
Thin Layer Antipad (0.68 mm), Backdrill Stub (6 mil)



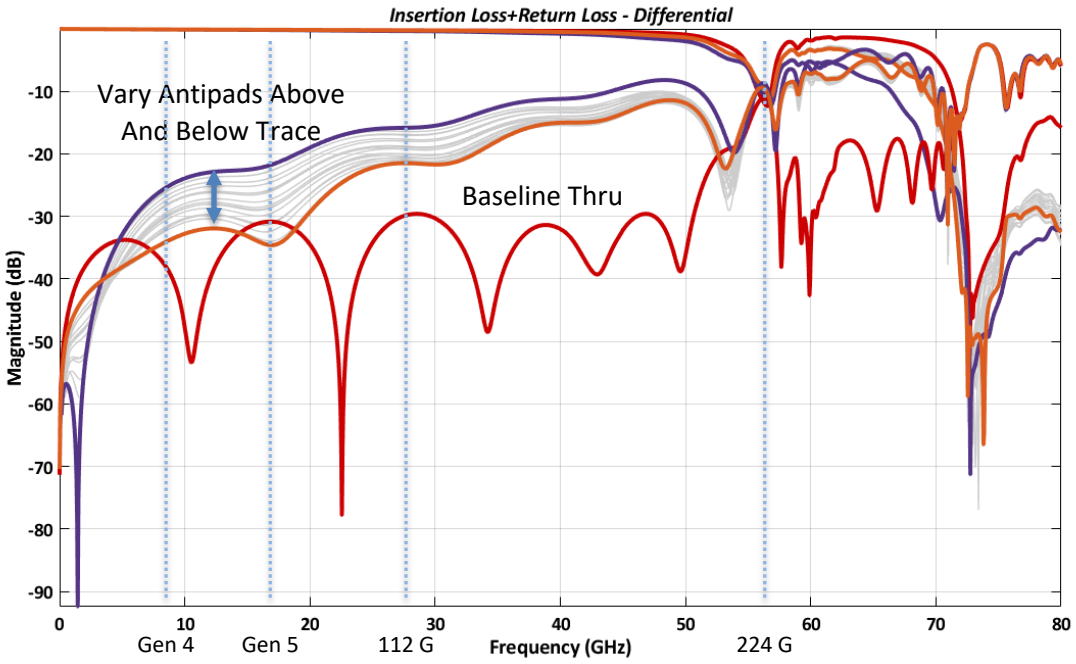


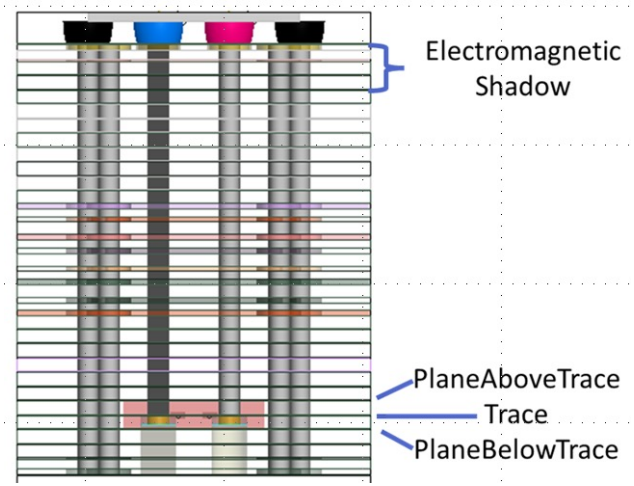
Baseline Trace Escape
Drill (0.25 mm), Top Antipad (1 mm)
Thin Layer Antipad (0.68 mm), Backdrill Stub (6 mil)



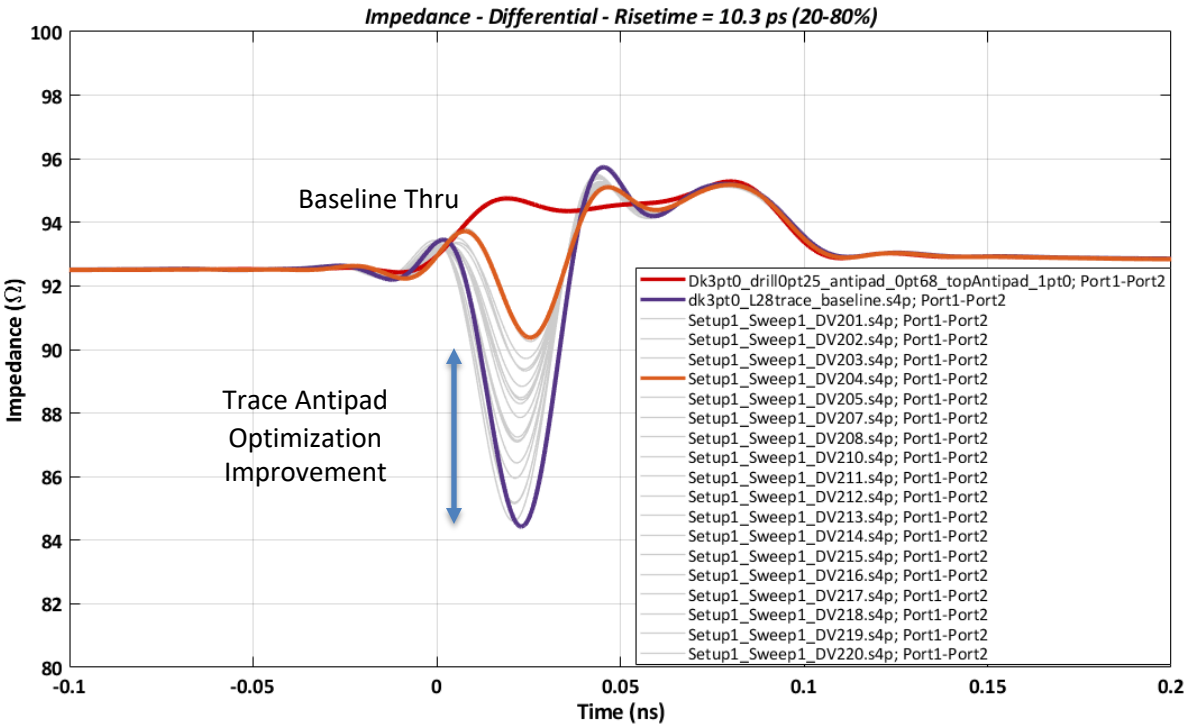


Optimized Trace Escape
Antipads Above and Below Trace Varied with Progressive Optimization from Original Thru Design



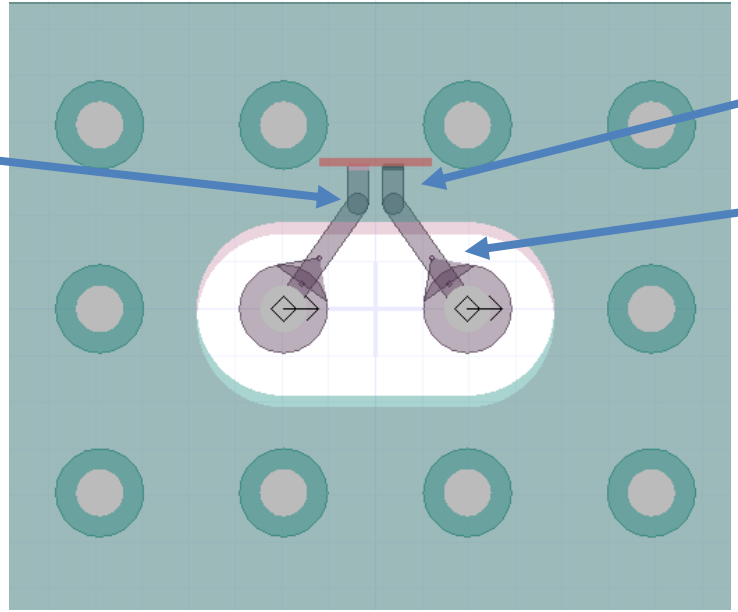


Optimized Trace Escape
Antipads Above and Below Trace Varied



Optimized BGA Launch
Trace Width/Pitch (4.5 / 7.6 mil)
Trace Antipad (0.94 mm), LowerAntipadOffset (0.06 mm)

Trace SE-to-Diff transition 0.1 mm after Antipad Crossing to accommodate manufacturing variation



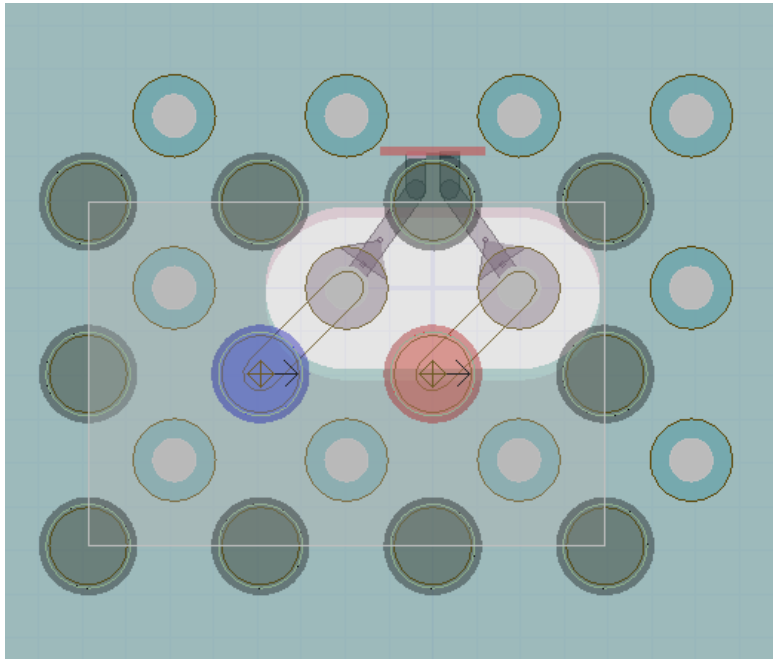
Trace geometry modified to Route through 1 mm via field

90-degree filet

Recap

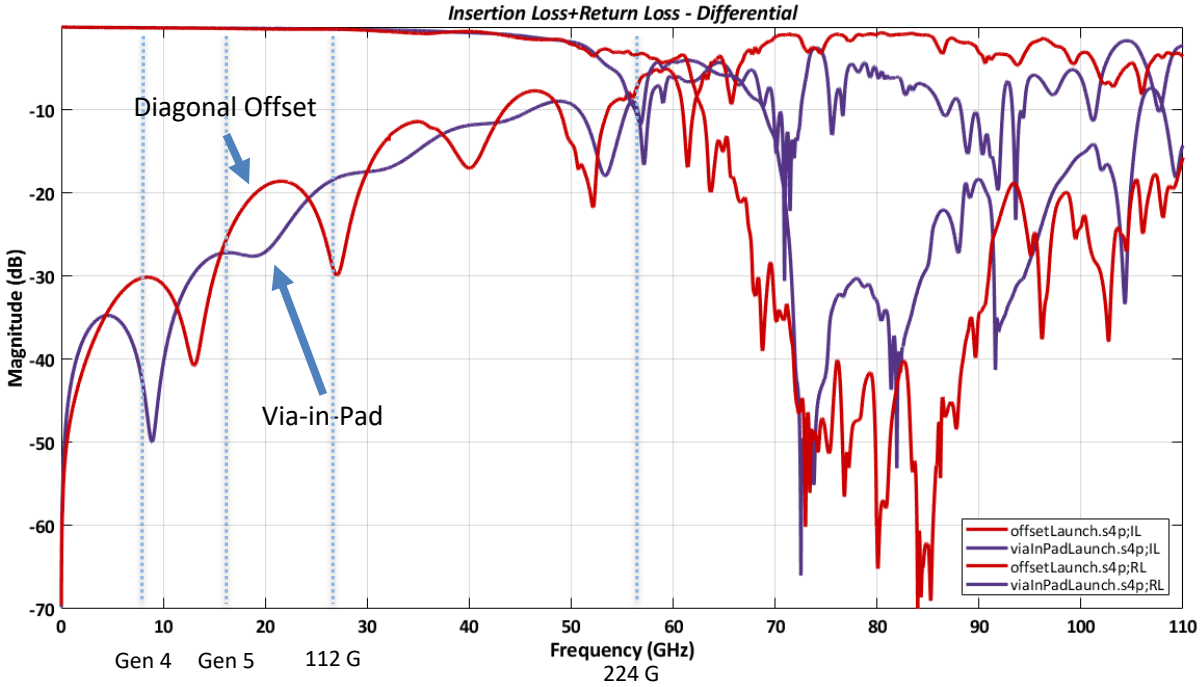
- **Simplified Theory of Periodically Loaded Transmission Lines**
- **Trace Design**
- **Zones of Control**
- **Step-by-Step near-optimal optimization process**
- **Step 1 – Create a thru design with launch on top and bottom.**
  - Signal Via Drill Size
  - Antipad Diameter for thick and thin plane layers.
  - Ground Via Drill Size (optional).
- **Step 2 – Create trace escapes on selected layers**
  - Optimize plane antipads above and below trace layers.
  - Fine tune via pitch.
  - Fine tune thick and thin plane antipad diameters.

Diagonal Offset Variant (Rapid Iteration)

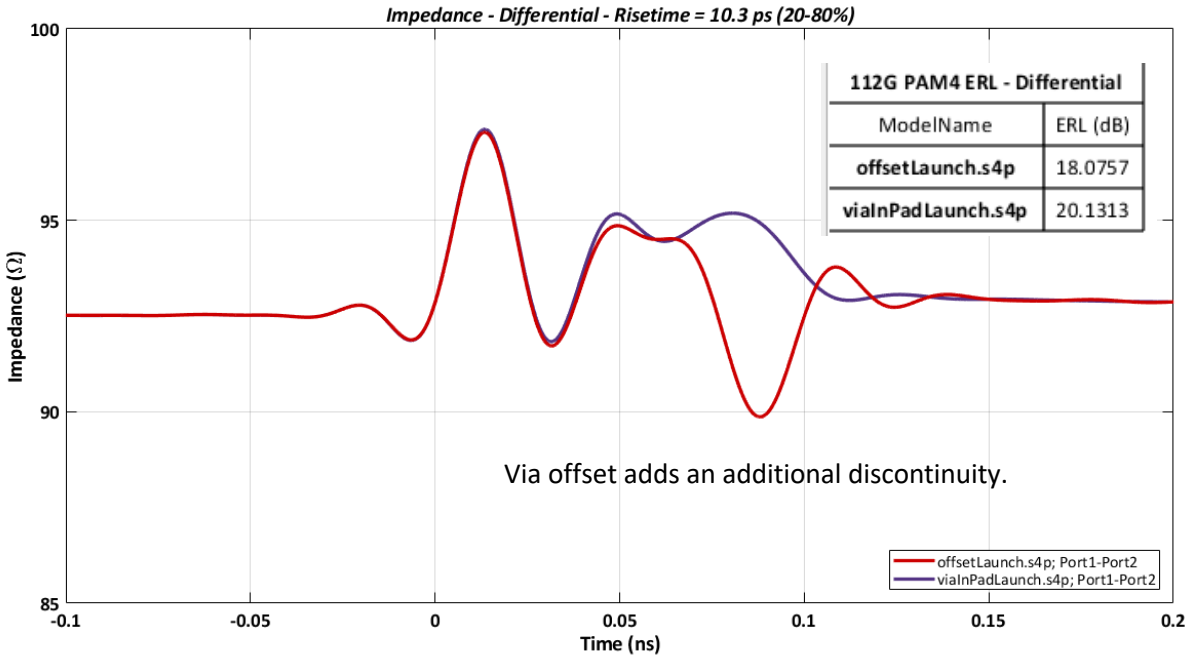


Vias offset from BGA pads by (0.5 mm, 0.5 mm)

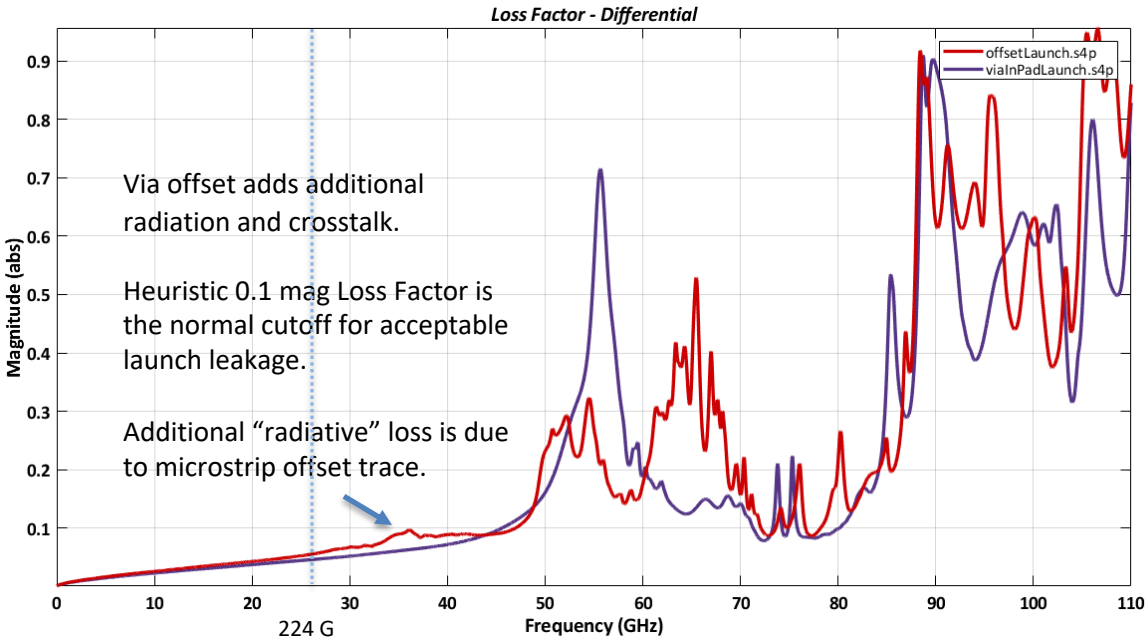
IL/RL Comparison without Further Optimization



112 GBPs TDR from Trace Side

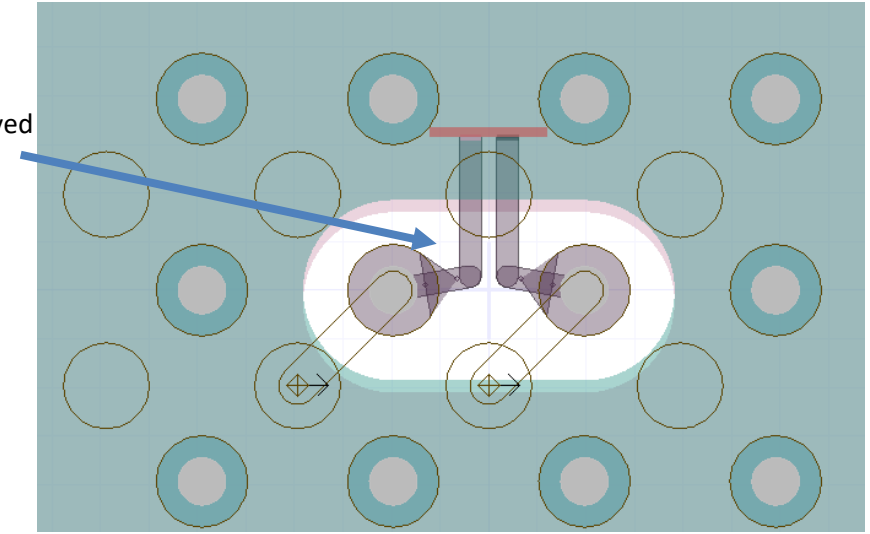


Loss Factor (1 – |S12|² x |S11|²)



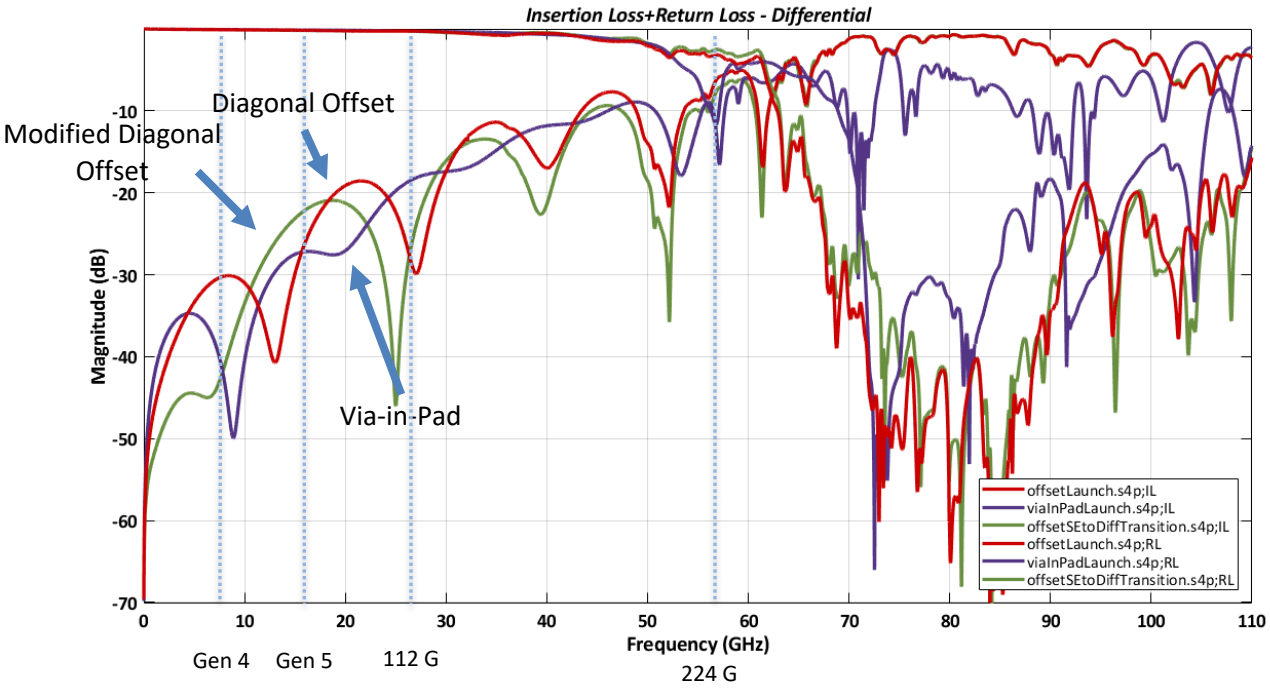
Diagonal Offset with Modified SE-to-Diff Transition (Rapid Iteration)

Trace SE-to-Diff transition moved closer to vias

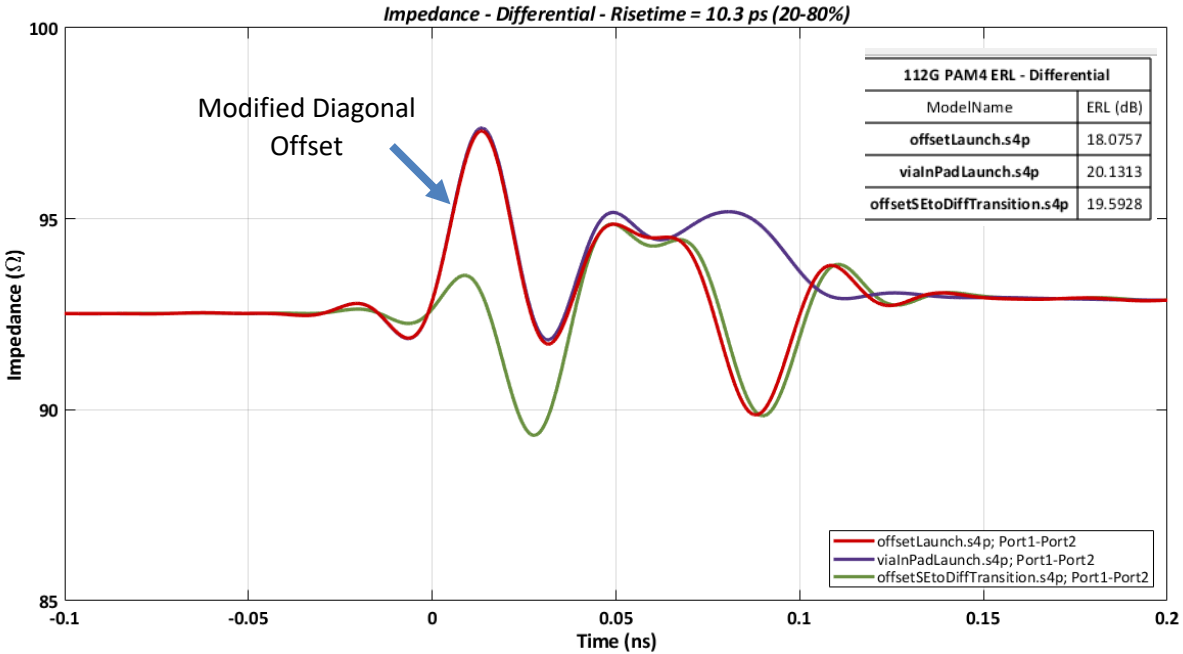


Vias offset from BGA pads by (0.5 mm, 0.5 mm)
Diff transition point placed within the antipad region

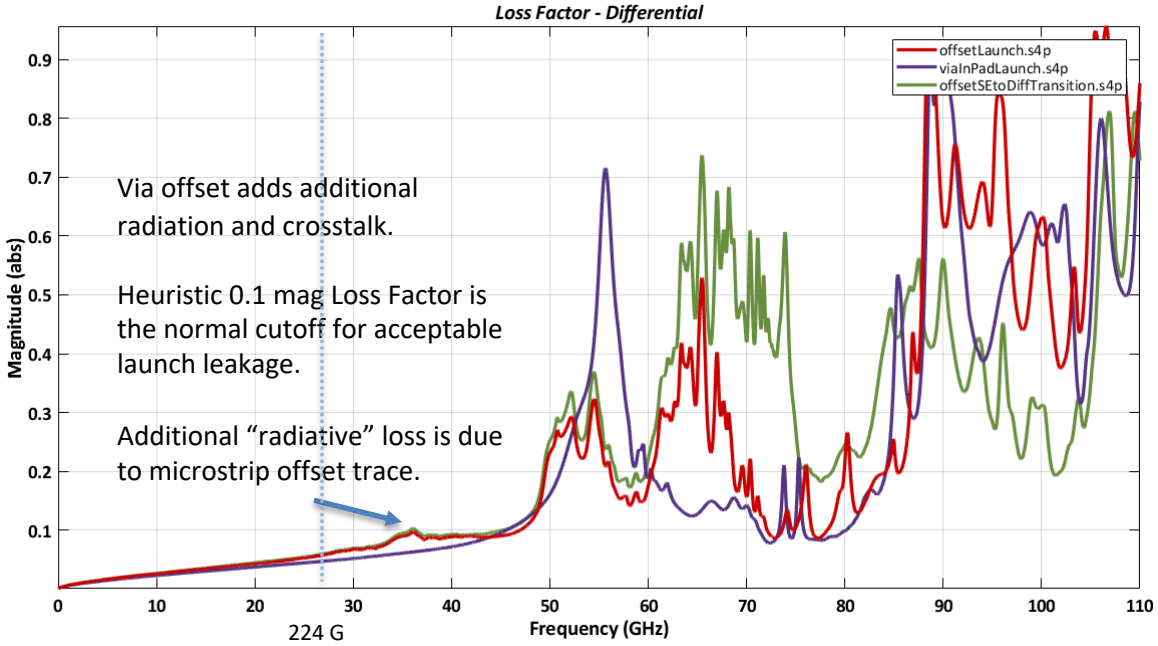
IL/RL Comparison without Further Optimization



112 GBPs TDR from Trace Side



Loss Factor (1 – |S12|² x |S11|²) Fast Proxy for Potential Crosstalk



Via offset adds additional radiation and crosstalk.

Heuristic 0.1 mag Loss Factor is the normal cutoff for acceptable launch leakage.

Additional "radiative" loss is due to microstrip offset trace.

Part 1 Summary

- **Simplified Theory of Periodically Loaded Transmission Lines**
- **Trace Design**
- **Zones of Control**
- **Step-by-Step near-optimal optimization process**
- **Step 1 – Create a thru design with launch on top and bottom.**
    - Signal Via Drill Size
    - Antipad Diameter for thick and thin plane layers.
    - Ground Via Drill Size (optional).
- **Step 2 – Create trace escapes on selected layers**
    - Optimize plane antipads above and below trace layers.
    - Fine tune via pitch.
    - Fine tune thick and thin plane antipad diameters.
- **Rapid Iteration of Design Variants (BOR Offset and SE-to-Diff Breakpoint)**
- **Loss Factor as Proxy for Crosstalk (Facilitates rapid evaluation, since no additional simulations required.)**
- **Thru and Trace Escape designs are computationally efficient (Fast to simulate with high accuracy.)**

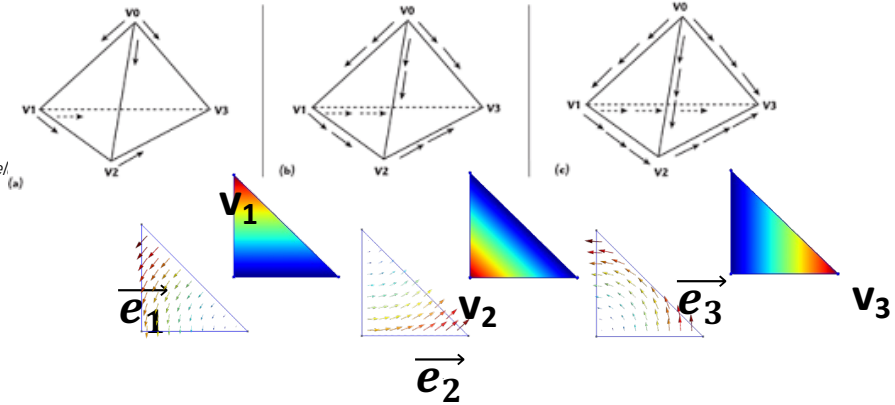
Interregnum: The Finite Element Method in Electromagnetics

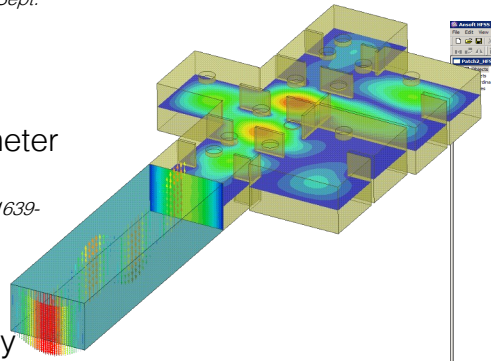
Background on the FEM Simulation Technique

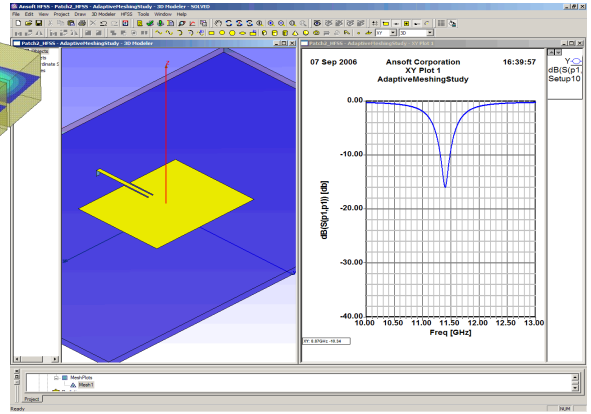
Discuss the finite element method and the key underlying technologies developed to enable it for 3D full-wave electromagnetic simulation and network (S,Y,Z) parameter extractions

Key Technologies for Electromagnetic FEM

- **Spurious Free Vector Basis Functions:**
  - Reliable FEM solutions of Maxwell's Equations
  - *M. L. Barton, Z. J. Cendes, "New vector finite elements for three-dimensional magnetic fiel computation", J. Appl. Phys., vol. 61, no. 8, pp. 3919-3921, 1987*
- **Automatic Adaptive Meshing:**
  - Accurate, efficient, and reliable results
  - *Z. J. Cendes and D.N. Shenton, "Adaptive mesh refinement in the finite element computation of magnetic field", IEEE Trans. Magn., vol. MAG-21, pp. 1811-1816, Sept. 1985*
- **Transfinite Element Method:**
  - Accurate and efficient extraction of S,Y,Z parameter
  - *Z. J. Cendes and J. F. Lee, "The transfinite element method for modelling MMIC devices", IEEE Trans. on Microwave Theory and Techniques, vol. 36, no. 12, pp. 1639-1649, December 1988*
- **Domain Decomposition Method:**
  - Distributed memory computing and key for many advanced solver features
  - *M. N. Vouvakis, Z. J. Cendes, and Jin-Fa Lee, "A FEM domain decomposition method for*







Some FEM Theory

- Maxwell's Equation, 2nd Order Vector Wave $\nabla \times \mu_r^{-1} \nabla \times \vec{E} - \left(\omega^2 / c^2\right) \varepsilon_r \vec{E} = -j\omega\mu_0 \vec{J}_{imp} \quad \Rightarrow \quad L\,\vec{E} = \vec{f}$
- The electric field is expanded in terms of basis functions:
  - The basis functions reside in finite elements such as tetrahedra
  - Residual of wave equation is non-zero due to approximation functions

$$\tilde{\vec{E}} = \sum_{j=1}^{N} \alpha_j \overrightarrow{W_j} \qquad r = L\,\tilde{\vec{E}} - \vec{f} \neq 0$$

- System of equations obtained by weighting residual with N testing functions:

$$R_i = \iiint_V \vec{W}_i \cdot \vec{r} = 0$$

$$A\,\mathbf{x} = \mathbf{b}$$

- Results in a matrix equation of the form…
  - Matrix A is sparse with the following entries:

$$A_{ij} = \iiint_V \nabla \times \vec{W}_i \mu_r^{-1} \nabla \times \vec{W}_j dV - \left(\omega^2 / c^2\right) \iiint_V \vec{W}_i \varepsilon_r \vec{W}_j dV + j\left(\frac{\omega}{c}\right)\left(\frac{\eta_0}{Z_s}\right) \iint_{IBC} \hat{n} \times \vec{W}_i \cdot \hat{n} \times \vec{W}_j dS$$

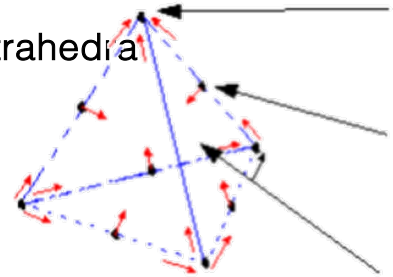
  - Impedance boundary, IBC, assumed on surfaces

$$\hat{n} \times \hat{n} \times \vec{E} = Z_s \hat{n} \times \vec{H}$$

    - *e.g., non-solve inside metals:*

Spurious Free Vector Basis Functions: Context

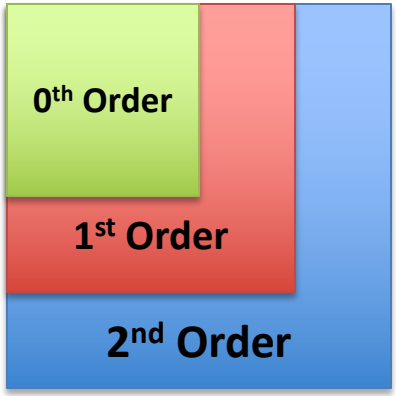
- Solving for electric field quantities at locations in the tetrahedra
- Element orders: 0th, 1st, 2nd, mixed
- The count starts at “0” because it is an H0 curl element
  - H stands for magnetic field
  - 1st order accurate in E
  - 0th order accurate in H due to taking derivative of E to compute H
  - Other solutions start order counting at 1st, causes some confusion
- **Element orders can be hierarchical**
  - Allows for mixed-order elements
  - Allows for hp refinement (size AND order)



The components of a field that are tangential to the edges of an element are explicitly stored at the vertices.

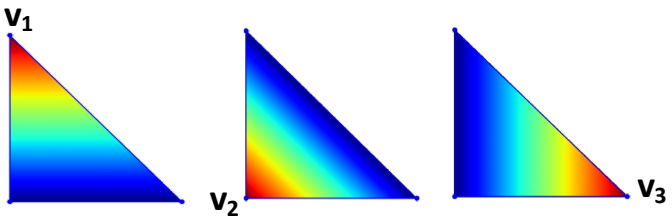
The component of a field that is tangential to the face of an element and normal to an edge is explicitly stored at the midpoint of selected edges.

The value of a vector field at an interior point is interpolated from the nodal values



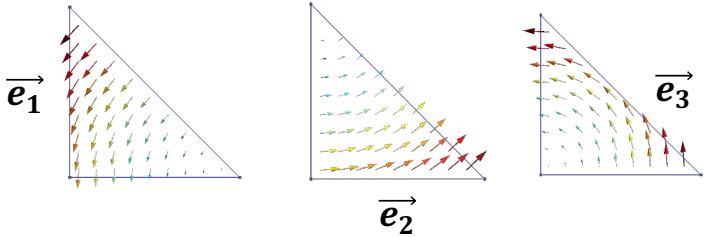
Spurious Free Vector Basis Functions

- Scalar Basis Functions
  - Vertex based where each basis function has one unknown coefficient for each field variable (ex,ey,ez)
  - Tangential and normal continuity of the electric field is enforced across elements
    - *But normal continuity of electric field* ***should not exist*** *across dielectric interfaces!*
    - *Results in unphysical spurious modes*
  - These issues caused FEM to be impractical as an industrial EM simulation method



$$\vec{E}(\vec{r}) = \sum_{i=0}^{n} \vec{e_i} v_i(\vec{r})$$

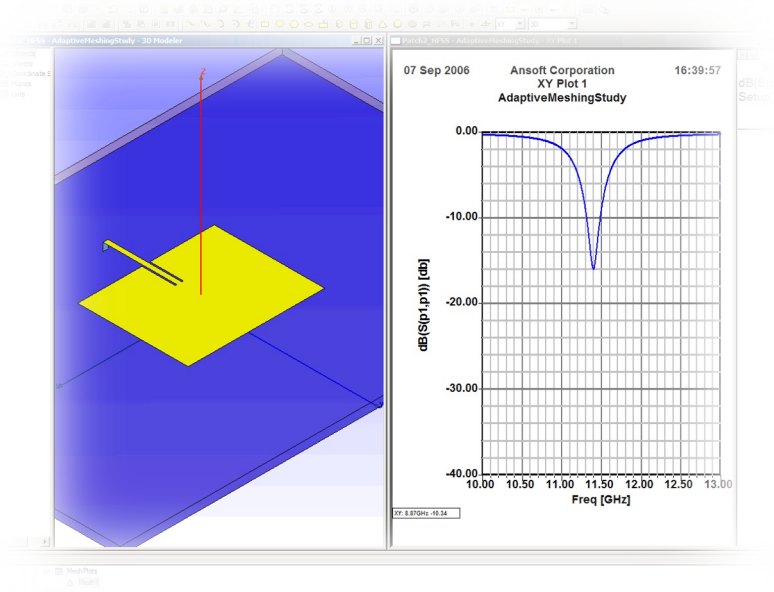
- Curl Confirming Vector Basis Functions
  - Edge based where each basis function has one unknown complex scalar coefficient
  - Only tangential continuity of the electric field is enforced across elements
  - Proper representation of the curl removes the spurious modes!
  - These improved basis functions made FEM practical as an industrial EM simulation method



$$\vec{E}(\vec{r}) = \sum_{i=0}^{n} \alpha_i \vec{e_i}(\vec{r})$$

Automatic Adaptive Meshing

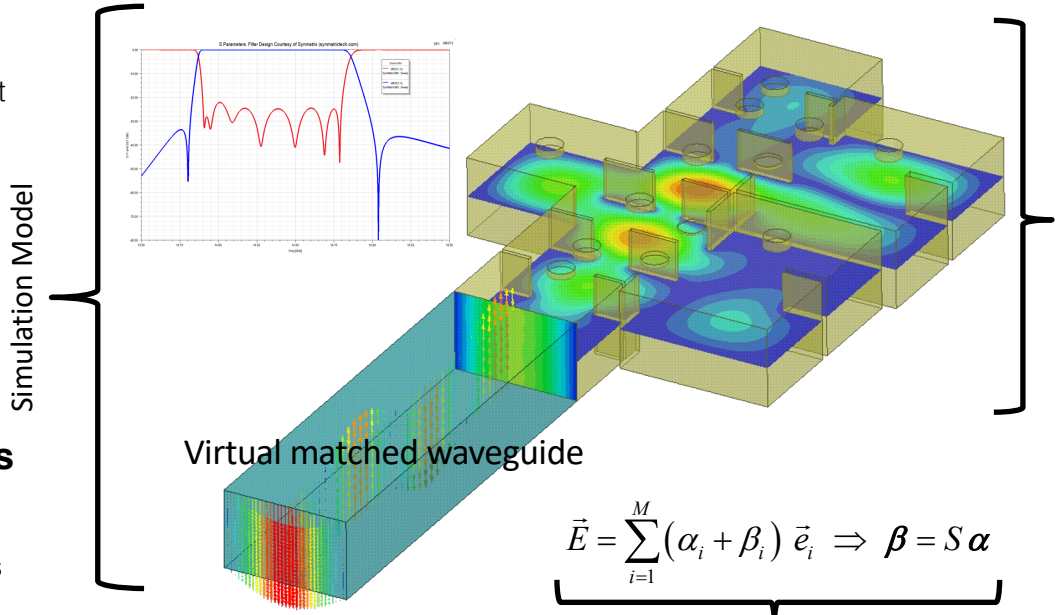
- Mesh is automatically adapted according to the electromagnetics
  - Removes burden of accurate mesh generation from the end-user
  - Technology is key for reliable accuracy
- Local error indicator drives the h and hp-refinement for optimal solution efficiency for desired level of accuracy
  - h-refinement selectively makes element size smaller
  - p-refinement selectively changes order of basis functions
  - hp-refinement selectively changes both order of basis functions and element size; aka, mixed order elements



- Refinement of patch antenna: Mesh refinement occurs in regions of highest strength and gradient of electric field, the perimeter of the patch antenna.

Transfinite Element Method

- **Transfinite Element Method**
  - Port modes are the basis functions on a port surface
  - Exact numerical port truncation
  - Yields very low noise floor with high computational efficiency
  - Is very efficient when only solving for S-parameters
- **Alternative Method: PML Backed Ports**
  - Less accurate
  - Less efficient with additional defined modes
  - Limited efficiency boost when only solving for S-parameters

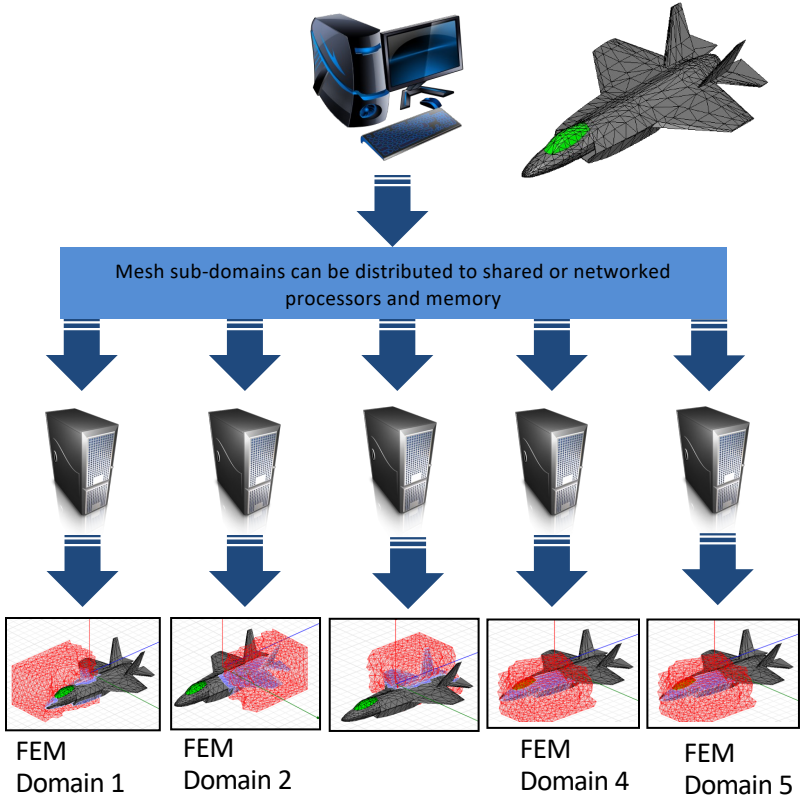


$$\vec{E} = \sum_{i=1}^{M} (\alpha_i + \beta_i)\, \vec{e}_i \;\Rightarrow\; \boldsymbol{\beta} = S\,\boldsymbol{\alpha}$$

Fields on port expanded in terms of Eigen Modes of waveguide:
- Each mode serves as a basis function on the port (accurate and efficient)
- By exciting the ith mode ($\alpha_j = \delta_{ij}$), solver obtains i^{th} column of S
- Additional modes come at a modest incremental cost in computational effort

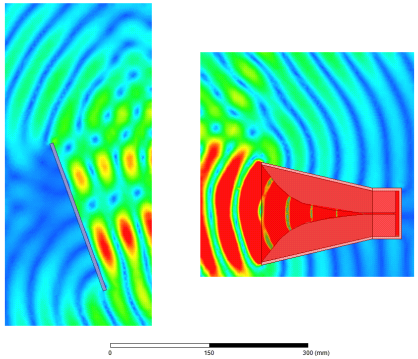
FEM Domain Decomposition Method, DDM

- **Domain Decomposition solver**
  - Efficient solution for electrically very large problems
  - Distributed memory: Large simulation clusters can be used to conquer huge designs
  - Rigorous: No simplified field coupling at interfaces
- **Automatic generation of domains by mesh partitioning**
- **Is a key technology baseline for more advanced solver technologies**

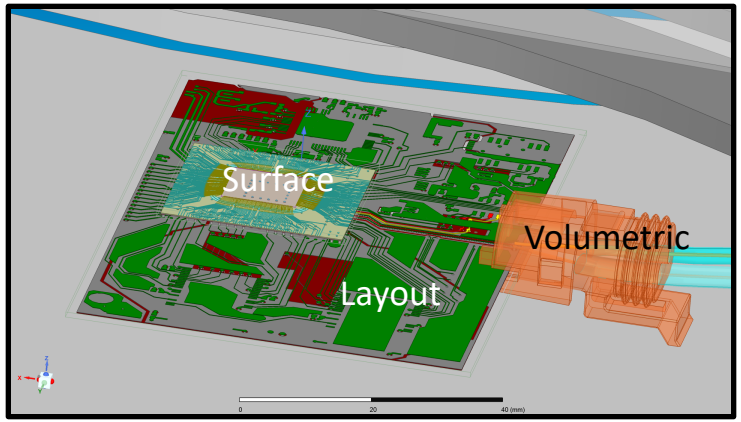


Advanced Solver Technology

- **Boundary Element/MoM Domains**
  - FE-BI Solver for Radiation/Scattering Projects
    - *Solves interior domain using FEM, exterior space using MoM*
    - *Enables a highly accurate and efficient solution for radiation*
  - IE (MoM) Regions
    - *Solve for objects in exterior space using MoM*
    - *Efficient for large metallic structures*
    - *Fully couples to FEM domains with FE-BI boundaries*
- **Mesh Fusion**
  - A breakthrough FEM solver technology
  - Regions meshed independently and in parallel
  - Mesh conformal to geometry, non-conformal at domain boundaries
  - Appropriate CAD-type mesh algorithm and units for each domain
  - Improves mesh success of multiscale assemblies
  - Requires non-conformal direct sparse matrix solver
  - Rigorous, matrix level, field coupling across domain interfaces

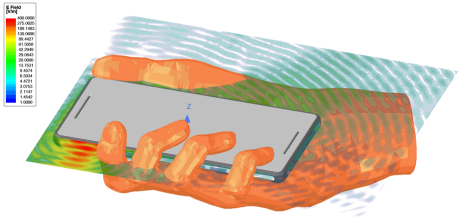


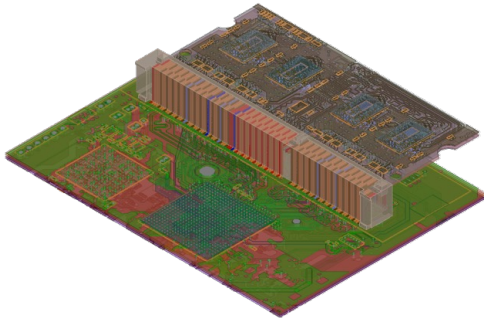
DDM foundational to both technologies



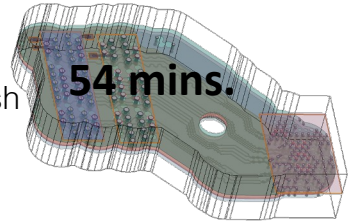
Evolving Simulation Techniques

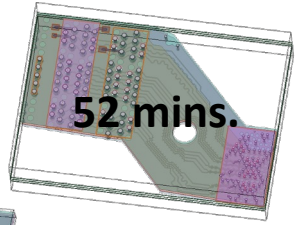
- **Platforms: 3D or Layout, pick the right one**
  - 3D if design is in mechanical CAD (MCAD)
  - Layout if design is in layout CAD (ECAD)
  - 3D Components can embed into Layout
  - Layout Components (new) can embed into 3D



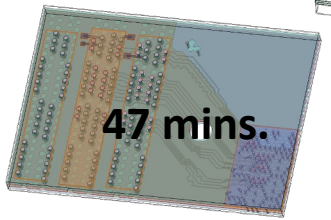


- **And Layout is 3D!**
  - Any difference in results is due to differences in CAD or mesh



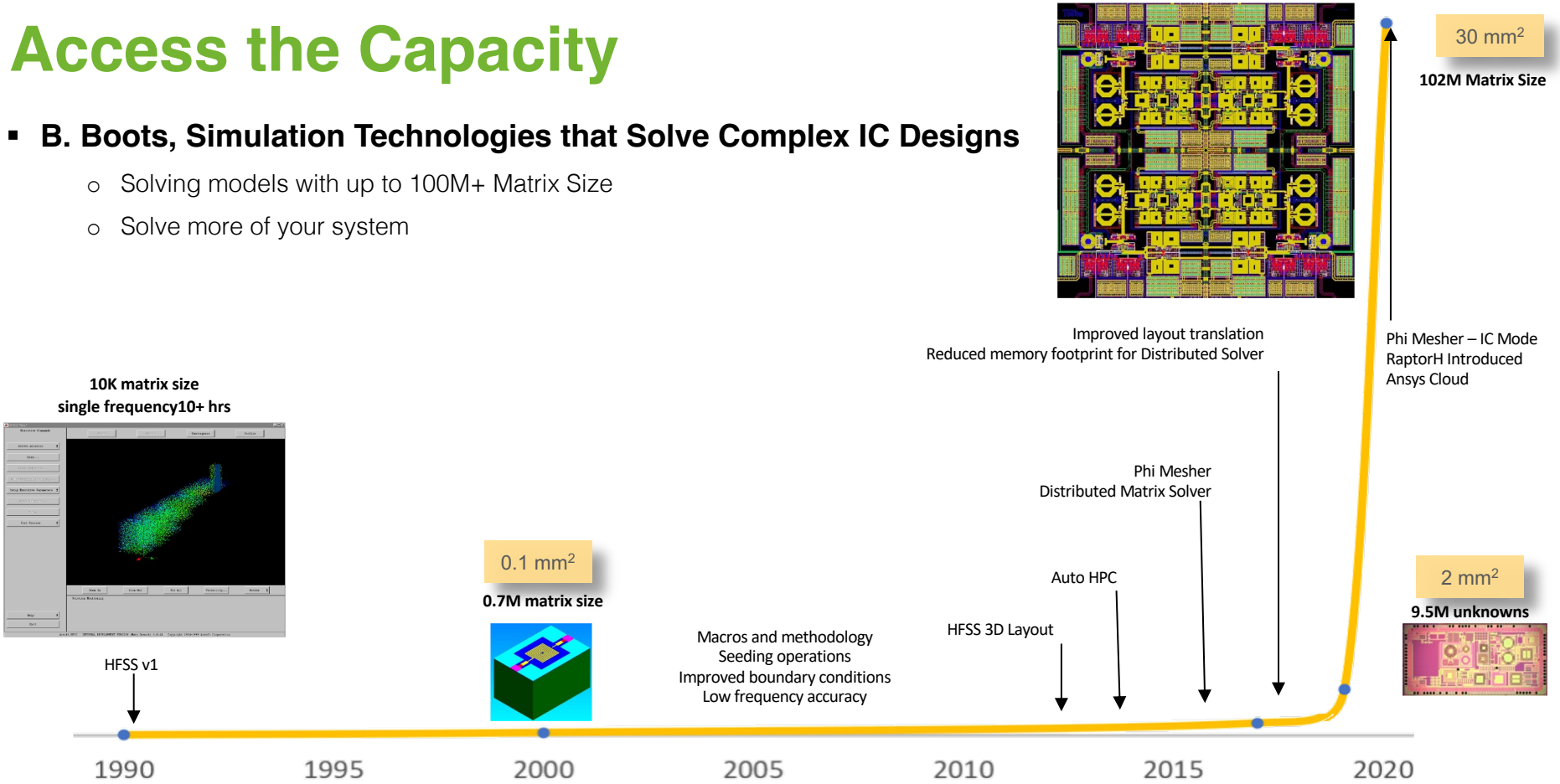


- **Cut out the Cutouts**
  - Smaller does not always mean faster
  - Simpler rectangular cutouts can solve as fast or faster with less uncertainty



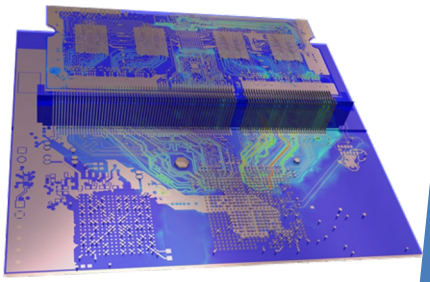
Access the Capacity

- **B. Boots, Simulation Technologies that Solve Complex IC Designs**
  - Solving models with up to 100M+ Matrix Size
  - Solve more of your system



Access the Capacity

- **B. Boots, Simulation Technologies that Solve Complex IC Designs**
  - Solving models with up to 100M+ Matrix Size
  - Solve more of your system
  - Push boundaries



800M

102M Matrix Size

Improved layout translation
Reduced memory footprint for Distributed Solver

Phi Mesher
Distributed Matrix Solver

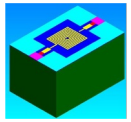
Auto HPC

HFSS 3D Layout

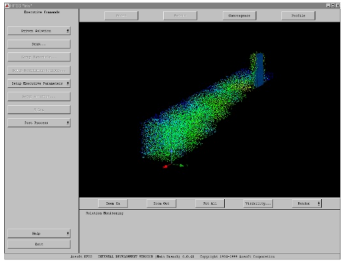
Macros and methodology
Seeding operations
Improved boundary conditions
Low frequency accuracy

0.7M Matrix size

0.1 mm^2



10K Matrix Size
single frequency10+ hrs



HFSS v1

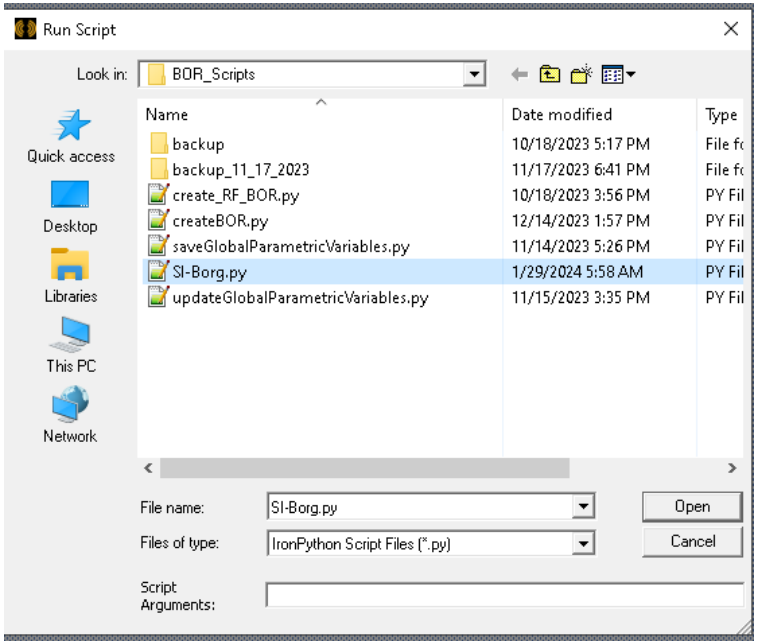
1990 1995 2000 2005 2010 2015 2020 2022

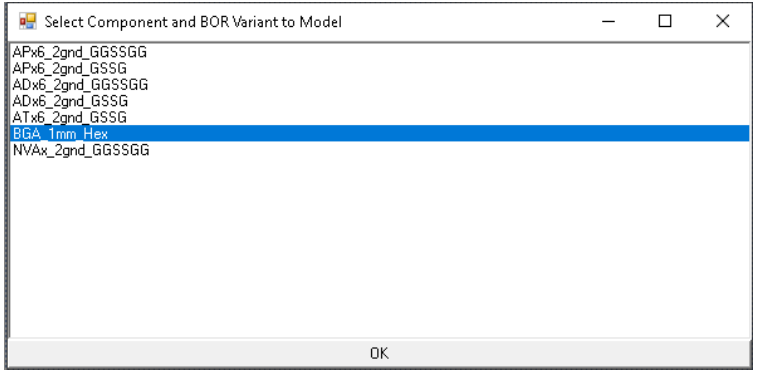
Part 2 – The Tool

SIBORG™
SIGNAL INTEGRITY BREAK OUT REGION GURU

Whereby We Show a Tool Which Can Be Used to Generate, Visualize, Optimize and Develop PCB Package and Component Launches

Launch Script and Choose Component





Select a Generic Stackup

Select a File

This PC › SIG (V:) › User › ScottM › Share › ProgrammableBOR › GenericStackups › programmableDielectricStackups

Organize ▾ New folder

PersonalLib
ADX6_2gnd_GGS
APX6_2gnd_GGS
ConfigurationTa
Network Drive (\
This PC
3D Objects
Desktop
Documents
Downloads
Music
Pictures
Videos
Local Disk (C:)
data (\\engr-1) (
sys1 (\\home1) (
Chicago Cluster
Chicago Cluster
ECAD Library (O
TestLab Electrica

Name	Date modified	Type	Size
4-Layer_ProgrammableDielectricStackup.xml	5/11/2023 11:20 AM	XML File	2 KB
6-Layer_ProgrammableDielectricStackup.xml	5/11/2023 11:20 AM	XML File	2 KB
8-Layer_ProgrammableDielectricStackup.xml	5/11/2023 11:20 AM	XML File	3 KB
10-Layer_ProgrammableDielectricStackup.xml	5/8/2023 7:05 PM	XML File	3 KB
12-Layer_ProgrammableDielectricStackup.xml	5/10/2023 3:30 PM	XML File	4 KB
14-Layer_ProgrammableDielectricStackup.xml	5/11/2023 11:20 AM	XML File	4 KB
16-Layer_ProgrammableDielectricStackup.xml	5/11/2023 11:20 AM	XML File	5 KB
18-Layer_ProgrammableDielectricStackup.xml	5/11/2023 11:20 AM	XML File	5 KB
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24-Layer_ProgrammableDielectricStackup.xml	5/11/2023 11:20 AM	XML File	7 KB
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38-Layer_ProgrammableDielectricStackup.xml	10/5/2023 1:32 PM	XML File	11 KB
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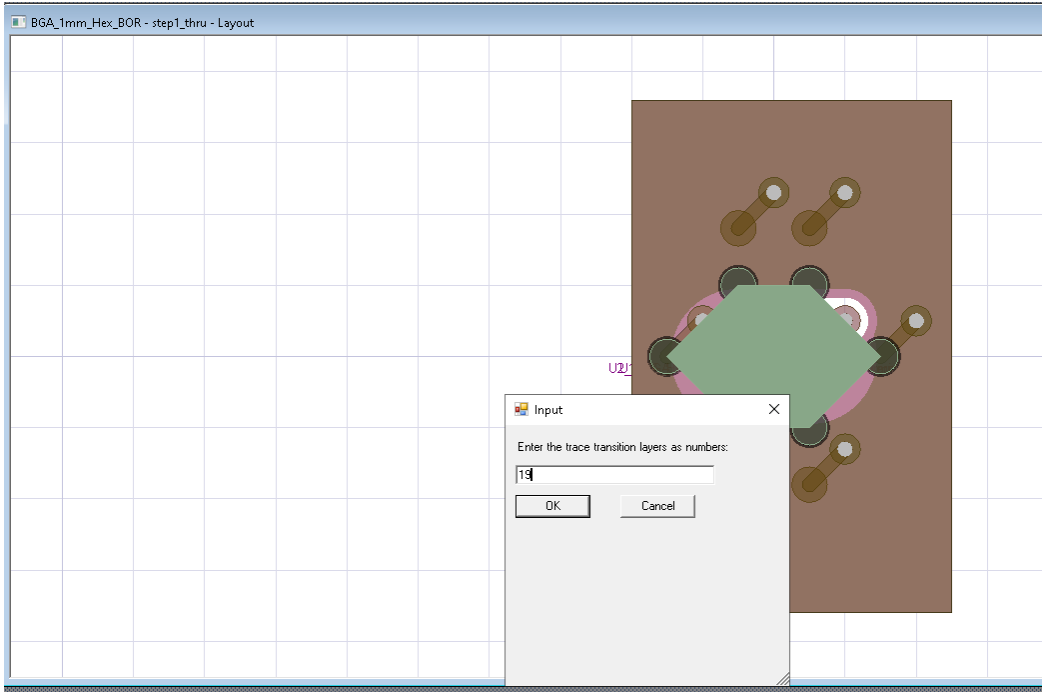
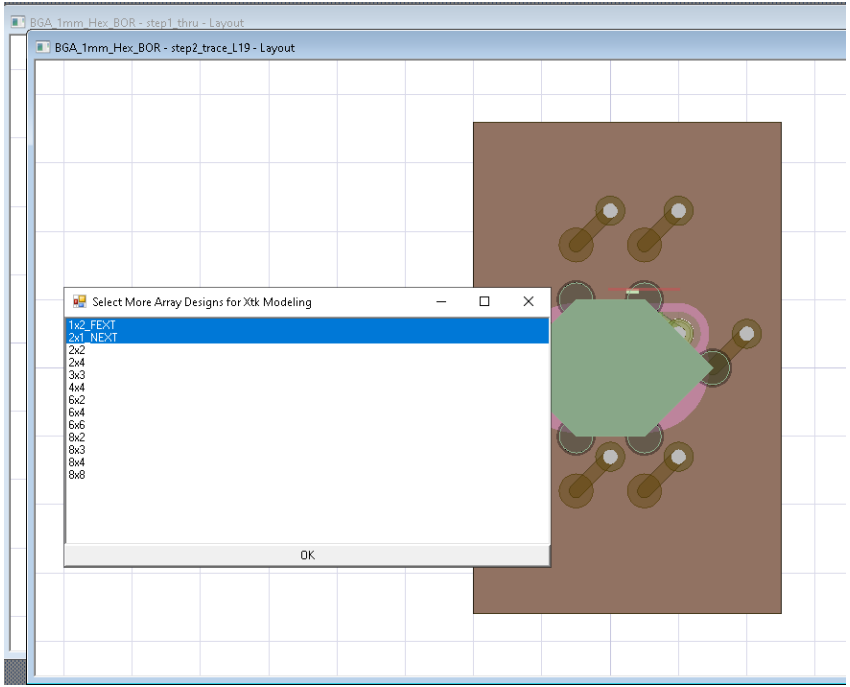
42-Layer_ProgrammableDielectricStackup.xml	10/5/2023 1:36 PM	XML File	12 KB
frog.xml	10/9/2023 2:01 PM	XML File	4 KB

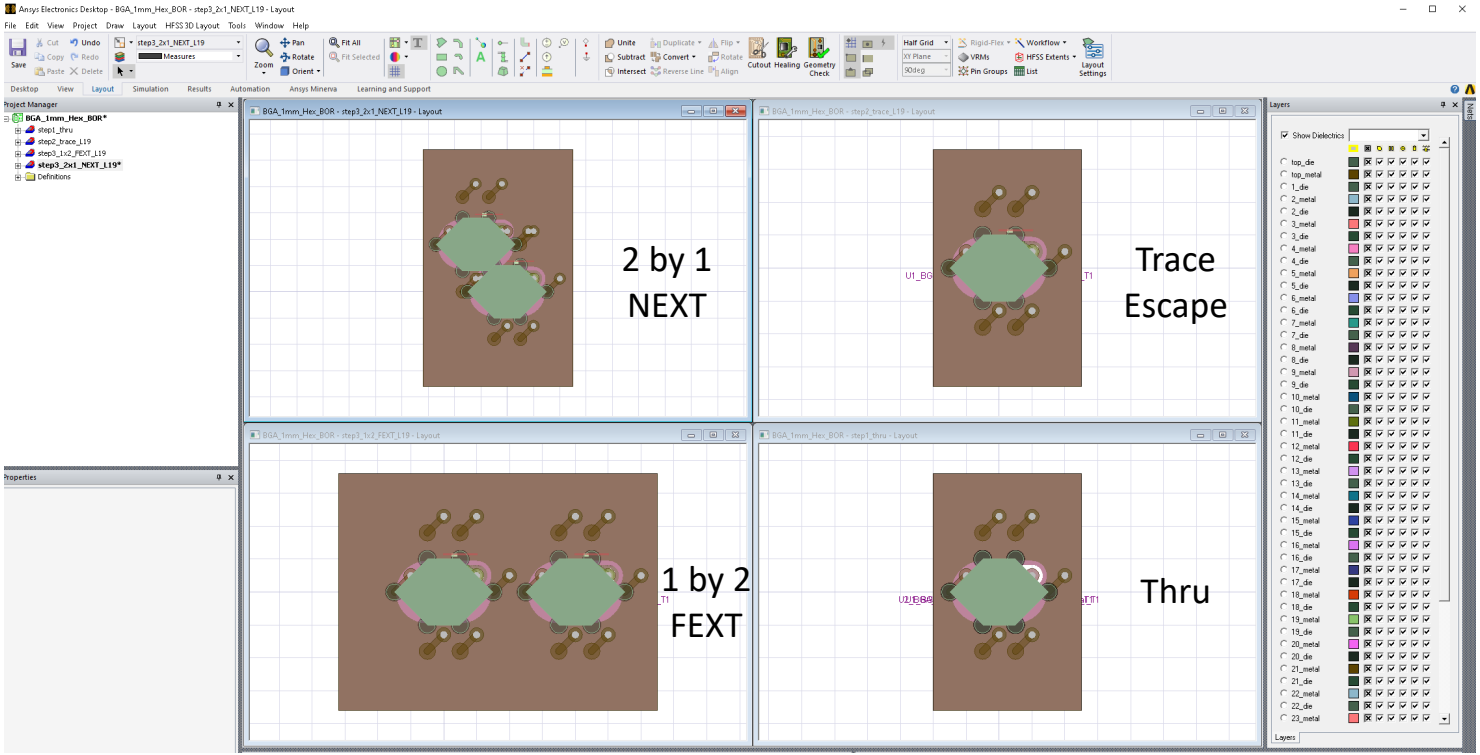
Enter Trace Transition Layer(s)



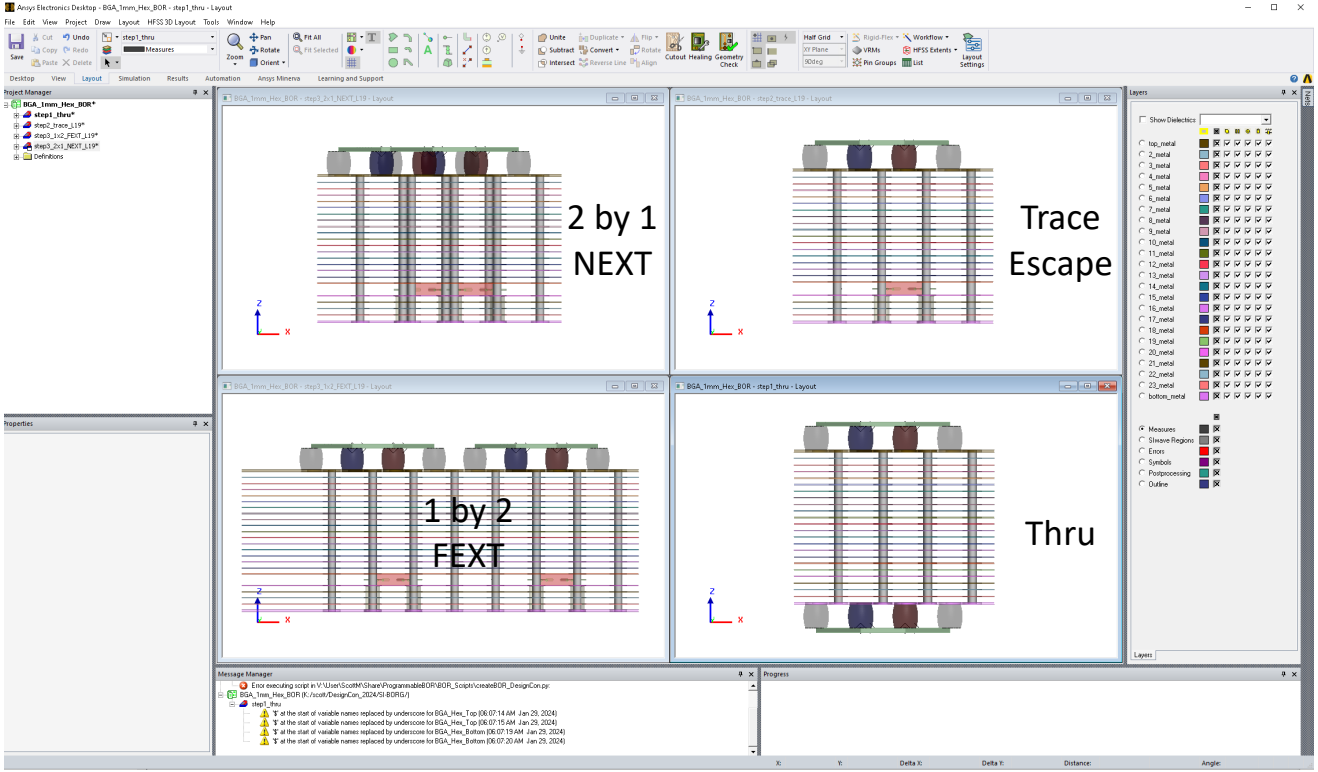
Select Additional Arrays for Routing and Crosstalk Evaluation



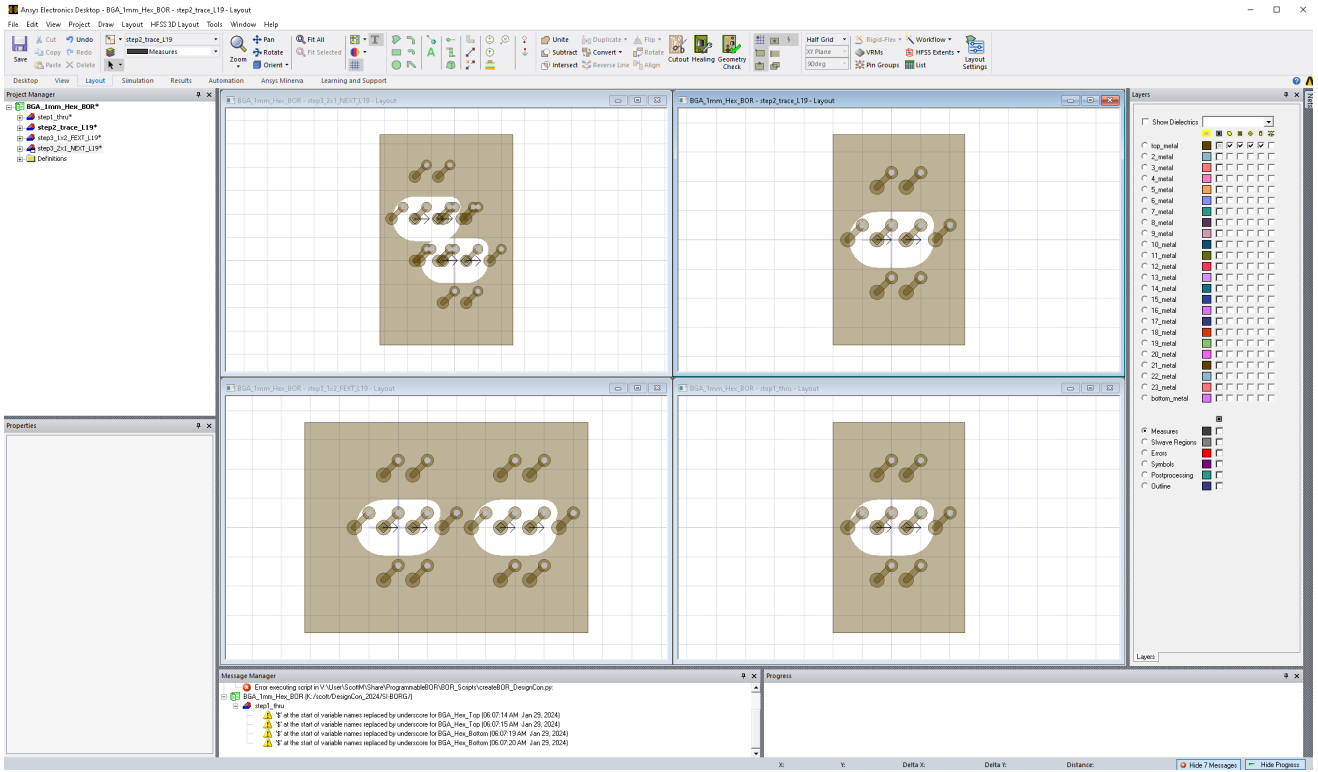
Generated Designs – Top View



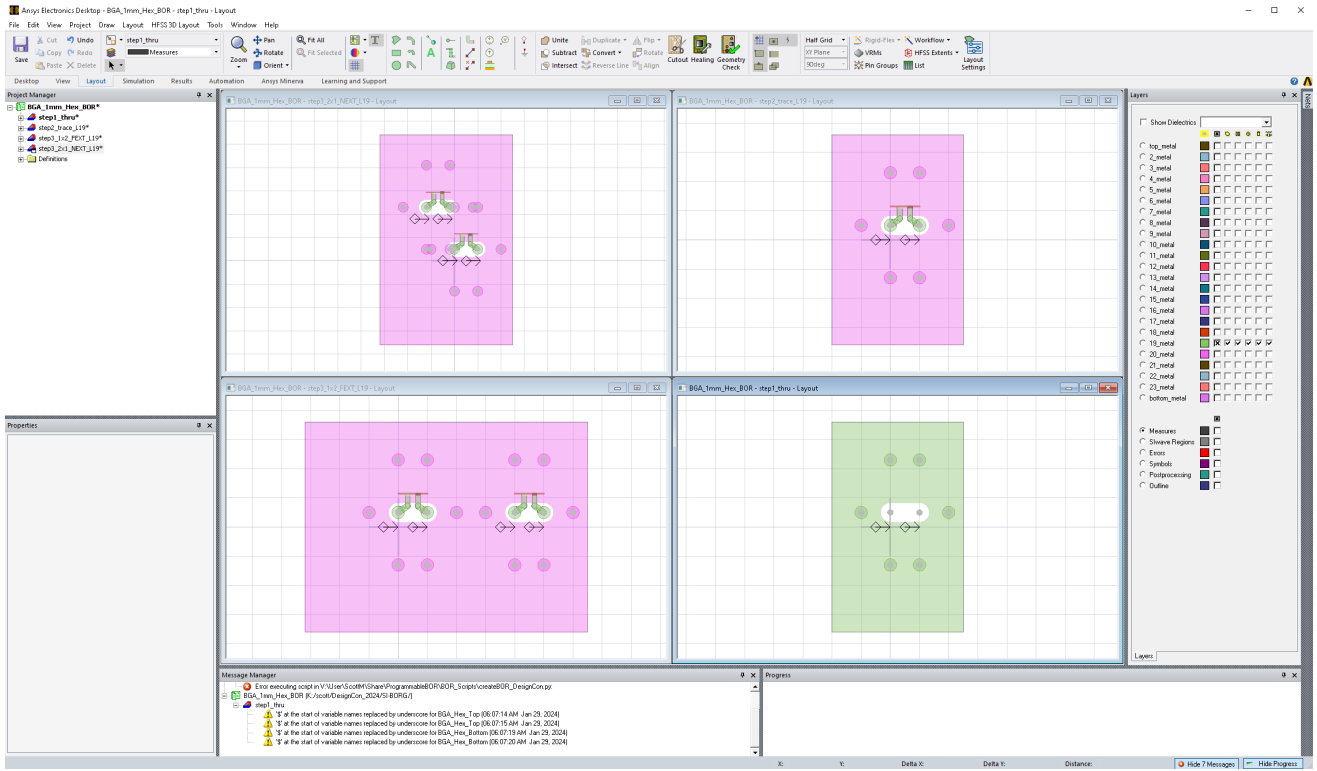
Generated Designs - Side View



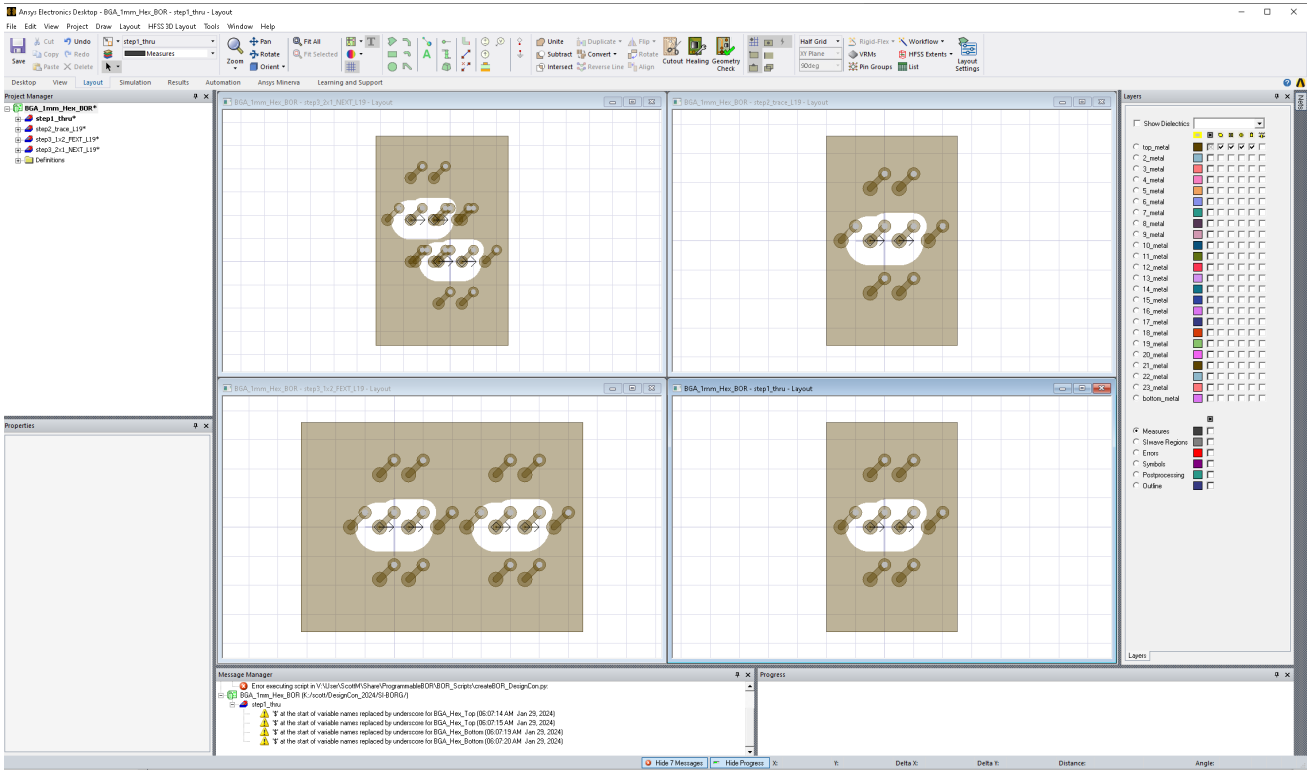
Generated Design - Top Layer



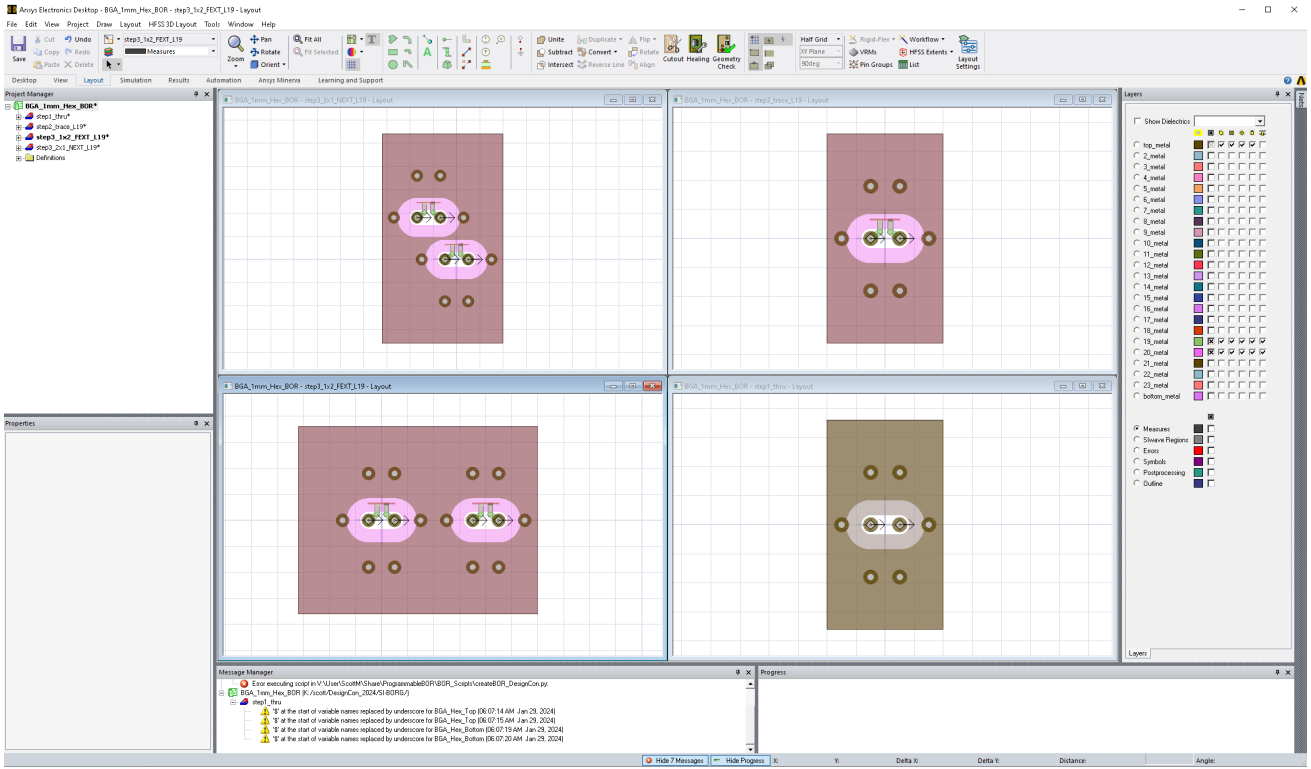
Generated Design – Trace Escape Layer



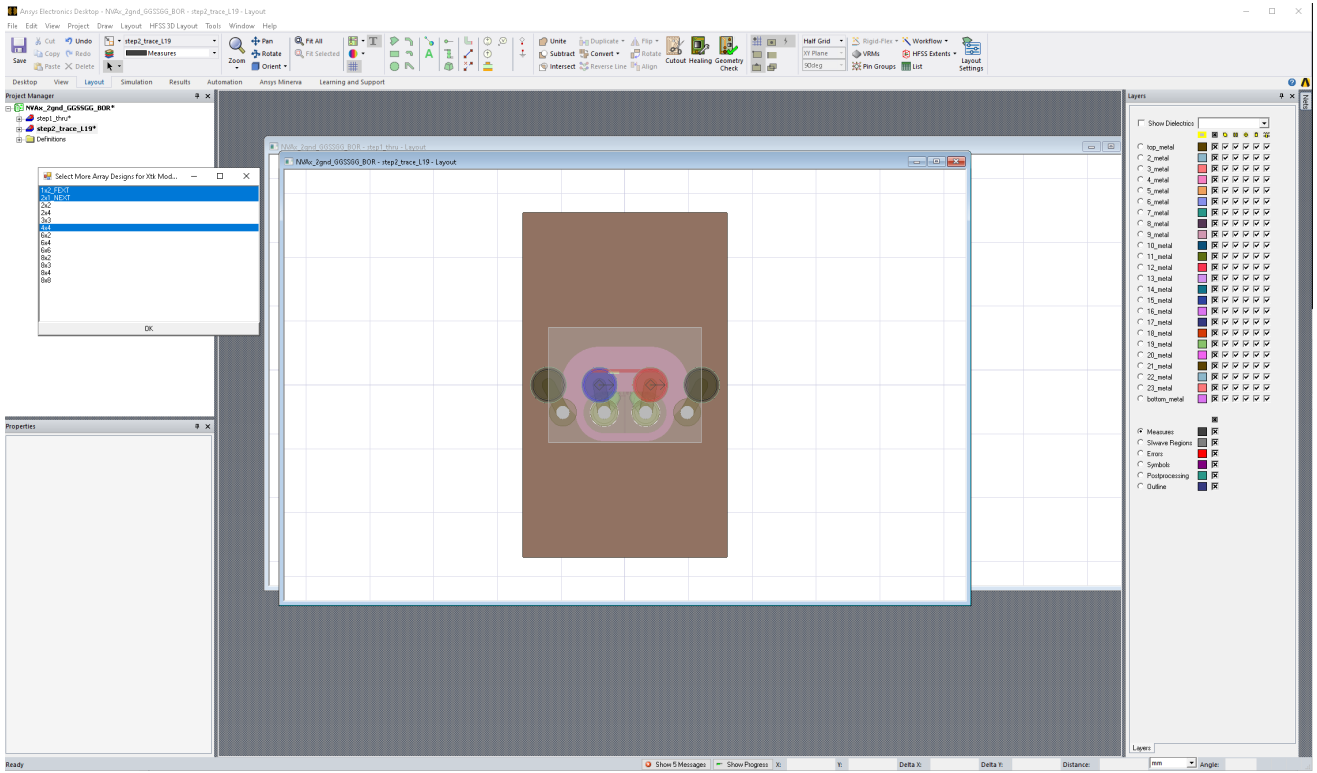
Rapidly Modify Top Ball Antipad



Rapidly Render Via-in-Pad Design



Generate NovaRay Design (FEXT, NEXT, 4x4)



Dielectric Variables

Name	Value	Unit	Evaluated Value	Description
Anisotropic_Dielectric_Variables				
$Dk	3		3	Dk for programmable djordjevic-sarkar dielectric to replace materials in design. Use average of prepreg/core
$Df	0.0023		0.0023	Df for programmable djordjevic-sarkar dielectric to replace materials in design. Use average of prepreg/core
$DS_XYcorrection	1.12		1.12	Anisotropic correction factor for layered dielectric in XY-axis direction.
$DS_Zcorrection	0.9625		0.9625	Anisotropic correction factor for layered dielectric in Z-axis direction.
$DS_measFreq	1000000000		1e+09	Measured Frequency for Djordjevic-Sarkar model

PCB Manufacturing Variables

PCB_Manufacturing_Variables				
$backdrillOversize	6	mil	6mil	Backdrill Drill Size = $viaDiameter_SigVia + $backdrillOversize
$backdrillStub	6	mil	6mil	Nominal Backdrill stub from Trace layer (4 mil +/- 2 mil)
$minAnnularClearance	0.1	mm	0.1mm	Manufacturing clearance between pad and pad or trace
$minimumViaClearance	10	mil	10mil	Manufacturing via barrel-to-barrel clearance for placing ground vias adjacent to each other
$padAnnularRing	0.115	mm	0.115mm	Manufacturing pad annular ring around via. (standard 0.115mm, advanced 0.090mm, developmental 0.076mm)

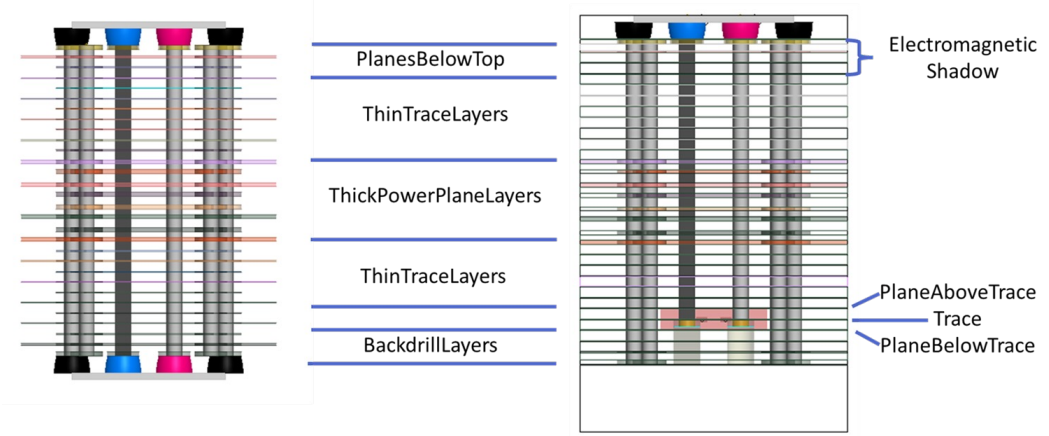
BGA Pad Geometry Variables

BGA_Pad_Geometry_Variables				
$bgaGndPitch	0.8	mm	0.8mm	Center-to-center pitch between ground ball and signal ball
$bgaSigPitch	0.8	mm	0.8mm	Center-to-Center pitch between signal balls.
$padDiameter_BGA	0.45	mm	0.45mm	NVAx BGA Pad Diameter defined by manufacturer

Via Geometry Variables

Via_Geometry_Variables				
$viaDiameter_GndStitchVia	0.2	mm	0.2mm	Ground Stitch Via Drill Diameter (0.15mm,0.18mm,0.2mm,0.225mm,0.25mm,0.3mm
$viaDiameter_GndVia	0.2	mm	0.2mm	Ground Via Drill Diameter (0.15mm,0.18mm,0.2mm,0.225mm,0.25mm,0.3mm
$viaDiameter_SigVia	0.2	mm	0.2mm	Signal Via Drill Diameter (0.15mm,0.18mm,0.2mm,0.225mm,0.25mm,0.3mm
$padDiameter_GndStitchVia	$viaDiame...		0.43mm	Ground Vias that are not incorporated into BGA component pad
$padDiameter_GndVia	$viaDiame...		0.43mm	gnd via Pad Diameter
$padDiameter_SigVia	$viaDiame...		0.43mm	Via in BGA signalPad via diameter + 2 x 0.115 mm (0.115 = 4.5 mil annular ring)
$antiPad_Backdrill	$viaDiame...		0.4524mm	Antipad around backdrill
$backdrillDiameter	$viaDiame...		0.3524mm	Calculated Backdrill drill size based on $viaDiameter_SigVia+$backdrillOversize
$gndViaInLineOffset	$viaDiame...		0.454mm	calculation for minimum DFM center-to-center via-to-via clearance on the same net. For example ground vias.
$viaMetalConductivity	5300000		5300000	Used to define lower conductivity via plating.

Antipad Sizing Variables



Antipad_Sizing_Variables				
$antiPad_TopLaunch	1.2	mm	1.2mm	Antipad for Top BGA pads
$antiPad_BelowTopLaunch	0.9	mm	0.9mm	Antipad Below the top of the board
$antiPad_ThinTraceLayers	0.65	mm	0.65mm	Antipad for thin signal routing layer signal and ground metal
$antiPad_ThickPlanes	0.85	mm	0.85mm	Antipad for Power/Ground Planes with thick metal
$antiPad_AboveTrace	0.65	mm	0.65mm	Antipad in plane above trace layer
$antiPad_BelowTrace	0.65	mm	0.65mm	Antipad in plane below trace layer
$antiPad_BelowTrace_Offset	0	mm	0mm	Shift antipad under trace to provide more continuous ground on exit

Trace Geometry Variables

Trace_Geometry_Variables				
$diffPitch	14	mil	14mil	Differential Signal Trace Pitch (0.36 mm = 14.17 mil for 1067 fiberglass weave)
$diffTraceWidth	0.17	mm	0.17mm	Trace width for differentially coupled traces
$seTraceWidth	0.2	mm	0.2mm	Obvious
$rowPairPitch	3*$bgaGn...		3.2mm	center-to-center Pitch between differential pairs in-row

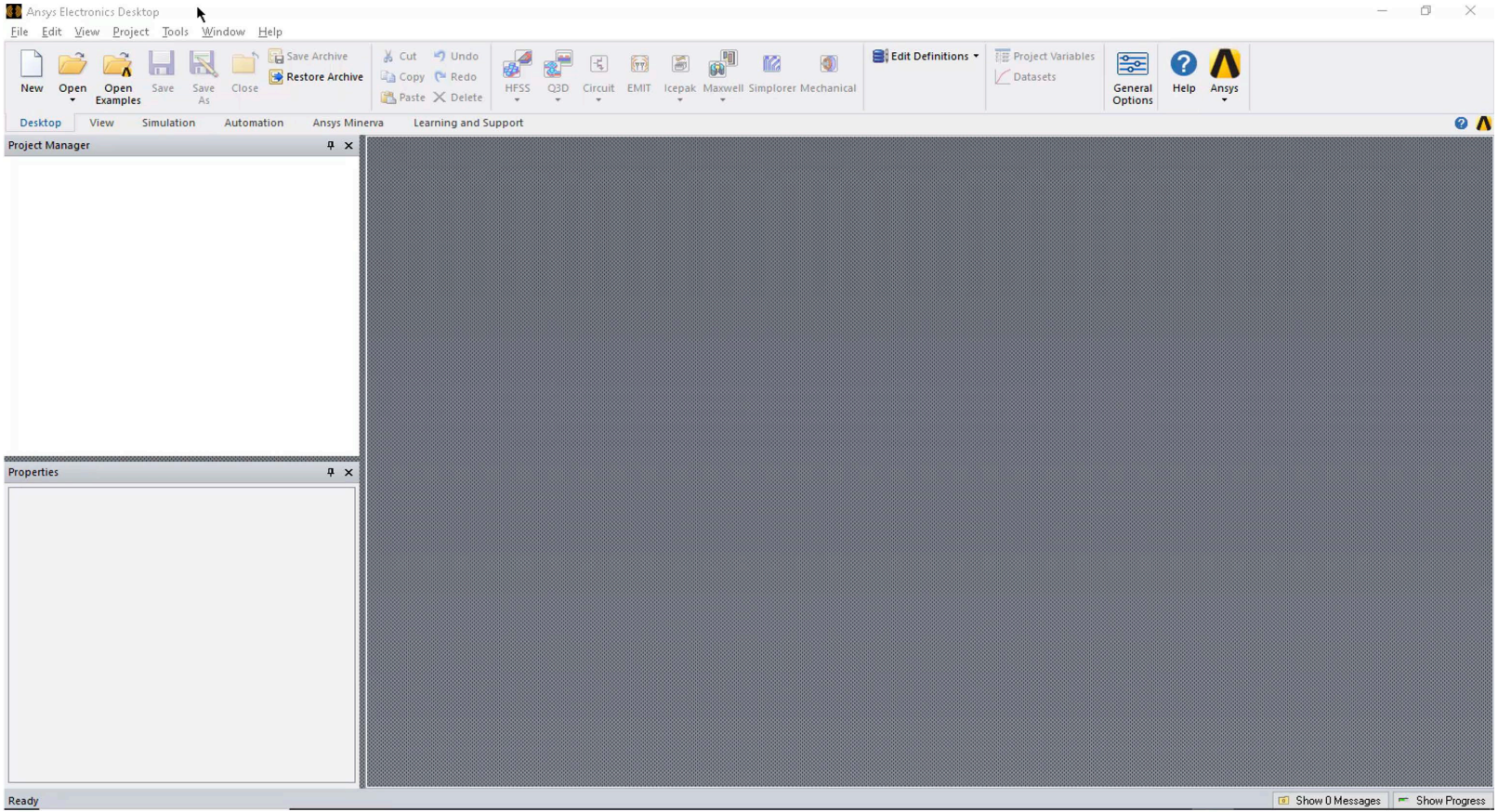
Launch Geometry Variables

Launch_Geometry_Variables				
$launchGndPitch	0.65	mm	0.65mm	Center-to-center pitch between ground via and signal via
$launchSigPitch	0.65	mm	0.65mm	Center-to-Center pitch between signal vias
$launchYOffset	0.43	mm	0.43mm	Y-axis Breakout Offset of BGA pattern from signal and ground vias for offset launch
$launchXOffsetOddColumn	0	mm	0mm	X-axis Breakout Offset of BGA pattern from signal and ground vias for offset launch
$launchXOffsetEvenColumn	0	mm	0mm	X-axis Breakout Offset of BGA pattern from signal and ground vias for offset launch
$se_to_diff_transitionPoint	-0.1	mm	-0.1mm	used to move the diff transition to a point before or after the antipad crossing

BOR Array Generation Variables

BOR_Array_Generation_Variables				
$rowXOffset_Even	-1.2	mm	-1.2mm	XOffset of pair placement on Even rows
$rowXOffset_Odd	0	mm	0mm	XOffset of pair placement on odd rows
$rowSpace_0to1	1.8	mm	1.8mm	location of second row
$rowSpace_0to2	3.6	mm	3.6mm	location of third row
$direction_allNorth	[1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, ...		[1, 1, 1, 1, 1, 1, ...	-1 = breakout to the South. 1 = breakout to the north, Other values will scale at the $launchYOffset value
$direction_allSouth	[-1, -1, -1, -1, -1, -1, -1, -1, -1, -1, -1,...		[-1, -1, -1, -1, -1,...	-1 = breakout to the South
$direction_South_North_byRow	[-1, -1, -1, -1, -1, -1, -1, -1, 1, 1, 1, ...		[-1, -1, -1, -1, -1,...	-1 = breakout to the South
$direction_South_South_North_North_byRow	[-1, -1, -1, -1, -1, -1, -1, -1, -1, -1, -1,...		[-1, -1, -1, -1, -1,...	-1 = breakout to the South
$direction_North_North_South_South_byRow	[1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, ...		[1, 1, 1, 1, 1, 1, ...	-1 = breakout to the South
$direction_North_South_byRow	[1, 1, 1, 1, 1, 1, 1, 1, -1, -1, -1, -...		[1, 1, 1, 1, 1, 1, ...	-1 = breakout to the South
$direction_North_South_byColumn	[1, -1, 1, -1, 1, -1, 1, -1, 1, -1, 1, ...		[1, -1, 1, -1, 1, -...	-1 = breakout to the South
$direction_South_North_byColumn	[-1, 1, -1, 1, -1, 1, -1, 1, -1, 1, -1,...		[-1, 1, -1, 1, -1, ...	-1 = breakout to the South
$breakoutDirection	$direction_South_South_North...		[-1, -1, -1, -1, -1,...	Breakout Direction Vector
$routingDirection	$direction_allNorth		[1, 1, 1, 1, 1, 1, ...	Breakout Direction Vector

Embedded video included. To view, download file to desktop then open with Adobe Acrobat. No audio included.



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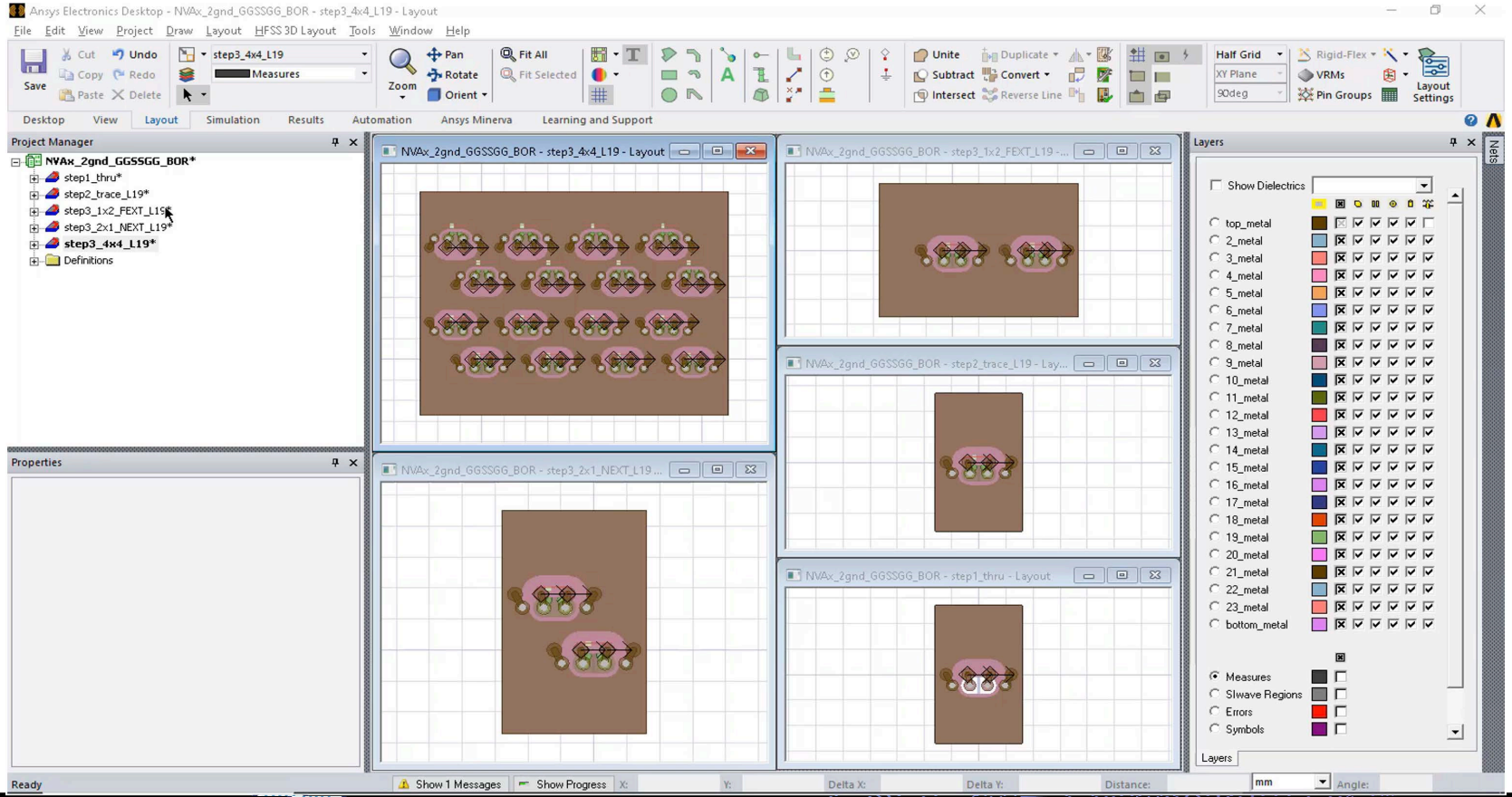

Thank you!

QUESTIONS?