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Bridging the Time-Frequency Chasm in PDN Design: Leveraging Cumulative Power-Rail Noise and Reverse Pulse Techniques for Spatial-Frequency Insight

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Kristoffer Skytte (Cadence), Shirin Farrahi (Marvell),
Abe Hartman (Oracle), John Phillips (Cadence),
Mario Rotigni (Retired), Istvan Novak (Samtec)

SPEAKERS

Ethan Koether

Sr. Signal and Power Integrity Engineer, Amazon Leo

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Ethan Koether earned his master's degree in EECS in 2014 from MIT then spent seven years as a hardware engineer at Oracle. He then joined Leo as a Sr. SIPI engineer. His interests are in commercial power solutions and power distribution network design, measurement, and analysis.

SPEAKERS

Kristoffer Skytte

Application Engineer Architect, Cadence

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Kristoffer Skytte has 20 years experience working on chip, package, board and full system analysis including SI, PI, thermal, and EMC challenges. His recent efforts are on examining differences between measurement and simulation. He holds an M.Sc.EE. degree from the Technical University of Denmark.

John Phillips

Sr. Principal Application Engineer, Cadence

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John has 30+ years experience working on SI, PI, and EMC challenges at the chip, board, and system level in applications including high-end computing and mil-aero. He holds an MSc. from Bolton University, UK. His current interests are SI/PI co-simulation and modelling for high-speed interfaces.

Shirin Farrahi

Signal and Power Integrity Engineer, Marvell

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Shirin is a Signal and Power Integrity Engineer for Advanced Packaging at Marvell. She previously held roles as a Senior Principal Software Engineer at Cadence working on SI and PI tools for automated PCB design and as a Hardware Engineer in the SPARC Microelectronics group at Oracle. She received her Ph.D. in Electrical Engineering from the Massachusetts Institute of Technology.

Abe Hartman

Senior Principal Hardware Engineer, Oracle

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Abe works on system SI/PI at Oracle and has worked at Amphenol TCS, Juniper Networks, Enterasys, and GM. Abe holds a MS in EE from UMass-Lowell, a MS in Engineering Science from Rensselaer Polytechnic Institute, and a BS in both ME and EE from Kettering University in Flint, MI.

SPEAKERS

Mario Rotigni

Retired

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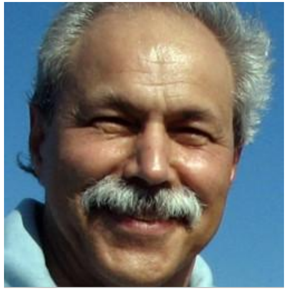
Mario retried after a 45-year career in R&D working on micro-controllers and EMC for automotive applications. He has co-authored 22 papers about EMC of Integrated Circuits and is a member of the IEEE & IEEE EMC Society.



Istvan Novak

Principal SI/PI Engineer, Samtec

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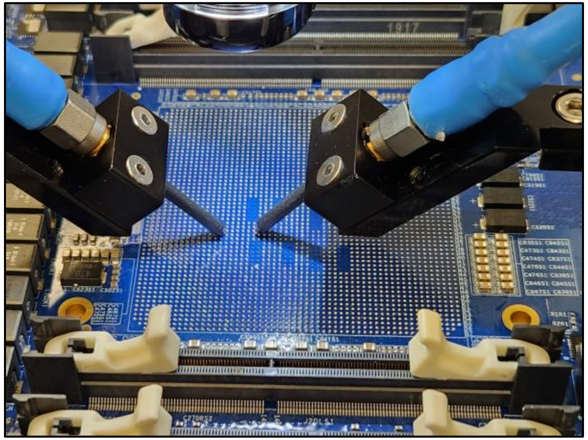
Istvan works on advanced SI/PI designs at Samtec and was previously a Distinguished Engineer at SUN later Oracle. He introduced the first 25µm power-ground laminates for large rigid PCBs and worked to create a series of low inductance, controlled-ESR capacitors. He is a Life Fellow of the IEEE with 25 patents, author of two books on PI, teaches SI/PI courses, and maintains a popular SI/PI website. He was named Engineer of the Year at DesignCon 2020.

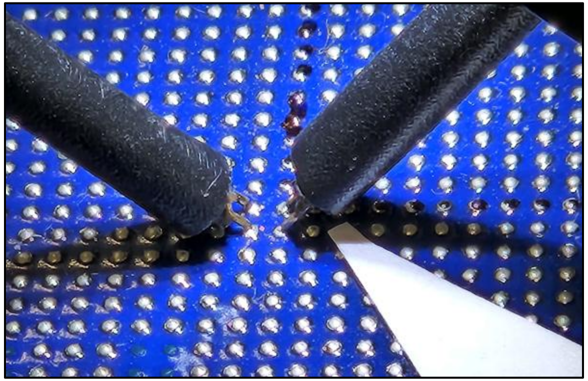
Outline

- Introduction
- Reverse Pulse Technique (RPT)
- Simulation Setups
- RPT Noise Spatial Variation Over Simple PDNs
- Cumulative Power Noise (CPN)
- CPN Analysis of “Real World” DUT
- Conclusion

Introduction

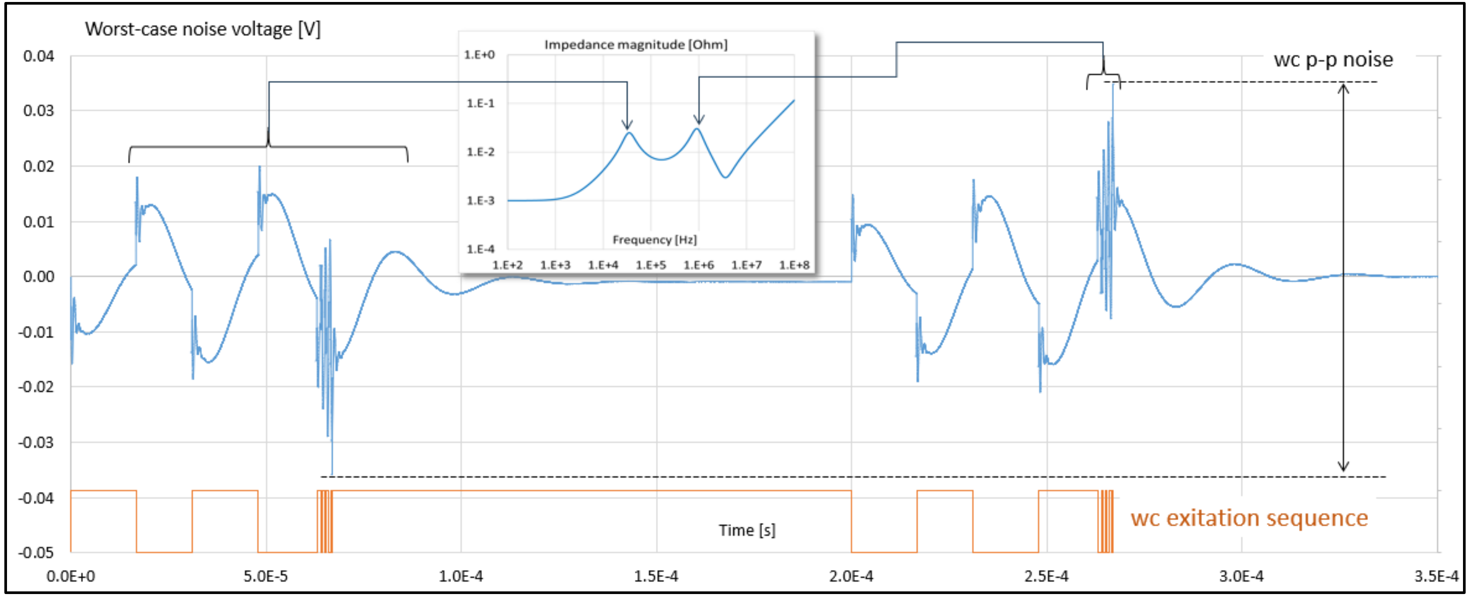
- **Target impedance-based** approach for PDN design **focuses on LTI systems**
- PCB-level PDN designed to handle **low frequency bypassing**
- PDNs supporting high power transients are becoming susceptible to **spatial variation effects**
  - DC Resistance
  - Frequency dependent series plane impedance
  - Parallel PDN impedance
- PDN quantities will vary over even a **BGA**. Measurement/Validation **much more challenging to capture** this
  - Ton of frequency domain impedance measurements
  - Full BGA time domain testers do not currently have necessary granularity
- Aim to **build intuition for spatial variation** and explore this on a real world DUT





Reverse Pulse Technique (RPT)

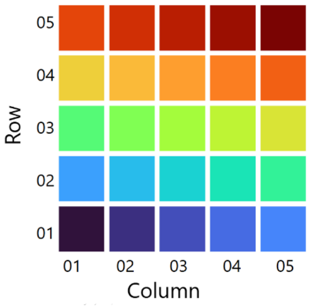
- Frequency domain perspective:
  - Energize resonances such that their corresponding ripples crest simultaneously
- Time domain perspective:
  - Build transient step responses to as to align and superimpose all the peaks and valleys

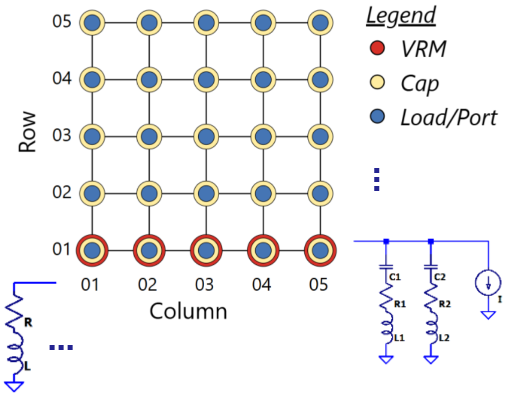


[1] V. Drabkin, C. Houghton, I. Kantorovich and M. Tsuk, "Aperiodic Resonant Excitation of Microprocessor Power Distribution Systems and the Reverse Pulse Technique," *IEEE 11th Topical Meeting on Electrical Performance of Electronic Packaging*, 2002.

Simple Grid PDN

- Experiment on 5x5 grid of nodes:
  - Each node has:
    - Load (1A total grid, 0° skew, 10MHz bandwidth)
    - Parallel capacitors
  - Each 01 row node has connected VRM model
- 6x versions of grid having different node connectivity types explored:
  - Lumped PDN: Direct (shorted) connectivity
  - Ideal PDN: Low Resistance + Low Inductance
  - Resistive PDN: High Resistance + Low Inductance
  - Resistive-Inductive (RL) PDN: High Resistance + High Inductance
  - Inductive PDN: Low Resistance + High Inductance
  - Typical PDN: Moderate Resistance + Moderate Inductance

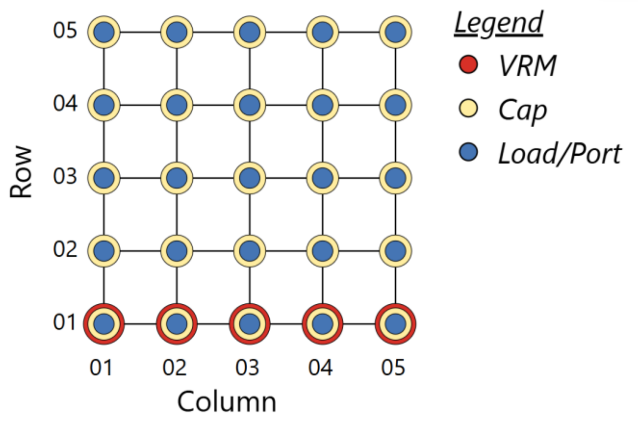


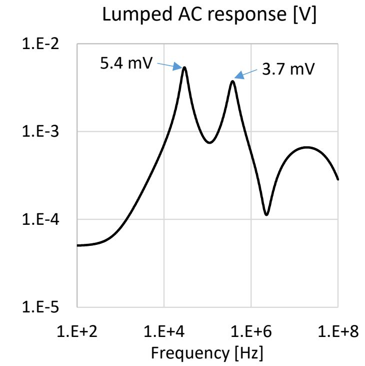


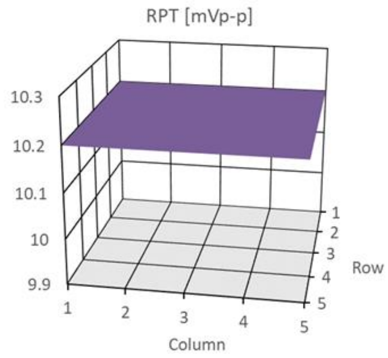
PDN Components	R	L	C
VRM	0.25 mΩ	50 nH	-
Capacitor 1	18.7 mΩ	20 nH	100 µF
Capacitor 2	3 mΩ	0.5 nH	10 µF

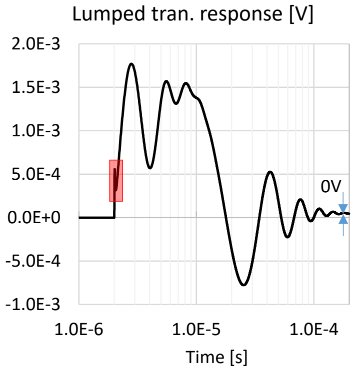
Simple Grid PDN: Lumped PDN

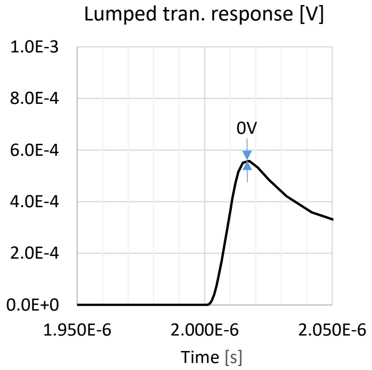
- All nodes directly attached (shorted) to one another
  - No plane structure included
- RPT noise: 10.2mVpp









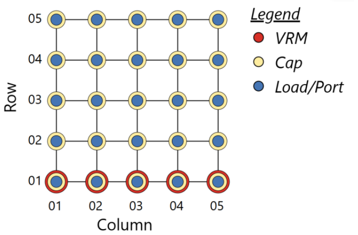


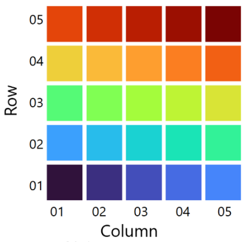
Simple Grid PDN: Ideal Plane

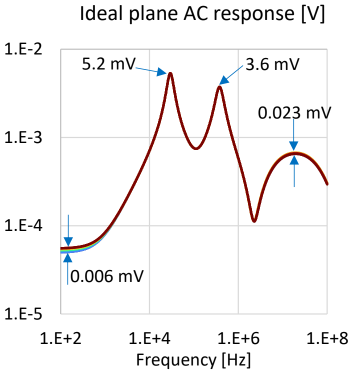
- Connectivity between nodes:

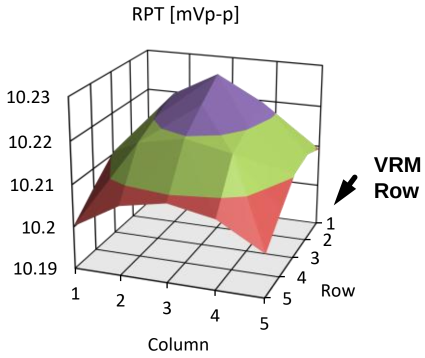
Plane Parameters	R	L	C
Ideal Plane	0.01 mΩ	0.02 nH	0.184nF

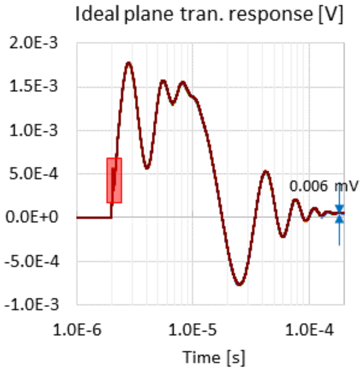
- Results very similar to “Lumped PDN” case
- See small deviation between node voltages:
  - Initial inductive spike peak value
  - DC offset due to load current
- RPT noise: 10.23mVpp

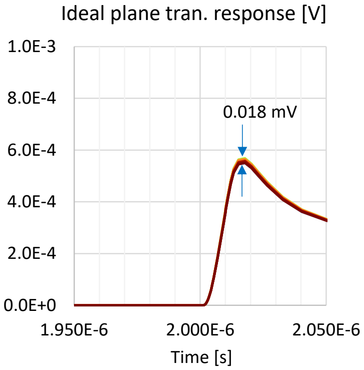










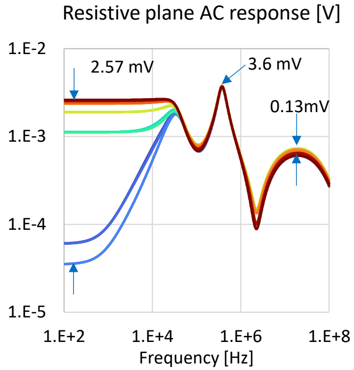


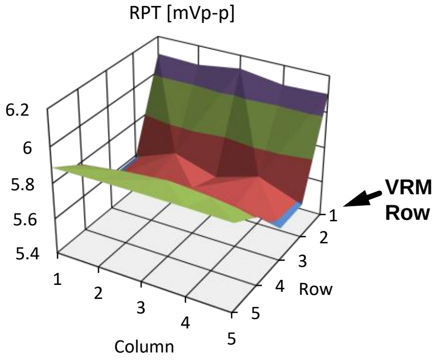
Simple Grid PDN: Resistive Plane

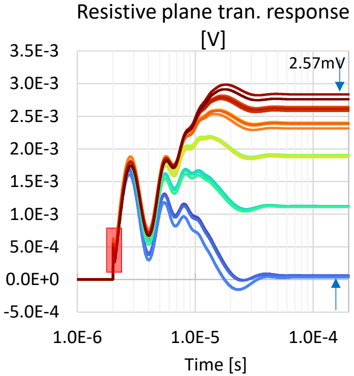
- Connectivity between nodes:

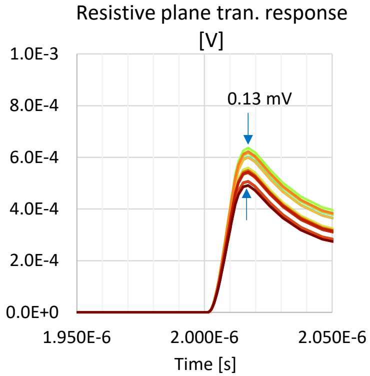
Plane Parameters	R	L	C
Resistive Plane	5 mΩ	0.142 nH	0.184nF

- Noticeable deviation between node voltages:
  - Large spread at low frequencies (DC offsets)
  - Small spread at high frequencies (small inductance)
  - Peak RPT noise decreased by ~2x due to added loss lowering the first impedance peak (5.2mΩ→2.57mΩ)
- Max RPT noise: ~6.1mVpp







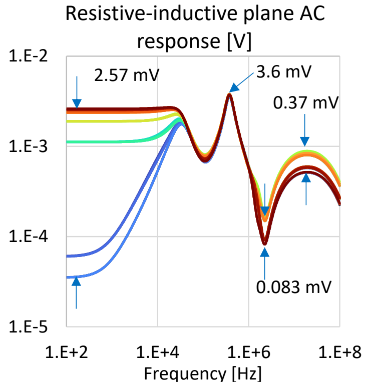


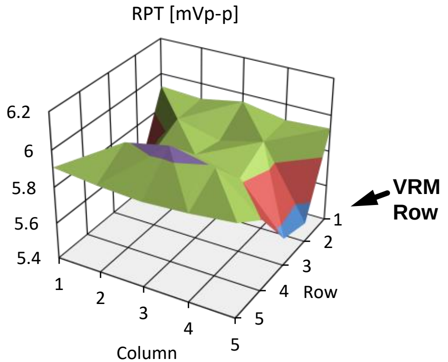
Simple Grid PDN: Resistive-Inductive Plane

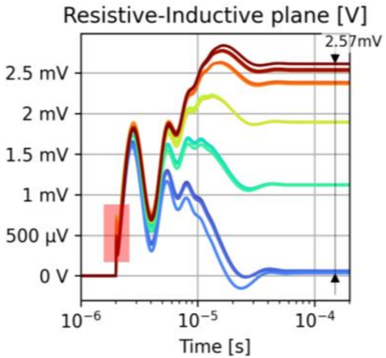
- Connectivity between nodes:

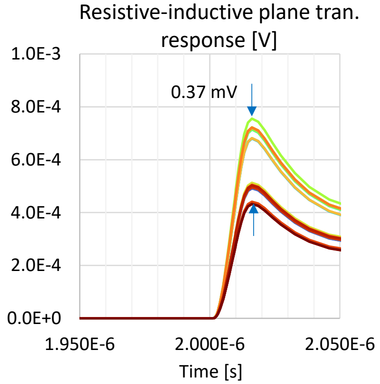
Plane Parameters	R	L	C
RL Plane	5 mΩ	1 nH	0.184nF

- Noticeable deviation between node voltages:
  - Large spread at low frequencies (DC offsets)
  - Large spread at high frequencies (inductive isolation)
  - Large spread at SRF of higher-frequency capacitor
  - Model filtering limits impact of larger inductance, “large resistance” behavior dominates RPT profile
- Peak RPT noise: ~5.9mVpp







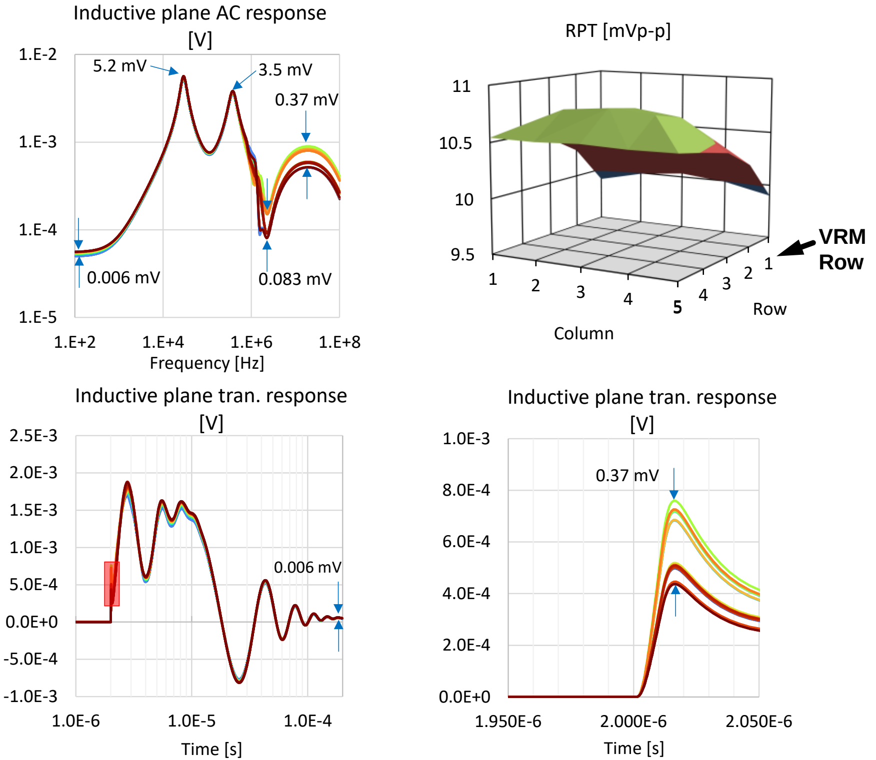


Simple Grid PDN: Inductive Plane

- Connectivity between nodes:

Plane Parameters	R	L	C
Inductive Plane	0.01 mΩ	1 nH	0.184nF

- Noticeable deviation between node voltages:
  - Large spread at high frequencies (Inductive isolation)
  - Large spread at SRF of higher-frequency capacitor
  - Large RPT spread across edge of plane
  - Small spread at low frequencies
  - Small RPT spread in center of plane
  - Increased first impedance peak (5.2mΩ) and lower loss gives larger max RPT voltage
- Max RPT noise: ~10.8mVpp

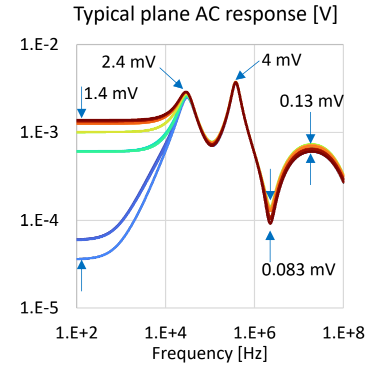


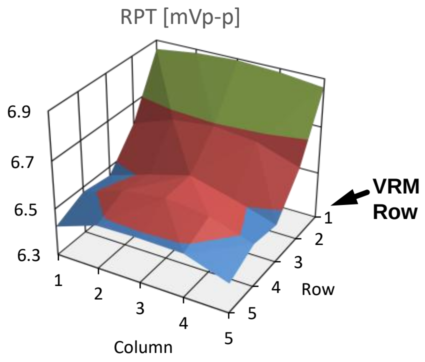
Simple Grid PDN: Typical Plane

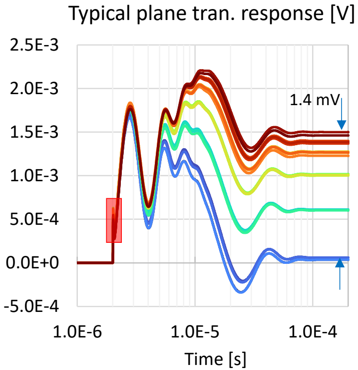
- Connectivity between nodes:

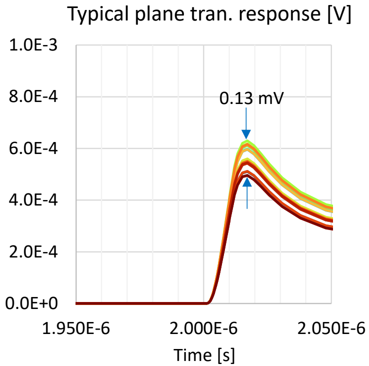
Plane Parameters	R	L	C
Inductive Plane	2.6 mΩ	0.142 nH	0.184nF

- Noticeable deviation between node voltages:
  - Moderate spread at high frequencies (Inductive isolation)
  - Moderate spread at SRF of higher-frequency capacitor
  - Moderate spread at low frequencies
- Max RPT noise: ~6.9mVpp



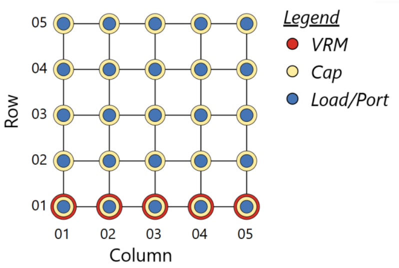




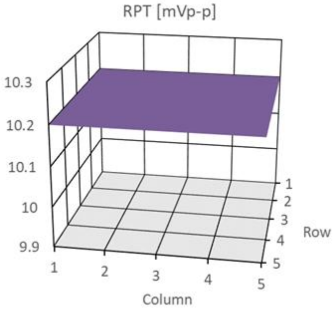


Simple Grid PDN: SUMMARY

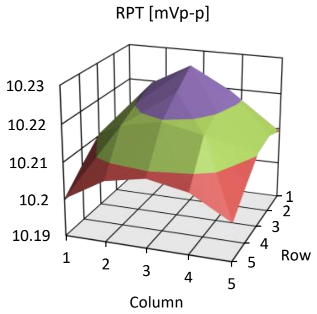
- Impedance variation at low frequencies:
  - ↑ spread of steady-state voltage levels
- Impedance variation at high frequencies:
  - ↑ spread of initial transient
- Larger peaking/Q in impedance profile:
  - ↑ RPT peak-to-peak magnitude
- Spreading out load in any case:
  - ↓ RPT peak-to-peak magnitude



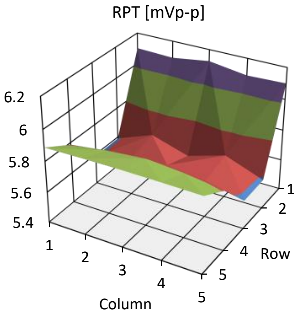
Lumped PDN (10.2mVpp)



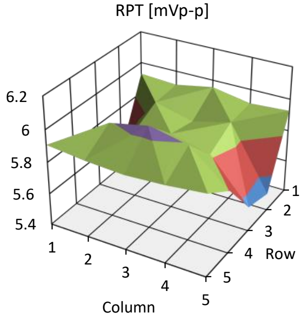
Ideal Plane (10.23mVpp)



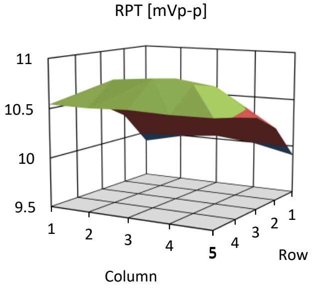
Resistive Plane (6.1mVpp)



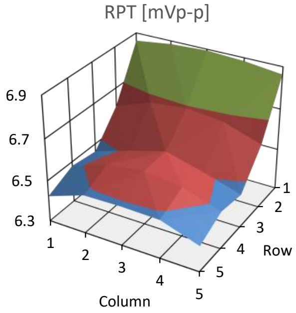
Resistive-Inductive Plane (5.9mVpp)



Inductive Plane (10.8mVpp)



Typical Plane (6.9mVpp)

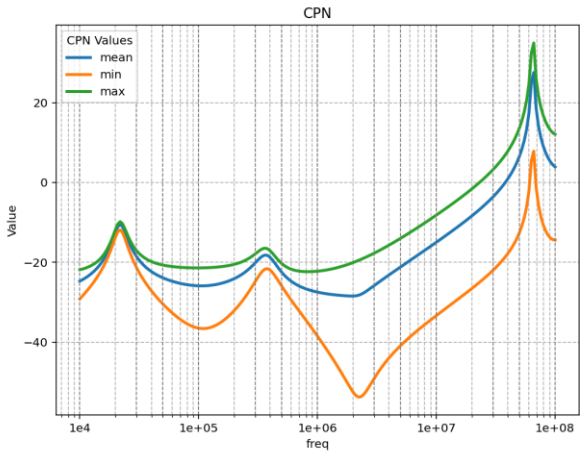


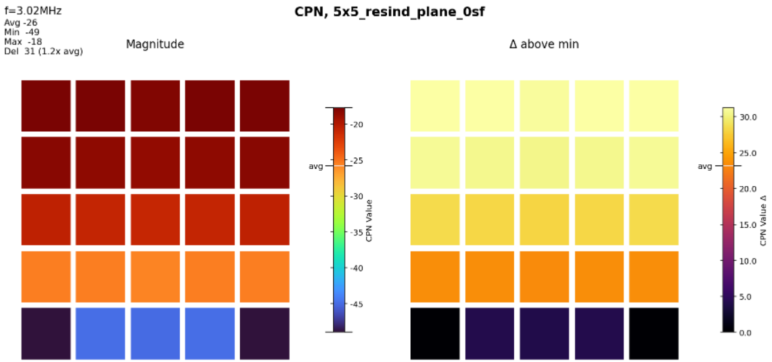
Cumulative Power Noise (CPN)

- Cumulative Power Noise (CPN) considers AC PDN noise:

$$CPN(P_{x_i,y_i}, f) = \sum_{n=1}^{N} |Z_{i,n}(f)|^2$$

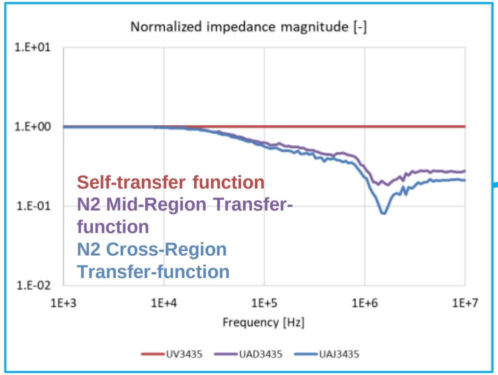
  - Include self-generated noise: examine total noise at victim
  - Exclude self-generated noise: examine susceptibility to aggressors
- Phase relationship of xtalk and skew between nodes ignored
- Examples (right) are for RL 5x5 PDN grid
- 3MHz frequency dominated by inductive component of example PDNs
  - >30dB delta in CPN magnitude across grid
  - Highest noise seen along top row (most isolation from the VRMs)
  - Slight increase in CPN towards center of the rows due to the higher current carrying capabilities

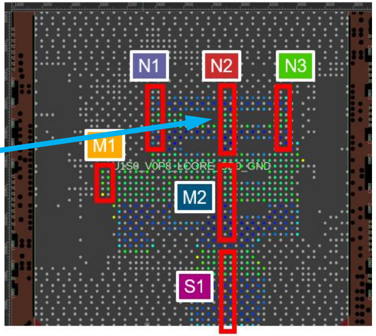


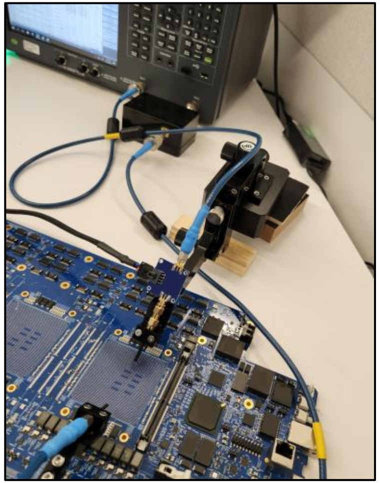


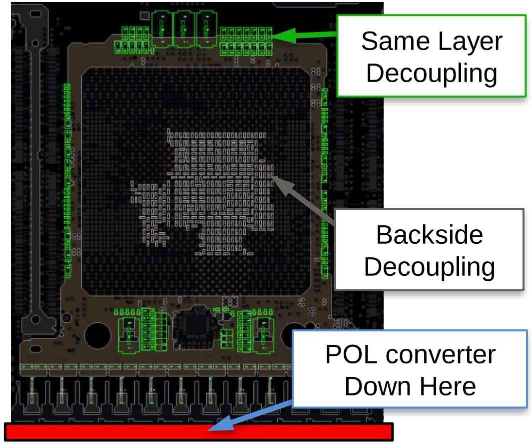
“Real World” DUT PDN

- DUT: POL, 250A AI application (2.5D simulation)
  - 30-layer stackup, 3 power layers, half of layers GND
  - BGA: 432 pwr pins, 1400 GND pins
  - 500 decoupling caps, 5 different values
  - <0.25nH net inductance seen by IC
  - <1mOhm impedance 10kHz - 3MHz (seen looking into pcb BGA)
- Spatial filtering above 30kHz between nearby pins
  → lumped BGA analysis against target impedance will lead to overdesign





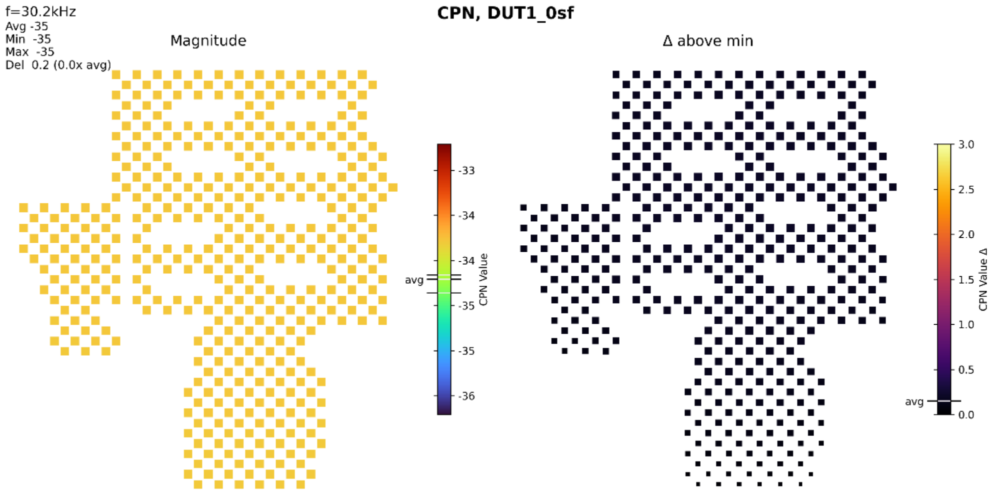




[22] E. Koether, J. Hartman, K. Skytte, S. Farrahi, M. Rotigni and I. J. Phillips, "Determining the Requirements, Die vs. Package vs. Board: Multi-level Power Distribution Network Design," in *Designcon*, 2025.

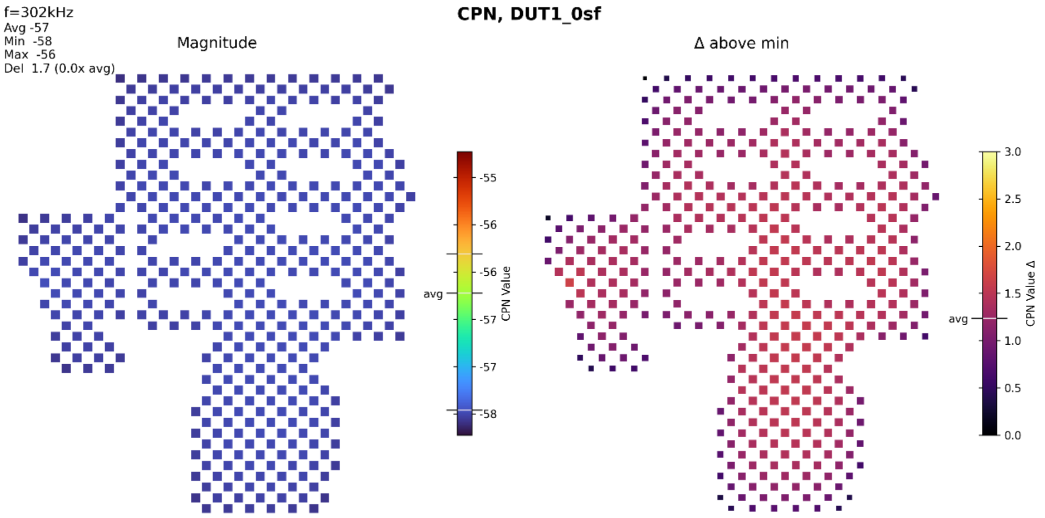
“Real World” DUT PDN: CPN (30kHz)

- CPN spatial distribution at 30kHz (excluding self-terms):
  - 30kHz is corner frequency of spatial filtering profiles
  - Approximately uniform CPN distribution across BGA (less than 0.2dB Δ)
  - Distribution aligns with pure DC behavior



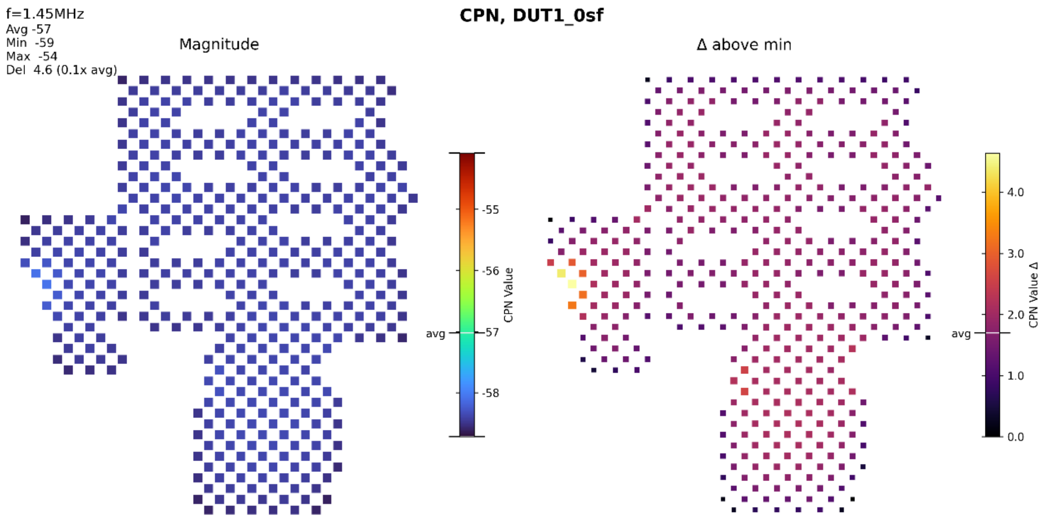
"Real World" DUT PDN: CPN (300kHz)

- CPN spatial distribution at 300kHz (excluding self-terms):
  - Average of 1.2dB Δ deviation in CPN above minimum value (2dB max Δ)
  - Minimum CPN values around perimeter of BGA, both close to VRM and at other end of BGA
    - Close to VRM, less noise is expected due to generally lower impedance magnitude
    - At other end of BGA, less noise due to pins having less shared current path, greater isolation compared to central pins



“Real World” DUT PDN: CPN (1.45MHz)

- CPN spatial distribution at 1.45MHz (excluding self-terms):
  - Average of 1.8dB ∆ deviation in CPN above minimum value (5dB max ∆)
  - Left hand group of outlier pins, believed to have “weak” PDN support at this frequency (i.e. relatively high inductance)



Conclusion

- Low impedance PDNs will see spatial variation in self-impedance and transfer-impedances from neighbors, and so **noise distribution will vary spatially as well**
- **RPT** derived from full BGA (grid) illumination **can be a useful metric** for quantifying the maximum noise seen by the load device
- RPT noise distribution will **depend on the nature of the PDN**
    - **[Resistive Behaving]** Impedance variation at low frequencies: ↑ spread of steady-state voltage levels
    - **[Inductive Behaving]** Impedance variation at high frequencies: ↑ spread of initial transient
    - **[PDN with Resonances]** Larger peaking/Q in impedance profile: ↑ RPT peak-to-peak magnitude
    - **[PDN with Distributed Load]** Spreading out load compared to “point” load: ↓ RPT peak-to-peak magnitude
- **CPN metric can also be useful** for understanding “uniformity” of PDN support for BGA and identifying pins having “weak” support
- RPT and CPN **analysis reduced risk for overdesign** compared to the target impedance methodology
- RPT and CPN are generic, accessible, and informative tools for analyzing PDN performance while being vendor IP-agnostic. They are therefore **a step in the direction of industry aligned PI compatibility analysis** that both protects vendor IP and reduces risk of overdesign.

Thank you!

QUESTIONS?

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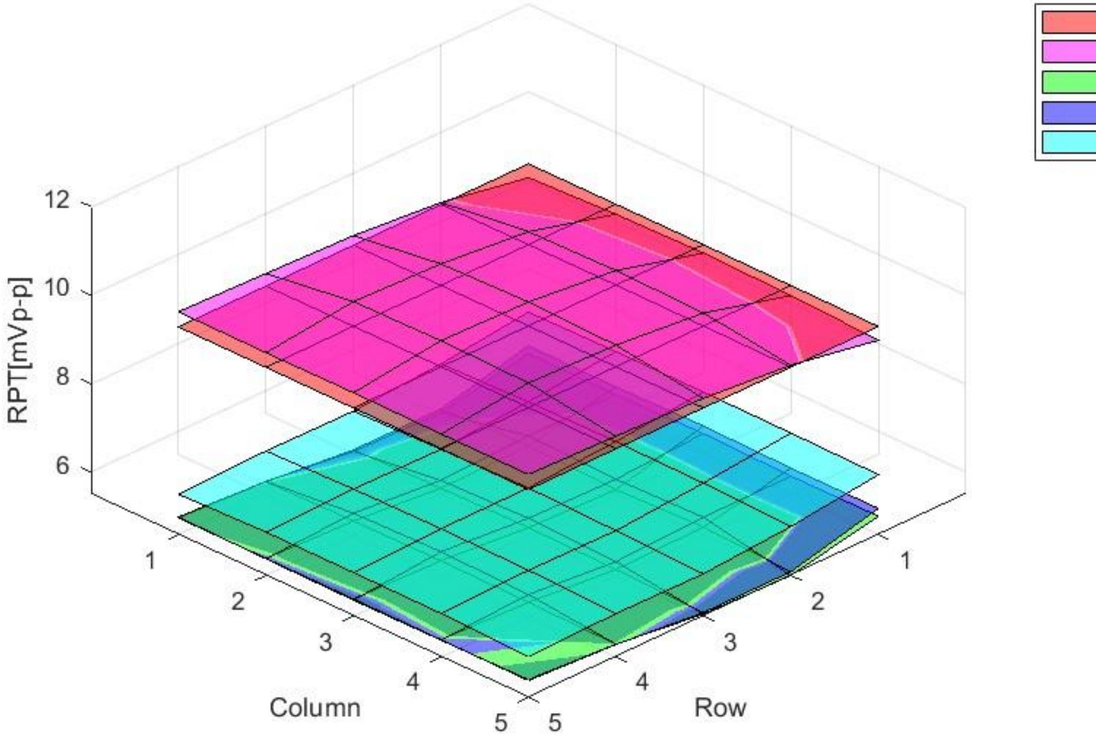
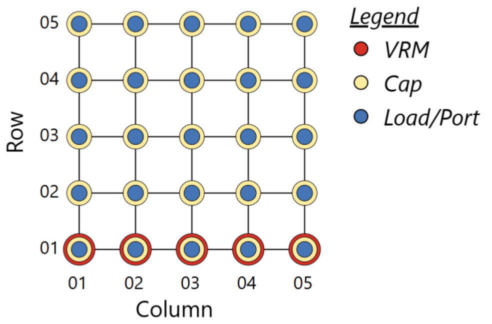
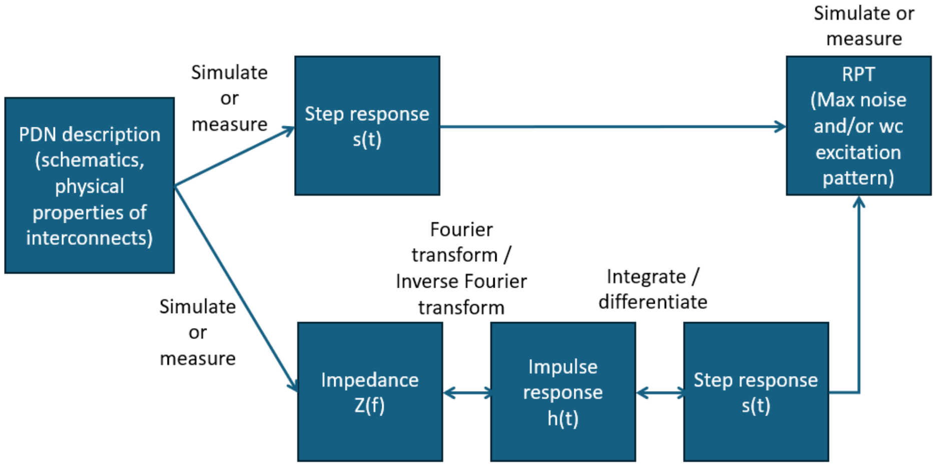
Simple Grid PDN: Overlay of RPT Surfaces

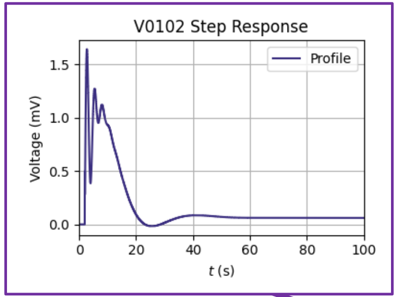




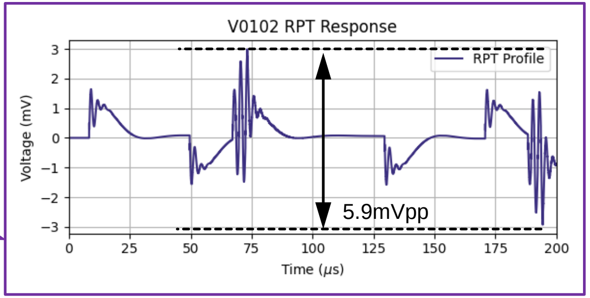
Simulation Setup

- Simple grid PDNs had step responses solved in SPICE
  - Default calculation/convergence settings
  - 5 pole 10MHz Butterworth filter used to bandwidth limit simulation
  - RPT generated in Python using SPICE results
- Generation of RPT voltage response can take either of two tracks
  - PDN model SPICE → simulated step response → Python calculated RPT



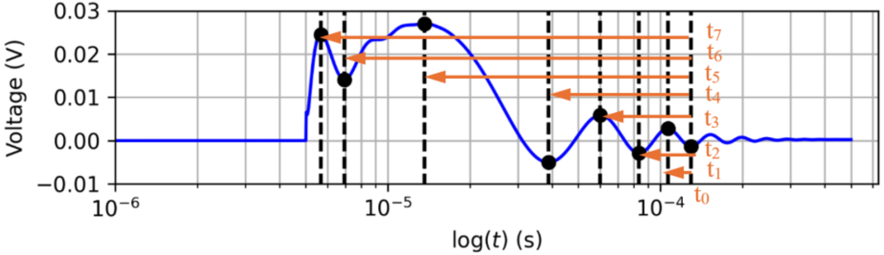


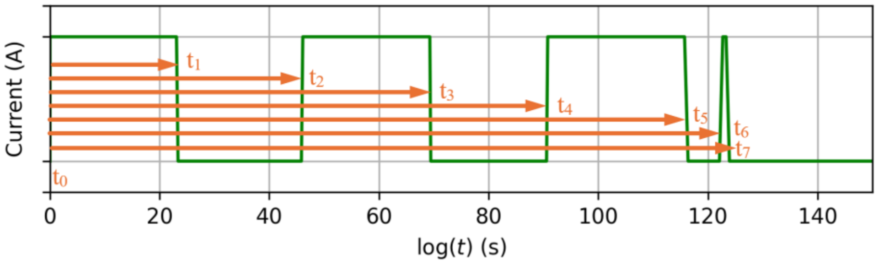
Python Script



Reverse Pulse Technique (RPT)

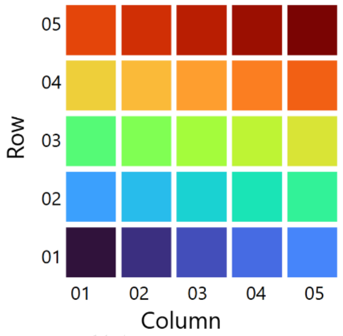
- RPT algorithm generates worst case current profile for a given PDN:
  1. Identify local maxima and minima of step response and their corresponding time stamps
  2. Identify time stamp of final extremum, t_m
  3. Find the difference in time between the final extremum time stamp, t_m, and each of the previous extremum time stamps, $t_1, t_2, \dots, t_N$
  4. Reverse sequence of time deltas found in step 3 to order from smallest to largest. The reversed sequence corresponds to the RPT current profile edges (transition times) from "low" → "high" and "high" → "low", alternating.

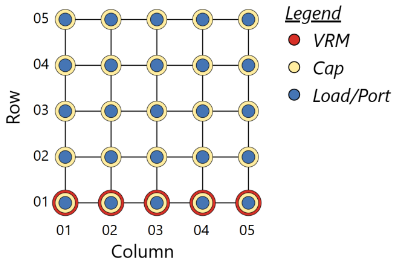


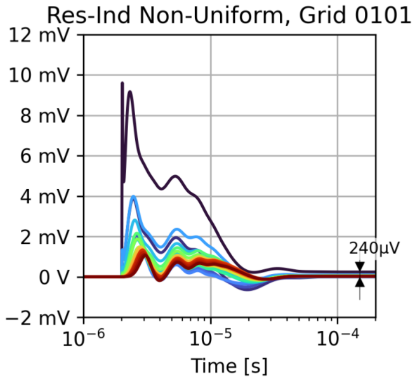


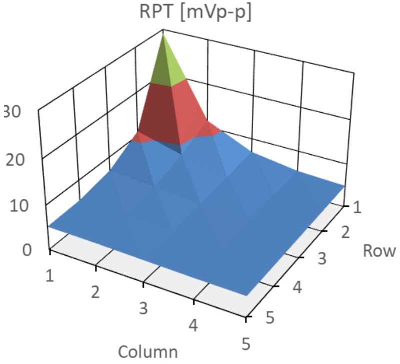
Simple Grid PDN: Single Pin Excitation of RL Grid (1)

- RPT defined and valid for single point excitation
  - Loading a over a region having spatial variation deviates from this definition
- Experiment loading single pin (1) at edge of grid on VRM row [0101] and (2) at pin furthest away from this [0505]
  - Initial peak transient the same in both cases, ~10mV
  - Steady state voltages different due to discrepancy in DC impedances between rows
  - Peak noise amplitude at aggressor
  - Peak RPT voltage ~30mV
  - Trend in step responses over spatial distribution align with trend in RPT surface plot



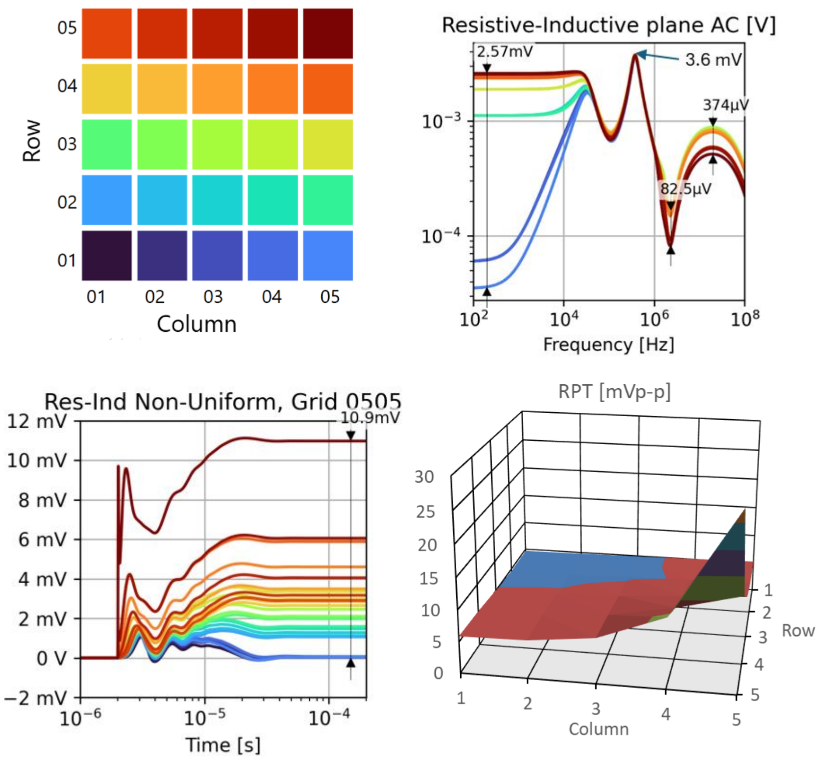






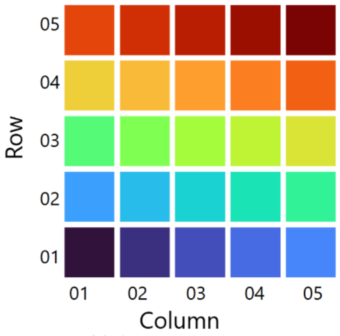
Simple Grid PDN: Single Pin Excitation of RL Grid (2)

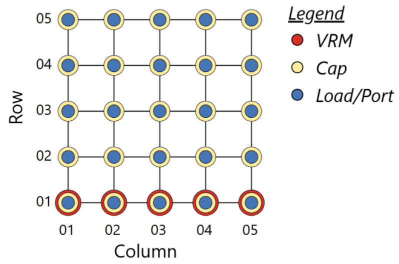
- RPT defined and valid for single point excitation
  - Loading a over a region having spatial variation deviates from this definition
- Experiment loading single pin (1) at edge of grid on VRM row [0101] and (2) at pin furthest away from this [0505]
  - Initial peak transient the same in both cases, ~10mV
  - Steady state voltages different due to discrepancy in DC impedances between rows
  - Peak noise amplitude at aggressor
  - Peak RPT voltage ~30mV
  - Trend in step responses over spatial distribution align with trend in RPT surface plot

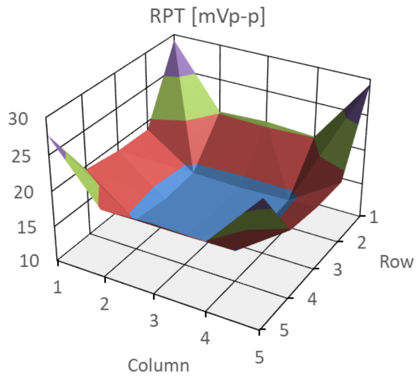


Simple Grid PDN: Single Pin Excitation of RL Grid (3)

- RPT defined and valid for single point excitation
  - Loading a over a region having spatial variation deviates from this definition
- Experiment loading single pin (1) at edge of grid on VRM row [0101] and (2) at pin furthest away from this [0505]
  - Initial peak transient the same in both cases, ~10mV
  - Steady state voltages different due to discrepancy in DC impedances between rows
  - Peak noise amplitude at aggressor
  - Peak RPT voltage ~30mV
  - Trend in step responses over spatial distribution align with trend in RPT surface plot

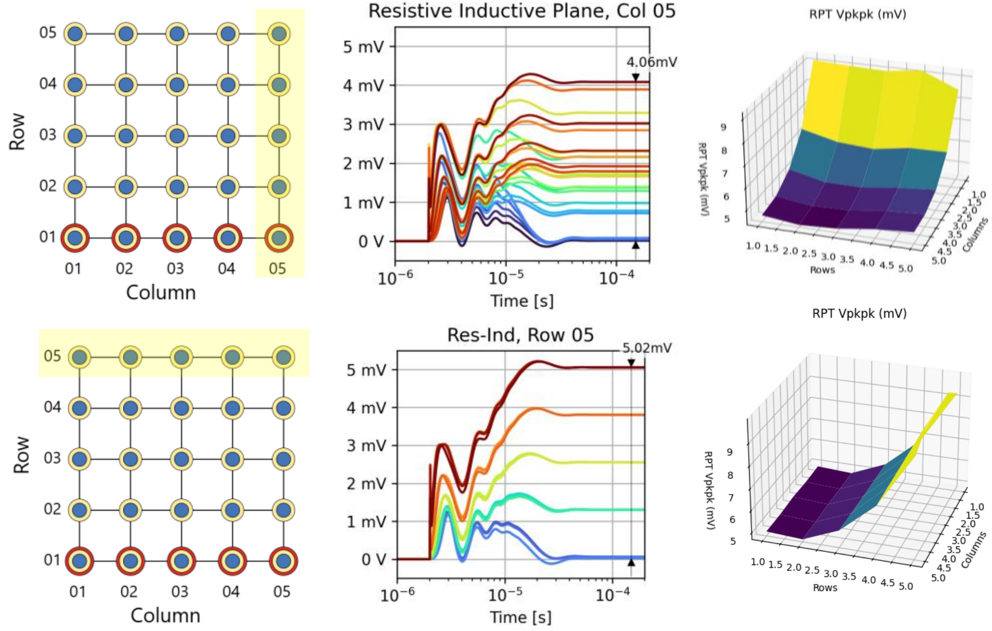






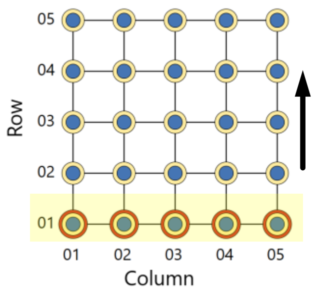
Simple Grid PDN: Non-Uniform Excitation of RL Grid

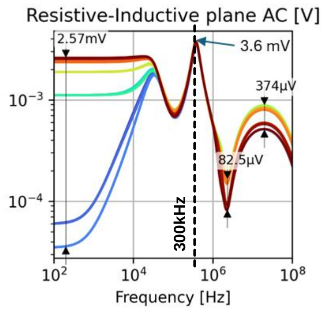
- Column-wise excitation (only) of RL PDN grid
  - Noise non-uniformly increases
- Row-wise excitation (only) of RL PDN grid
  - Noise lower than seen with column-wise excitation when excited row closer to VRM row (01-03)
  - Noise larger than seen with column-wise excitation when excited row far from VRM (04-05)

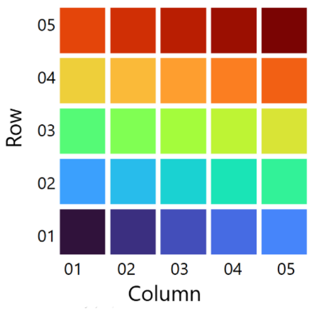


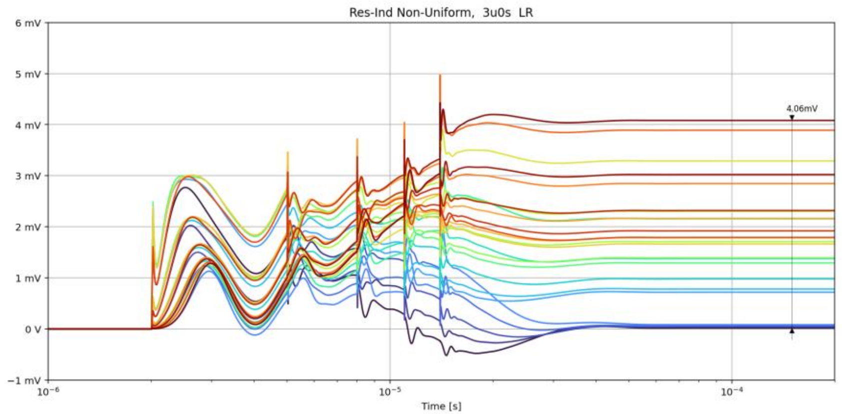
Simple Grid PDN: Non-Uniform Excitation of RL Grid

- Row-wise rolling excitation of RL PDN grid
  - Turn on/off one row at a time from 01 → 05
  - 3us period to aggravate 300kHz resonance
  - Noise builds up in excitation profile
  - Transient ripples peak-to-peak magnitude decrease as excitations move towards row 05
  - DC deviation grows as move towards row 05



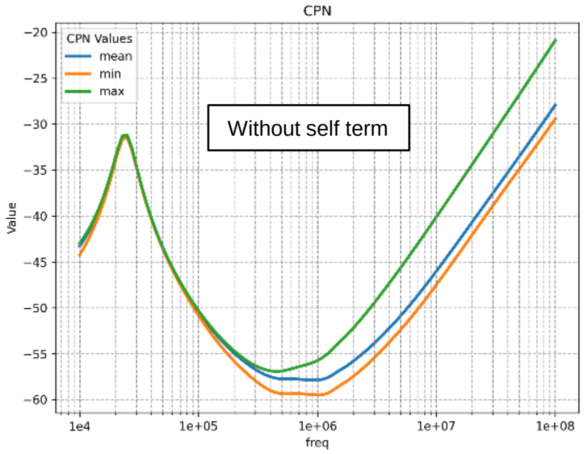


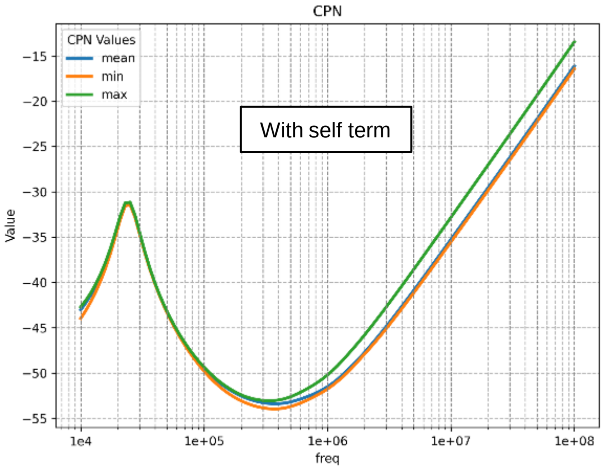




“Real World” DUT PDN: CPN

- CPN curves:
  - Virtually no variation below 100kHz
  - Above 100kHz see larger spread (>5dB) in CPN excluding self terms
  - Less pronounced deviation between CPN values across BGA when including self terms





SPICE – PDN Simulation Deck (Main)

- Main Netlist – parameters, sub-circuits and simulation options

```
* Plane-grid-TRAN analysis for PSPICE
*
* Double Z peak PDN from Istvan
* TRAN simulation using KS Filter 5 poles

*filter related parameters
.param fMHz=100
.param fc = {fMHz * 1e6}

*Plane parameters
.param Rp 5m
.param Lp 1n
.param Cp 0.184n

*Component parameters
.param Vrm_r=0.25m
.param Vrm_l=50n
.param Cap1=100u Cap2=10uF
.param ESR1 18.7m ESR2=3m
.param ESL1 20n ESL2=0.5n

* ****Source settings
* Time
.param tdshift=0.1u tdini=10n tdead=0 tON={tdshift-tdead}
* Current amplitudes periphery and core
.param Iperi={1/8} Imid={1/4}
```

```

* Include subckt models and configure grid
.inc 'network.spi'
.inc 'source_spec.sp'

.TRAN 0 0.2m 0 10n
.OPTIONS RELTOL = 0.001
.OPTIONS NUMDGT = 6

.print tran V(0501) V(0502) V(0503) V(0504) V(0505)
.print tran V(0401) V(0402) V(0403) V(0404) V(0405)
.print tran V(0301) V(0302) V(0303) V(0304) V(0305)
.print tran V(0201) V(0202) V(0203) V(0204) V(0205)
.print tran V(0101) V(0102) V(0103) V(0104) V(0105)

.end
```

SPICE – PDN Simulation Deck (subckt)

- Circuit models of capacitors, VRMs, plane and current filter (network.spi)

```
.subckt BUTTER5 in out ref PARAMS: fMHz=10
    .param wc = {2 * 3.14159 * fMHz * 1e6}

    * Normalized Butterworth prototype values (g-values)
    * g1 = 0.618, g2 = 1.618, g3 = 2.0, g4 = 1.618, g5 = 0.618

    * Stage 1
    .param R1 = {1 / wc * 0.618}
    .param C1 = {1}
    R1 in n1 {R1}
    C1 n1 ref {C1}

    * Stage 2
    .param R2 = {1 / wc * 1.618}
    .param C2 = {1}
    R2 n1 n2 {R2}
    C2 n2 ref {C2}

    * Stage 3
    .param R3 = {1 / wc * 2.0}
    .param C3 = {1}
    R3 n2 n3 {R3}
    C3 n3 ref {C3}

    * Stage 4
    .param R4 = {1 / wc * 1.618}
    .param C4 = {1}
    R4 n3 n4 {R4}
    C4 n4 ref {C4}

    * Stage 5
    .param R5 = {1 / wc * 0.618}
    .param C5 = {1}
    R5 n4 out {R5}
    C5 out ref {C5}
.ends BUTTER5

.subckt src_filter out ref PARAMS: I0=0 IMAX=1 trf=10e-9 td=0 tpulsew=1 tperiod=1
    Vin 100 ref PULSE ( {I0} {IMAX} {2e-6+td} {trf} {trf} {tpulsew} {tperiod})
    * Instantiate filters
    XACTIVE 100 101 ref BUTTER5 PARAMS: fMHz={fMHz}
    Rdmu  101  ref  1E6
    G ref out 101 ref 1
.ends
```

```
.SUBCKT Planecell Left Right Ret PARAMS: Rp={Rp} Lp={Lp} Cp={Cp}
R1 Left dummy {Rp}
L1 dummy Right {Lp}
C1 Right Ret {Cp}
.ENDS Planecell

.SUBCKT Planeedgecell Left Right Ret PARAMS: Rp={Rp} Lp={Lp} Cp={Cp}
R1 Left dummy {2*Rp}
L1 dummy Right {2*Lp}
C1 Right Ret {Cp/2}
.ENDS Planeedgecell

.SUBCKT VRM Vrm_p Vrm_m PARAMS: Vrm_r={Vrm_r} Vrm_l={Vrm_l}
R1 Vrm_m dummy3 {Vrm_r}
L1 dummy3 Vrm_p {Vrm_l}
.ENDS VRM


.SUBCKT Mycapacitor Cap_p Cap_m PARAMS: Cap1={Cap1} ESR1={ESR1} ESL1={ESL1} Cap2={Cap2} ESR2={ESR2} ESL2={ESL2}
C1 Cap_p dummy1 {Cap1}
R1 dummy1 dummy2 {ESR1}
L1 dummy2 Cap_m {ESL1}
C2 Cap_p dummy3 {Cap2}
R2 dummy3 dummy4 {ESR2}
L2 dummy4 Cap_m {ESL2}
.ENDS Mycapacitor
```

SPICE – PDN Simulation Deck (Grid)

- Component placements and grid model (network.spi)

```
* Bottom horizontal plane cells
Xph11 0101 0102 0 Planeedgecell
Xph12 0102 0103 0 Planeedgecell
Xph13 0103 0104 0 Planeedgecell
Xph14 0104 0105 0 Planeedgecell
*
* Inside horizontal plane cells
Xph21 0201 0202 0 Planecell
Xph22 0202 0203 0 Planecell
Xph23 0203 0204 0 Planecell
Xph24 0204 0205 0 Planecell
Xph31 0301 0302 0 Planecell
Xph32 0302 0303 0 Planecell
Xph33 0303 0304 0 Planecell
Xph34 0304 0305 0 Planecell
Xph41 0401 0402 0 Planecell
Xph42 0402 0403 0 Planecell
Xph43 0403 0404 0 Planecell
Xph44 0404 0405 0 Planecell
*
* Top horizontal plane cell
Xph51 0501 0502 0 Planeedgecell
Xph52 0502 0503 0 Planeedgecell
Xph53 0503 0504 0 Planeedgecell
Xph54 0504 0505 0 Planeedgecell

* Left vertical plane cells
Xpv11 0101 0201 0 Planeedgecell
Xpv21 0201 0301 0 Planeedgecell
Xpv31 0301 0401 0 Planeedgecell
Xpv41 0401 0501 0 Planeedgecell
*
```

```
* Inside vertical plane cells
Xpv12 0102 0202 0 Planecell
Xpv22 0202 0302 0 Planecell
Xpv32 0302 0402 0 Planecell
Xpv42 0402 0502 0 Planecell
Xpv13 0103 0203 0 Planecell
Xpv23 0203 0303 0 Planecell
Xpv33 0303 0403 0 Planecell
Xpv43 0403 0503 0 Planecell
Xpv14 0104 0204 0 Planecell
Xpv24 0204 0304 0 Planecell
Xpv34 0304 0404 0 Planecell
Xpv44 0404 0504 0 Planecell
*
* Right vertical plane cells
Xpv15 0105 0205 0 Planeedgecell
Xpv25 0205 0305 0 Planeedgecell
Xpv35 0305 0405 0 Planeedgecell
Xpv45 0405 0505 0 Planeedgecell
```

```
*Capacitor grid
Xc11 0101 0  Mycapacitor
Xc12 0102 0  Mycapacitor
Xc13 0103 0  Mycapacitor
Xc14 0104 0  Mycapacitor
Xc15 0105 0  Mycapacitor
Xc21 0201 0  Mycapacitor
Xc22 0202 0  Mycapacitor
Xc23 0203 0  Mycapacitor
Xc24 0204 0  Mycapacitor
Xc25 0205 0  Mycapacitor
Xc31 0301 0  Mycapacitor
Xc32 0302 0  Mycapacitor
Xc33 0303 0  Mycapacitor
Xc34 0304 0  Mycapacitor
Xc35 0305 0  Mycapacitor
Xc41 0401 0  Mycapacitor
Xc42 0402 0  Mycapacitor
Xc43 0403 0  Mycapacitor
Xc44 0404 0  Mycapacitor
Xc45 0405 0  Mycapacitor
Xc51 0501 0  Mycapacitor
Xc52 0502 0  Mycapacitor
Xc53 0503 0  Mycapacitor
Xc54 0504 0  Mycapacitor
Xc55 0505 0  Mycapacitor

*VRM subcircuits
Xv1 0101 0 Vrm
Xv2 0102 0 Vrm
Xv3 0103 0 Vrm
Xv4 0104 0 Vrm
Xv5 0105 0 Vrm
```

SPICE – PDN Simulation Deck (Source)

- Source and amplitude configuration (sample for left to right rolling excitation; source_spec.sp)

```
*LR source specification, last switch stays high

* Source array specification
*Time delay
.param td51={0*tdshift+tdini} td52={1*tdshift+tdini+tdead} td53={2*tdshift+tdini+2*tdead} td54={3*tdshift+tdini+3*tdead} td55={4*tdshift+tdini+4*tdead}
.param td41={0*tdshift+tdini} td42={1*tdshift+tdini+tdead} td43={2*tdshift+tdini+2*tdead} td44={3*tdshift+tdini+3*tdead} td45={4*tdshift+tdini+4*tdead}
.param td31={0*tdshift+tdini} td32={1*tdshift+tdini+tdead} td33={2*tdshift+tdini+2*tdead} td34={3*tdshift+tdini+3*tdead} td35={4*tdshift+tdini+4*tdead}
.param td21={0*tdshift+tdini} td22={1*tdshift+tdini+tdead} td23={2*tdshift+tdini+2*tdead} td24={3*tdshift+tdini+3*tdead} td25={4*tdshift+tdini+4*tdead}
.param td11={0*tdshift+tdini} td12={1*tdshift+tdini+tdead} td13={2*tdshift+tdini+2*tdead} td14={3*tdshift+tdini+3*tdead} td15={4*tdshift+tdini+4*tdead}


*Amplitude - uniform distribution
.param sa51={Iperi} sa52={Iperi} sa53={Iperi} sa54={Iperi} sa55={Iperi}
.param sa41={Imid}  sa42={Imid}  sa43={Imid}  sa44={Imid}  sa45={Imid}
.param sa31={Imid}  sa32={Imid}  sa33={Imid}  sa34={Imid}  sa35={Imid}
.param sa21={Imid}  sa22={Imid}  sa23={Imid}  sa24={Imid}  sa25={Imid}
.param sa11={Iperi} sa12={Iperi} sa13={Iperi} sa14={Iperi} sa15={Iperi}


*Sources
x0101 0101 0 src_filter PARAMS: td={td11} IMAX={sa11} tpulsew={tON}
x0102 0102 0 src_filter PARAMS: td={td12} IMAX={sa12} tpulsew={tON}
x0103 0103 0 src_filter PARAMS: td={td13} IMAX={sa13} tpulsew={tON}
x0104 0104 0 src_filter PARAMS: td={td14} IMAX={sa14} tpulsew={tON}
x0105 0105 0 src_filter PARAMS: td={td15} IMAX={sa15} tpulsew=10

x0201 0201 0 src_filter PARAMS: td={td21} IMAX={sa21} tpulsew={tON}
x0202 0202 0 src_filter PARAMS: td={td22} IMAX={sa22} tpulsew={tON}
x0203 0203 0 src_filter PARAMS: td={td23} IMAX={sa23} tpulsew={tON}
x0204 0204 0 src_filter PARAMS: td={td24} IMAX={sa24} tpulsew={tON}
x0205 0205 0 src_filter PARAMS: td={td25} IMAX={sa25} tpulsew=10

x0301 0301 0 src_filter PARAMS: td={td31} IMAX={sa31} tpulsew={tON}
x0302 0302 0 src_filter PARAMS: td={td32} IMAX={sa32} tpulsew={tON}
x0303 0303 0 src_filter PARAMS: td={td33} IMAX={sa33} tpulsew={tON}
x0304 0304 0 src_filter PARAMS: td={td34} IMAX={sa34} tpulsew={tON}
x0305 0305 0 src_filter PARAMS: td={td35} IMAX={sa35} tpulsew=10

x0401 0401 0 src_filter PARAMS: td={td41} IMAX={sa41} tpulsew={tON}
x0402 0402 0 src_filter PARAMS: td={td42} IMAX={sa42} tpulsew={tON}
x0403 0403 0 src_filter PARAMS: td={td43} IMAX={sa43} tpulsew={tON}
x0404 0404 0 src_filter PARAMS: td={td44} IMAX={sa44} tpulsew={tON}
x0405 0405 0 src_filter PARAMS: td={td45} IMAX={sa45} tpulsew=10

x0501 0501 0 src_filter PARAMS: td={td51} IMAX={sa51} tpulsew={tON}
x0502 0502 0 src_filter PARAMS: td={td52} IMAX={sa52} tpulsew={tON}
x0503 0503 0 src_filter PARAMS: td={td53} IMAX={sa53} tpulsew={tON}
x0504 0504 0 src_filter PARAMS: td={td54} IMAX={sa54} tpulsew={tON}
x0505 0505 0 src_filter PARAMS: td={td55} IMAX={sa55} tpulsew=10
```