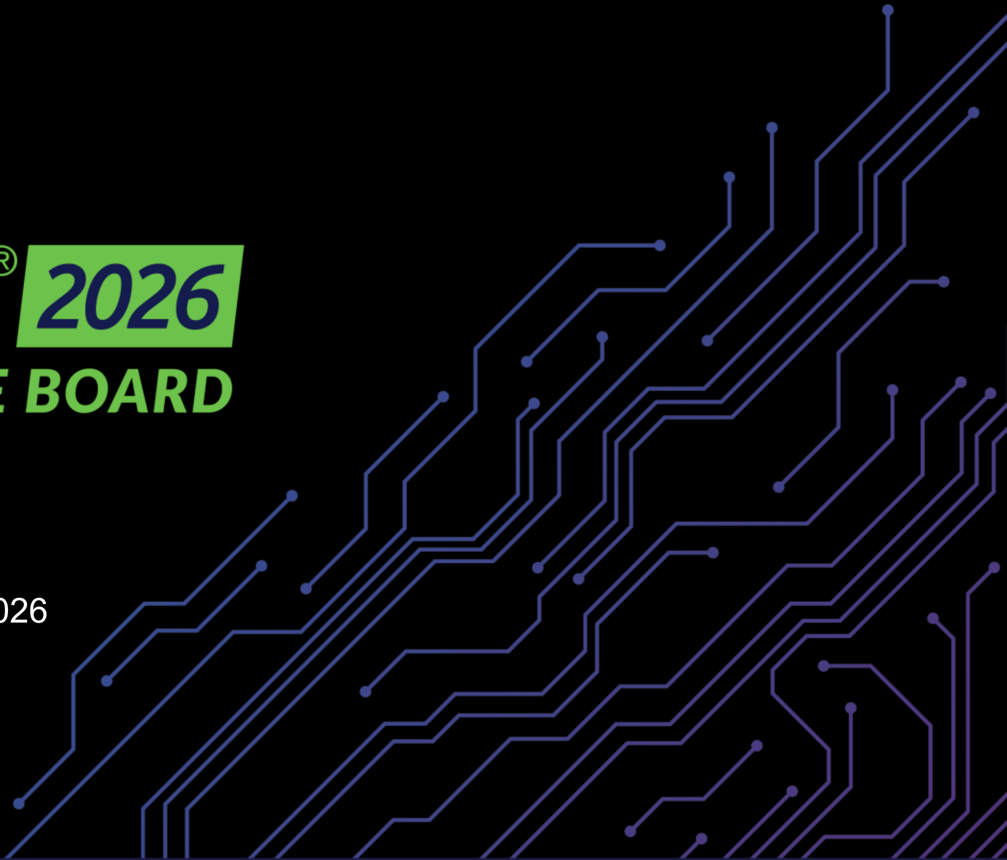
Welcome to

DESIGNCON® 2026

WHERE THE CHIP MEETS THE BOARD



Conference

February 24–26, 2026

Santa Clara Convention Center

Expo

February 25–26, 2026

Improving Spectral Efficiency by Optimizing Sub-Nyquist Equalization for 448 Gbps

Andrew Josephson, (Samtec)
Brandon Gore, (Samtec)

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Francesco de Paulis (Univ. L'Aquila), Luis Boluna (Keysight),
John Calvin (Keysight), Rick Rabinovich (Keysight), Mike
Resso (Keysight)*

SPEAKERS

Andrew Josephson

Technologist, Samtec
www.samtec.com

Focusing on emerging data rate interface technology development, maturation and standardization. Andrew was previously Distinguished Member of the Technical Staff at General Dynamics where he contributed to mission critical embedded computing solutions for HPC systems and airborne platforms.

Brandon Gore, PhD

Technologist, Samtec
www.samtec.com

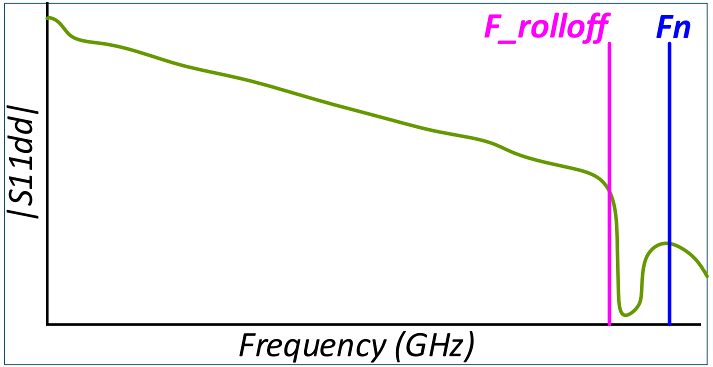
Principal Technologist at Samtec managing both the Signal Integrity R&D and Electronic Industry Standards teams. His research focuses are advanced interconnect materials, packaging, direct drive optics, and general signal integrity bottlenecks beyond 200Gbps data rates. He is an active contributor to IEEE 802.3 and OIF Common Electrical I/O projects.

OUTLINE

- Motivation
- Review some common Channel BW Descriptors
  - Discussion of Spectral Efficiency
- Present 3 Channels for Analysis
  - 2 x Empirical Measurement Based to 110 GHz s-param BW
  - 1 x Simulation Based to 120 GHz s-param BW
- Measurement Emulation Setup (pre-silicon)
  - SerDes equalization settings
- Swept Data Rate Metrics
  - Eye metrics from Keysight FlexDCA
- Conclusions

MOTIVATION

- 425-448 Gbps PAM4 Signaling requires 106 – 112 GHz Nyquist frequencies.
    - Quarter-Wave resonant Stub ~400um in Air.
- Mechanically separable interfaces often drive the achievable roll-off frequency
    - Components and test fixtures frequency domain responses have approached and encroached on signaling Nyquist.
- Classical SI metrics (IL, ILD, RL, Roll-Off Frequency) can describe the channel but recoverability becomes SerDes/DSP dependent.
- This work co-optimizes CTLE-FFE-DFE to recover PAM4 signal up to 425Gbps on channels with **roll-off resonances** near or below **Nyquist**.
- IO intensive compute applications have increased tolerance for engineered solutions.



Can we survive in a Sub-Nyquist channel world?

SPECTRAL EFFICIENCY

- Conceptually, spectral efficiency is how well we get information (bps) through a given channel BW (Hz).
  - Ex. Wifi 7 Signal has a theoretical 46.1Gbps throughput in a 320 MHz channel allocation. (144 bps/Hz).
- From Shannon : ***Spectral Efficiency (η_{ideal}) = $\log_2$(1 + SNR).***
- For a 400G-Class SerDes Phy, we replace $\boldsymbol{\eta_{ideal}}$ with $\boldsymbol{\eta_{achievable}}$ to reflect finite equalization capability and implementation penalties with a SerDes capability factor, $\boldsymbol{\rho_{SerDes}}$,defined as follows:

$$\eta_{achievable} = \boldsymbol{\rho_{SerDes}} \times \log_2(1 + \mathrm{SNR})$$

$$\boldsymbol{\rho_{SerDes}} = \gamma_M \times (1 - \alpha_{FEC}) \times \boldsymbol{\chi_{ISI}} \times \chi_{XT} \times (1 - \alpha_{impl})$$

γ_M represents modulation efficiency

α_{FEC} represents FEC Code overhead

$\boldsymbol{\chi_{ISI}}$ represents ISI recovery capability

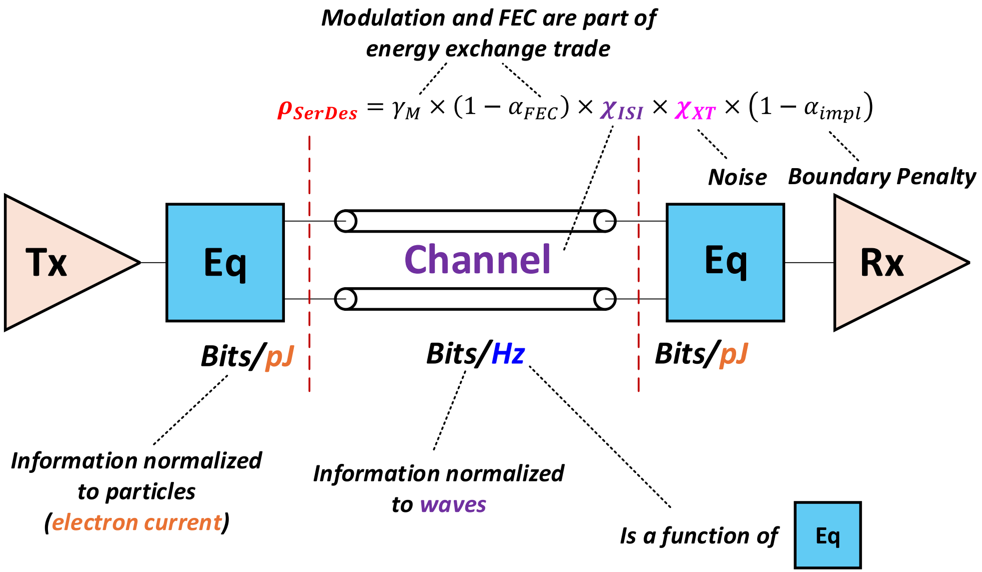
χ_{XT} represents crosstalk penalty

α_{IMPL} represents implementation penalty

- The channel bandwidth is determined by the characteristics of the SerDes.
- $\boldsymbol{\chi_{ISI}}$ is a factor and is the focus for this study.

Channel BW has become firmware defined.

SPECTRAL EFFICIENCY



Modulation and FEC are part of energy exchange trade

$$\rho_{SerDes} = \gamma_M \times (1-\alpha_{FEC}) \times \chi_{ISI} \times \chi_{XT} \times (1-\alpha_{impl})$$

Noise

Boundary Penalty

Bits/pJ

Bits/Hz

Bits/pJ

Information normalized to particles (electron current)

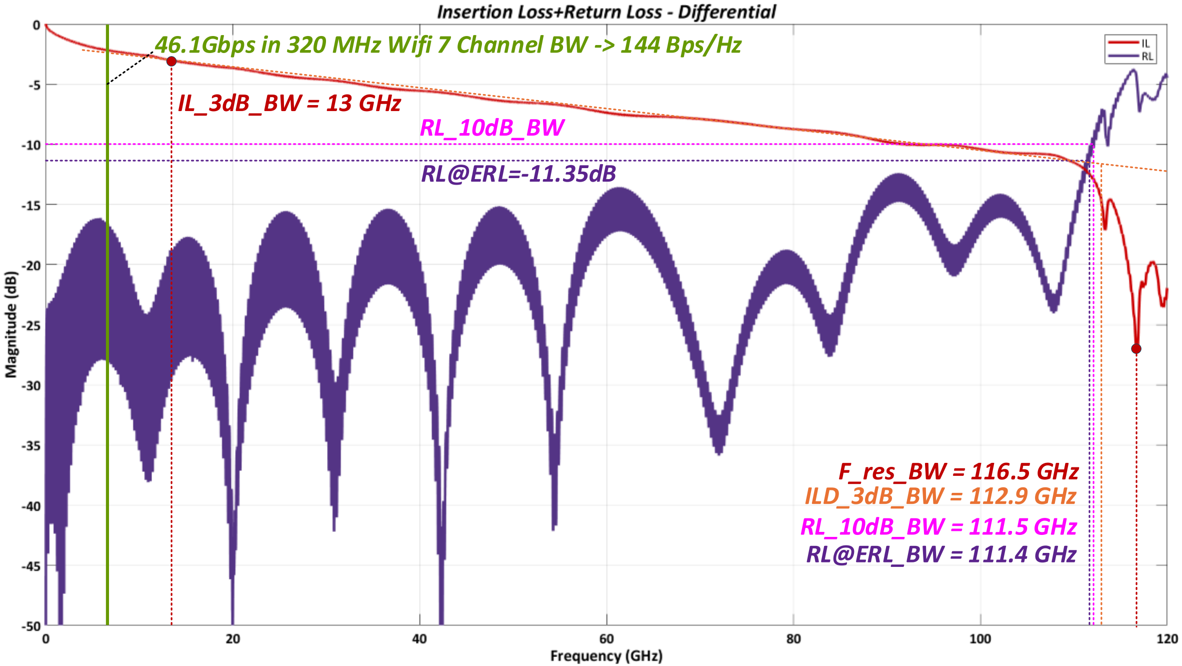
Information normalized to waves

Is a function of Eq

- **1 bit represents 2 reliably distinguishable physical sates** carried by waves or particles.
- **Spectral Efficiency (bits/Hz)** is how much spectral BW those states consume.
- **Energy per bit (pJ/bit or mW/Gbps)** is how much particle-side energy must be injected to keep those states distinguishable in noise.
- **Equalization** utilizes both energy and computational resources to maximize the amount of recoverable bandwidth within a channel **exchanging pJ/bit for bits/Hz**.

Design Goal: Co-Optimize Spectrum, Energy and SerDes Equalization Capability to maintain state separation.

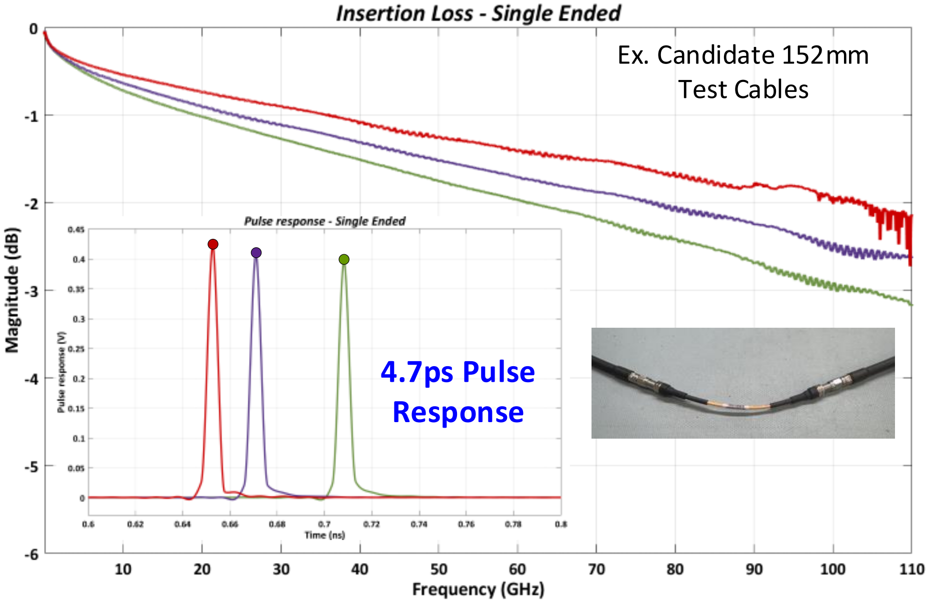
DESCRIPTIONS OF CHANNEL BANDWIDTH



- Insertion Loss at Frequency
- Insertion Loss Deviation
- Rolloff Frequency
- Return Loss BW (ERL)
- Pulse Height
- ICR

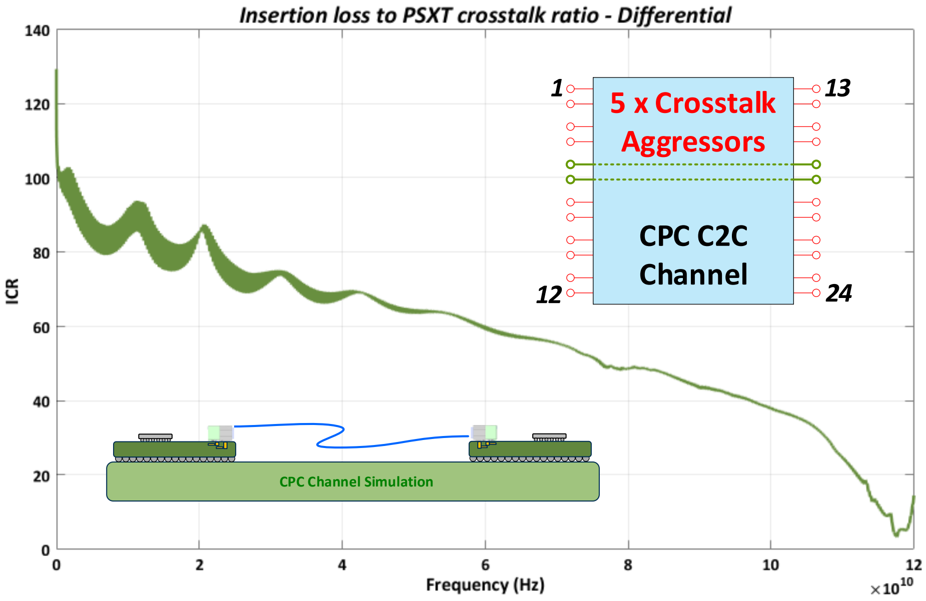
What channel BW do we use to estimate spectral efficiency when considering a 400G-Class SerDes?

DESCRIPTIONS OF CHANNEL BANDWIDTH


Insertion Loss - Single Ended

Ex. Candidate 152mm Test Cables

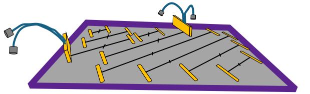
4.7ps Pulse Response


Insertion loss to PSXT crosstalk ratio - Differential

What channel BW do we use to estimate spectral efficiency when considering a 400G-Class SerDes?

CHANNEL TYPES

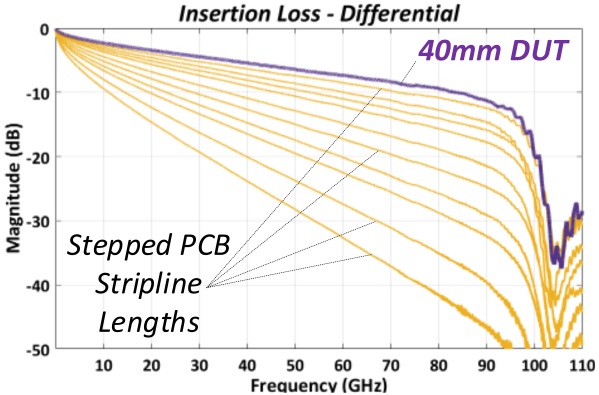
CHANNEL EMULATOR DESCRIPTION



DUT1 – Meas. Stripline Chan. Emu.

Coax to Stepped Stripline Chan. Em.

	Thickness (um)	Construction	Material	Datasheet Dk	Datasheet Df	Via Padstacks	Via Padstacks
L01	52	18um + Plating	~HVLP2			410	405
D01	99	2X1035 (65%)	ULL Preg	2.73	0.0011	150	150
L02	15	1/2 Oz	HVLP4			320	
D02	102	2X1035 (66%)	ULL Core	2.72	0.0011		
L03	15	1/2 Oz	HVLP4				
D03	228	3X1078LRC (63%)	ULL Preg	2.73	0.0011		
L04	15	1/2 Oz	HVLP4				
D04	102	2X1035 (66%)	ULL Core	2.72	0.0011		
L05	15	1/2 Oz	HVLP4			320	
D05	99	2X1035 (65%)	ULL Preg	2.73	0.0011	150	
L06	52	18um + Plating	~HVLP2			410	405



- 152mm Coax + 1.5dB/inch (@53GHz) PCB Striplines
  - Single laminate blind laser via Break out Region (BOR) resonates at 103GHz
  - 128um wide, 50 Ohm SE BUS routes

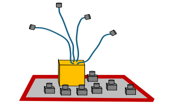
Summary Description of fixture measurements

https://www.ieee802.org/3/ad_hoc/E4AI/public/25_0430/josephson_e4ai_01_250430.pdf

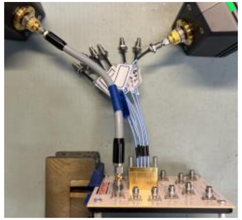
S-Parameter data available for download

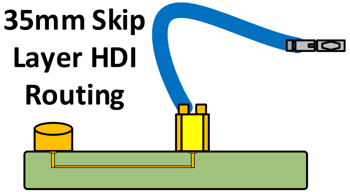
https://grouper.ieee.org/groups/802/3/ad_hoc/E4AI/public/channel/C2M/josephson_e4ai_03_250430.zip

COAXIAL C2M DESCRIPTION

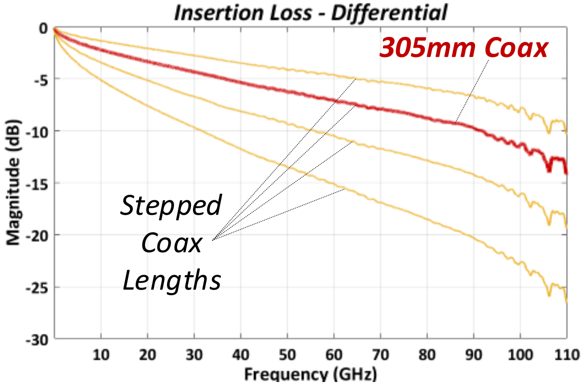

DUT2 – Measured Coaxial C2M

HDI Substrate to Stepped Coax C2M





Coax high water mark for C2M topology

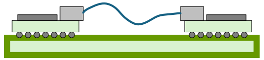


	Thickness (um)	Construction	Material	Datasheet Dk	Datasheet Df		Via Padstacks		Via Padstacks	
L01	38	3/8oz. + Plating	STD				215			
D01	76	1X1078 (67%)	ULL Preg	2.84	0.0015		100			
L02	25	3/8oz. + Plating	HVLP2				215		215	
D02	76	1X1078 (67%)	ULL Preg	2.84	0.0015				100	
L03	25	3/8oz. + Plating	HVLP2				215		215	
D03	76	1X1078 (67%)	ULL Preg	2.84	0.0015		100			
L04	25	3/8oz. + Plating	HVLP2				215		215	
D04	76	1X1078 (67%)	ULL Preg	2.84	0.0015				100	
L05	25	1/2 oz. + Plating	HVLP2				215		215	
D05	76	1X1078 (64%)	ULL Core	2.84	0.0015		100			
L06	25	1/2 oz. + Plating	HVLP2				215		215	
D06	76	1X1078 (67%)	ULL Preg	2.84	0.0015				100	
L07	25	3/8oz. + Plating	HVLP2				215		215	
D07	76	1X1078 (67%)	ULL Preg	2.84	0.0015		100			
L08	25	3/8oz. + Plating	HVLP2				215		215	
D08	76	1X1078 (67%)	ULL Preg	2.84	0.0015				100	
L09	25	3/8oz. + Plating	HVLP2				215		215	
D09	76	1X1078 (67%)	ULL Preg	2.84	0.0015		100			
L10	38	3/8oz. + Plating	STD				215			

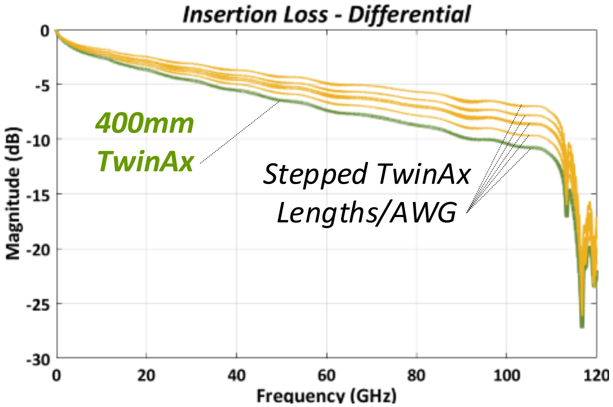
- 305mm Coax + 1.65dB/inch (@53GHz) PCB Striplines
  - Any layer stacked laser via Break out Region (BOR) resonant free to 110GHz
  - 218um wide, 50 Ohm SE BUS routes from skip layer reference plane

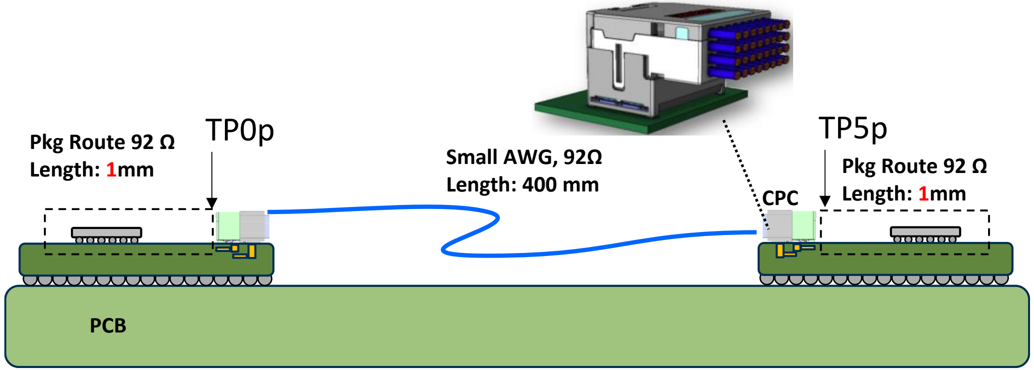
S-Parameter data available for download
https://grouper.ieee.org/groups/802/3/ad_hoc/E4AI/public/channel/C2M/josephson_e4ai_02_250430.zip

C2C MODEL CHANNEL DESCRIPTION



- CPC C2C Topology representative of GPU-to-GPU mesh (Intra-Tray)
- Exploratory, simulation-based channel models to identify future design space
- Connector model includes shallow vertical substrate transition and neglects long PKG routing.
  - Channel boundary has just enough PKG trace to establish good TEM boundary on ports at TP0p/TP5p.





CPC Channel Simulation

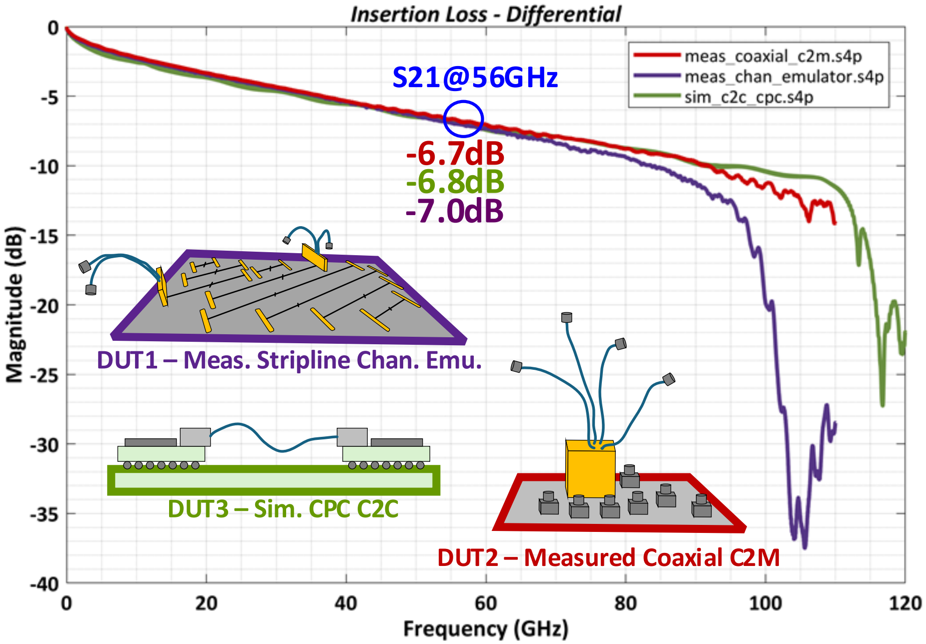
Summary Description of channel model

https://www.oiforum.com/bin/c5i?mid=4&rid=7&gid=0&k1=55229

S-Parameter data available for download

https://www.oiforum.com/bin/c5i?mid=4&rid=7&gid=0&k1=55229&k2=1&k3=3

CHANNEL S-PARAMETERS



S21@56GHz

-6.7dB

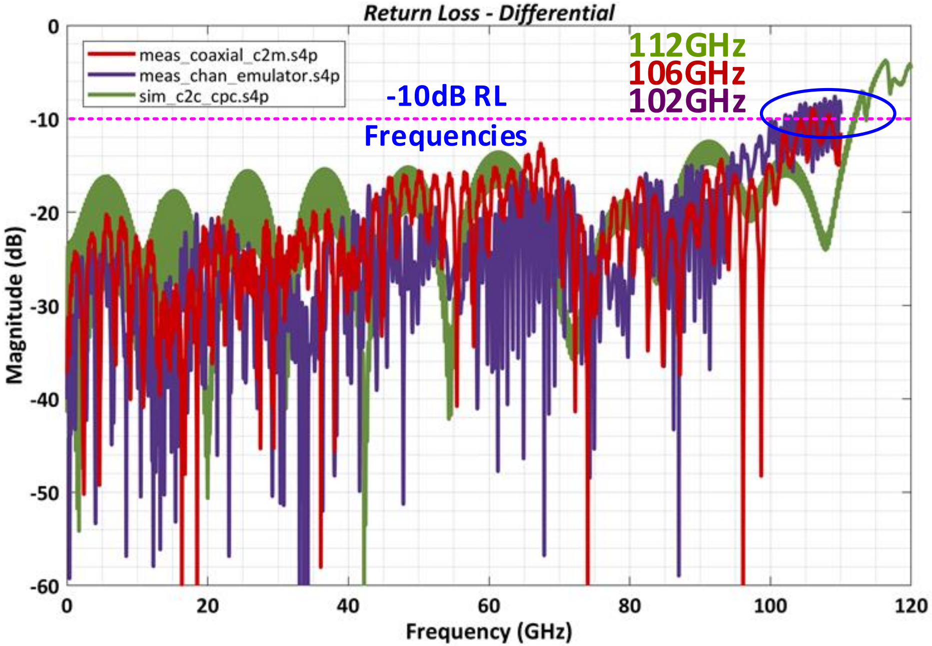
-6.8dB

-7.0dB

DUT1 – Meas. Stripline Chan. Emu.

DUT3 – Sim. CPC C2C

DUT2 – Measured Coaxial C2M



-10dB RL

Frequencies

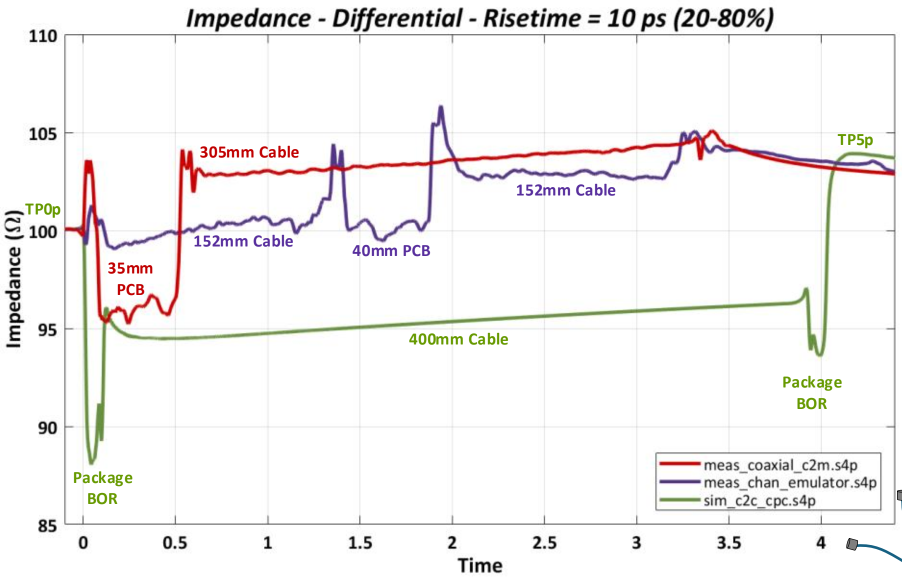
112GHz

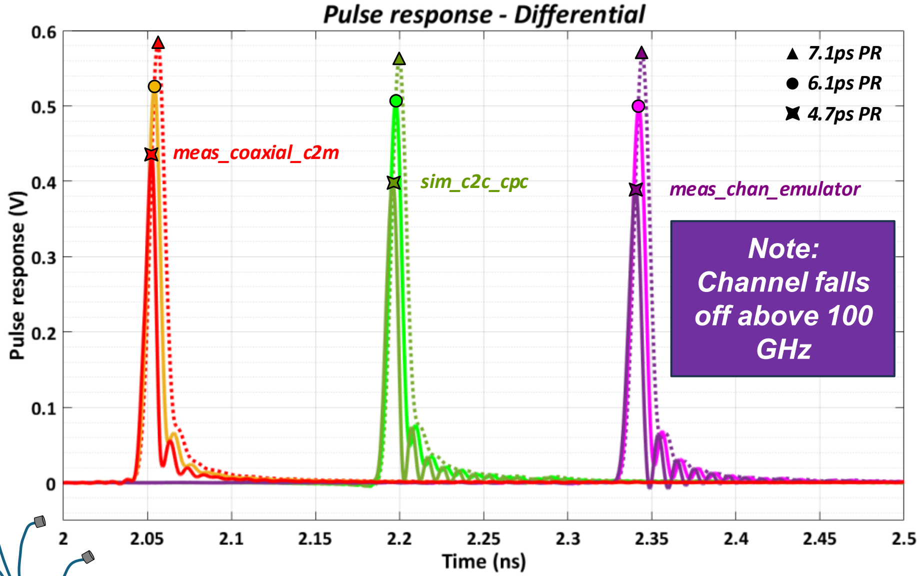
106GHz

102GHz

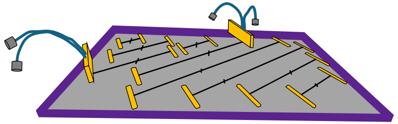
Nearly Identical 212Gbps IL Channels : Deviation above 95GHz

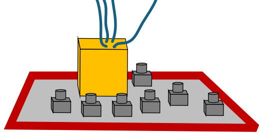
CHANNEL TIME DOMAIN RESPONSES

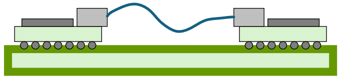




Note: Channel falls off above 100 GHz


DUT1 – Meas. Stripline Chan. Emu.

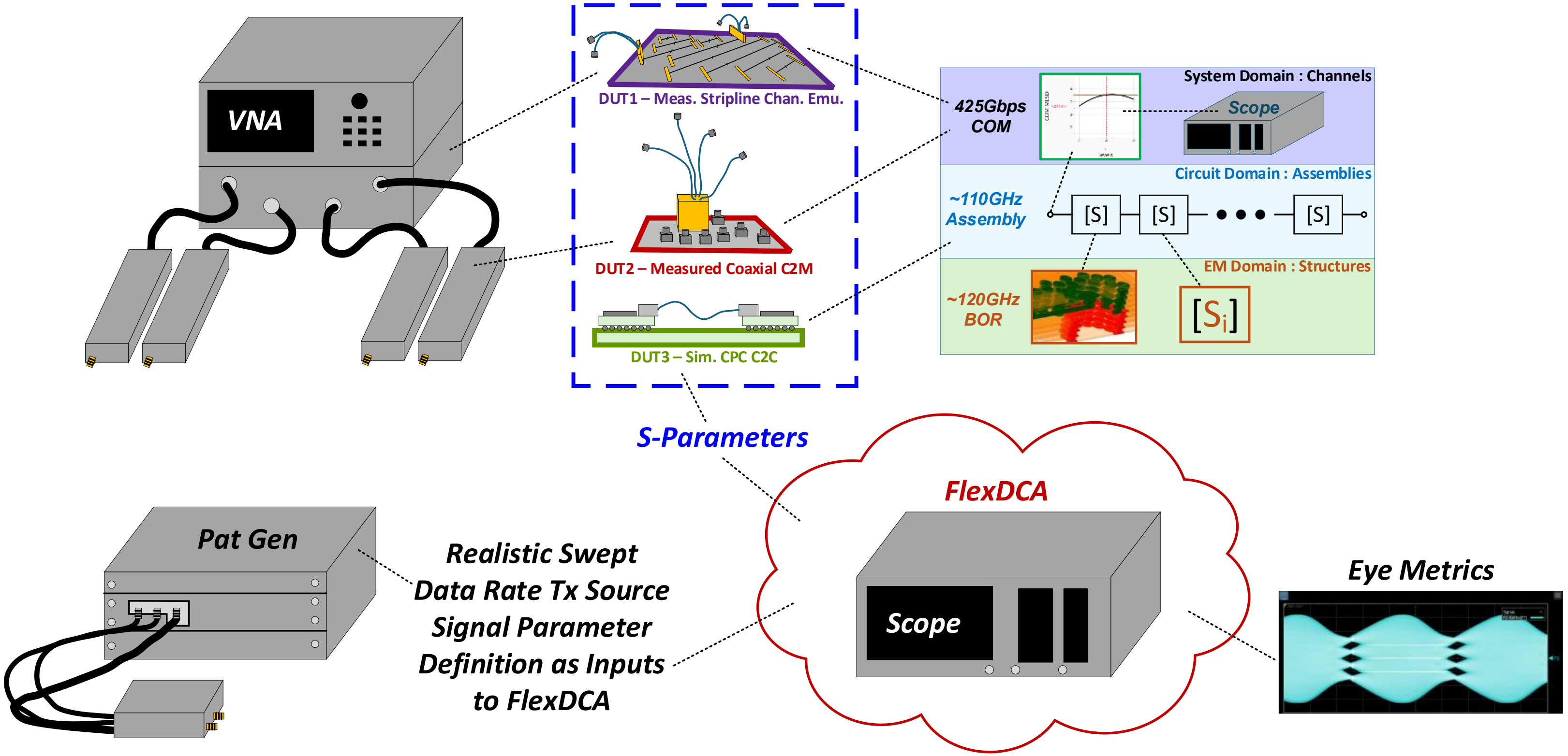

DUT2 – Measured Coaxial C2M


DUT3 – Sim. CPC C2C

4.7ps (400Gbs PAM4) Pulse Height Correlates to IL Trend to ~80GHz

MEASUREMENT EMULATION

CHANNEL MEASUREMENT EMULATION



VNA

DUT1 – Meas. Stripline Chan. Emu.

DUT2 – Measured Coaxial C2M

DUT3 – Sim. CPC C2C

System Domain : Channels

425Gbps
COM

Scope

Circuit Domain : Assemblies

~110GHz
Assembly

[S] [S] • • • [S]

EM Domain : Structures

~120GHz
BOR

$[S_i]$

S-Parameters

Pat Gen

Realistic Swept
Data Rate Tx Source
Signal Parameter
Definition as Inputs
to FlexDCA

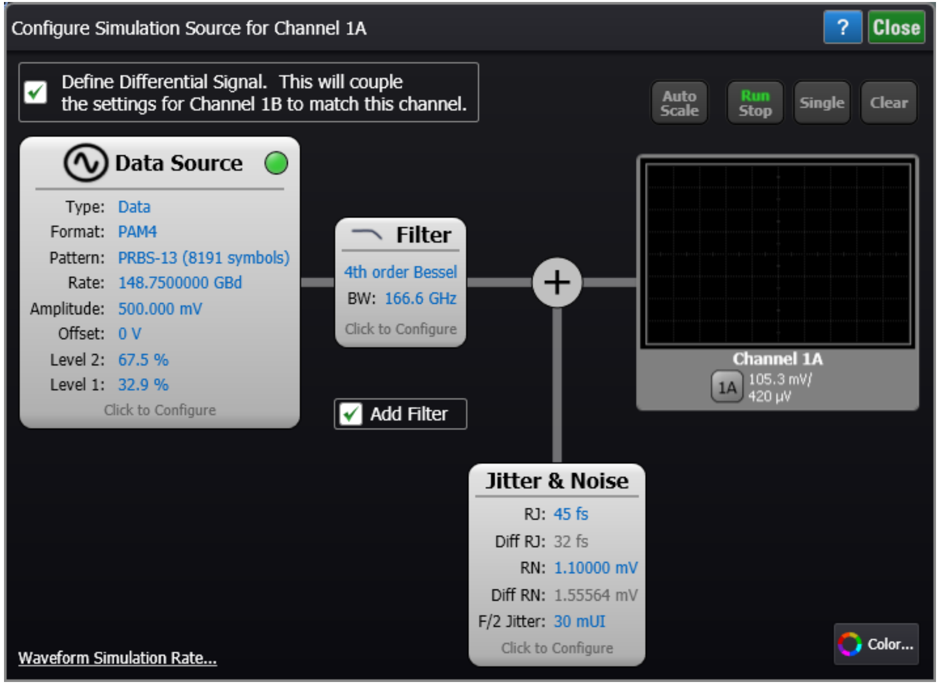
FlexDCA

Scope

Eye Metrics

EMULATION SETUP – TX ASSUMPTIONS

- R_{LM} = 0.95
  Symbol Level 1 and 2 set to 32.9% and 67.5%.
- σ_{RJ} = 32 fs differential random jitter (45 fs for the single-ended)
- A_{DD} = 30 mUI Dual-Dirac model deterministic jitter.
- V_N = 1.1 mV random noise amplitude



Configure Simulation Source for Channel 1A

☑ Define Differential Signal. This will couple the settings for Channel 1B to match this channel.

Data Source

Type: Data
Format: PAM4
Pattern: PRBS-13 (8191 symbols)
Rate: 148.7500000 GBd
Amplitude: 500.000 mV
Offset: 0 V
Level 2: 67.5 %
Level 1: 32.9 %
Click to Configure

Filter

4th order Bessel
BW: 166.6 GHz
Click to Configure

☑ Add Filter

Jitter & Noise

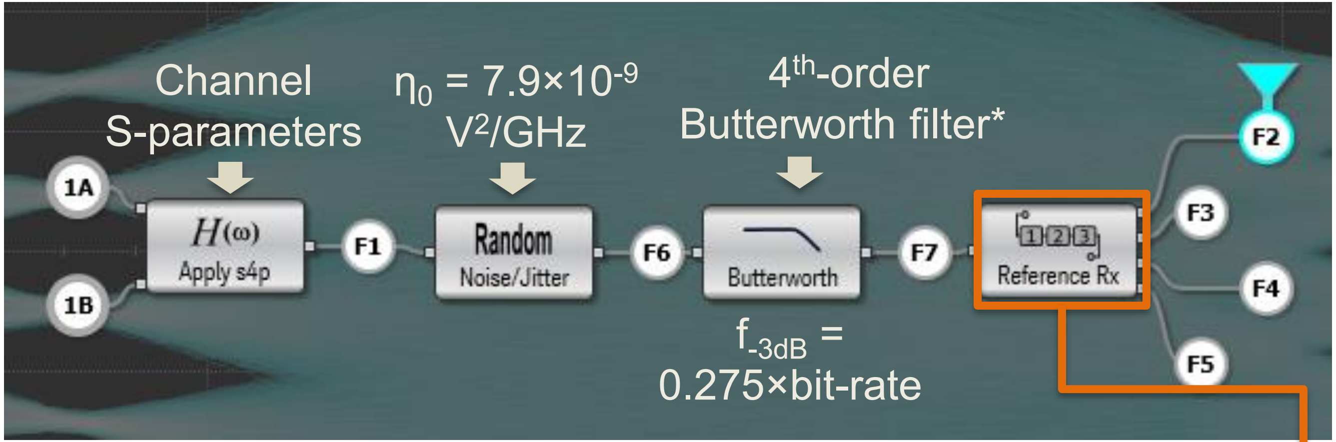
RJ: 45 fs
Diff RJ: 32 fs
RN: 1.10000 mV
Diff RN: 1.55564 mV
F/2 Jitter: 30 mUI
Click to Configure

Channel 1A
1A 105.3 mV/ 420 µV

Waveform Simulation Rate...

Virtual tools enable pre-silicon Design of Experiments (DoE) in validation flows.

EMULATION SETUP – RX ASSUMPTIONS



Channel S-parameters

$\eta_0 = 7.9\times10^{-9}$ V^2/GHz

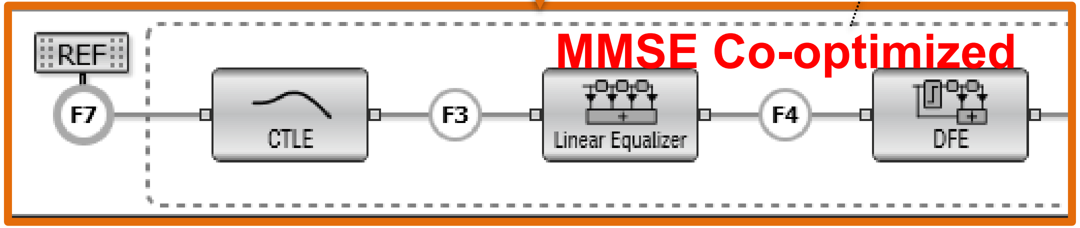
4th-order Butterworth filter*

$f_{-3dB} =$ 0.275×bit-rate

2-stage CTLE

$$H_{CTLE}(f) = \frac{\left(10^{\frac{g_{DC}}{20}} + j\frac{f}{f_z}\right)\left(10^{\frac{g_{DC2}}{20}} + j\frac{f}{f_{LF}}\right)}{\left(1 + j\frac{f}{f_{p1}}\right)\left(1 + j\frac{f}{f_{p2}}\right)\left(1 + j\frac{f}{f_{LF}}\right)}$$

Non-LTI



MMSE Co-optimized

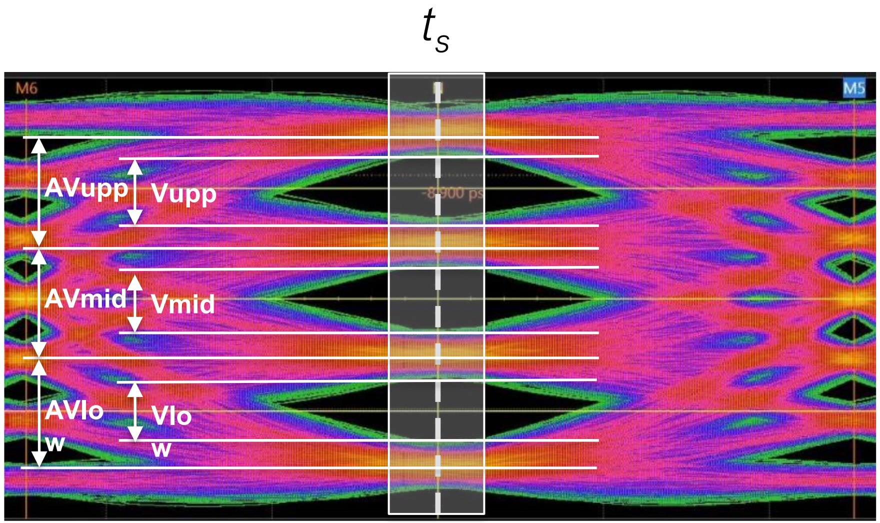
30-taps FFE
8 pre-cursors
21 post-cursors

1-tap DFE

*In lieu of SIRC

VERTICAL EYE CLOSURE (VEC)

VEC is a statistic measure over a window around t_s



VEC (Vertical Eye Closure)

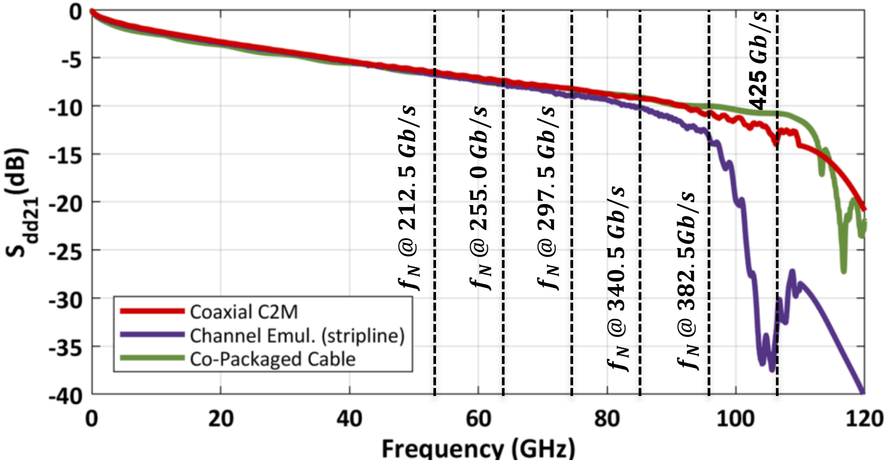
$$\mathrm{VEC} = \boldsymbol{20 * log10\left(\frac{AVupp}{Vupp}, \frac{AVmid}{Vmid}, \frac{AVlow}{Vlow}\right)}$$

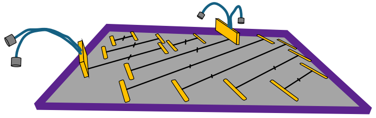
AVxxx = Eye Amplitude
Vxxx = Eye Height

Reference: “A Novel Approach to 224 Gb/s Reference Receiver Design Using Raised Cosine Response for Noise Mitigation” DesignCon 2023

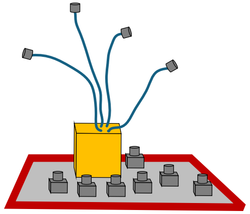
DATA-RATE SWEEP

- The bit-rate is swept from 212.5 Gbps to 425 Gbps
- Corresponding frequency settings are applied to the TX and RX filters, and to the CTLE poles/zeros

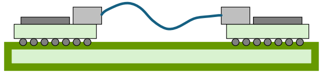




DUT1 – Meas. Stripline Chan. Emu.



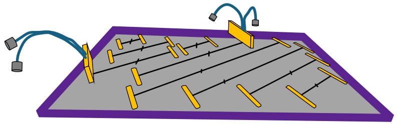
DUT2 – Measured Coaxial C2M



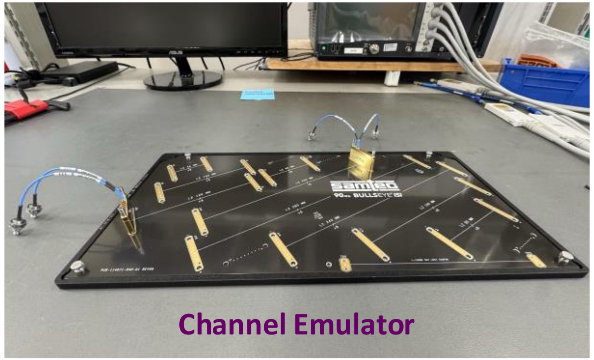
DUT3 – Sim. CPC C2C

Bitrate	Baud-rate f_b	Nyquist freq. f_N	RX 4th Butterworth filter f_r	CTLE Settings (GHz)			
Gb/s	Gbaud	GHz	1.1×f_N	f_{LF}	f_z	f_{p1}	f_{p2}
212.5	106.25	53.125	58.4375	0.66	42.5	42.5	106.25
255.0	127.5	63.75	70.125	0.80	51	51	127.5
297.5	148.75	74.375	81.8125	0.93	59.5	59.5	148.75
340.5	170	85	93.5	1.06	68	68	170
382.5	191.25	95.625	105.1875	1.20	76.5	76.5	191.25
425.0	212.5	106.25	116.875	1.33	85	85	212.5

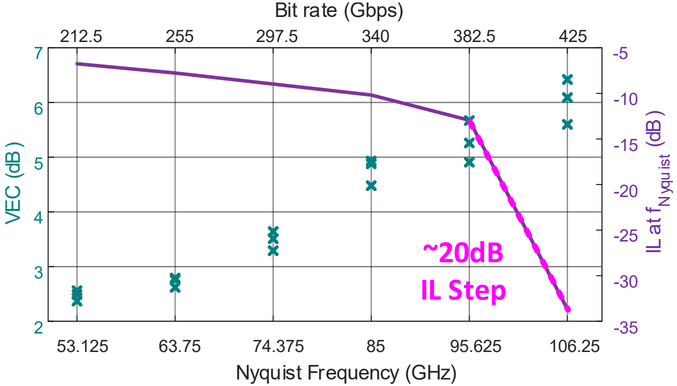
DUT1 – STRIPLINE CHANNEL EMULATION

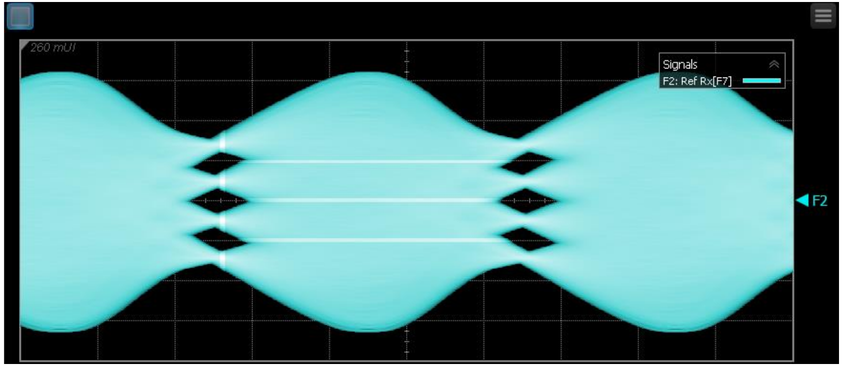


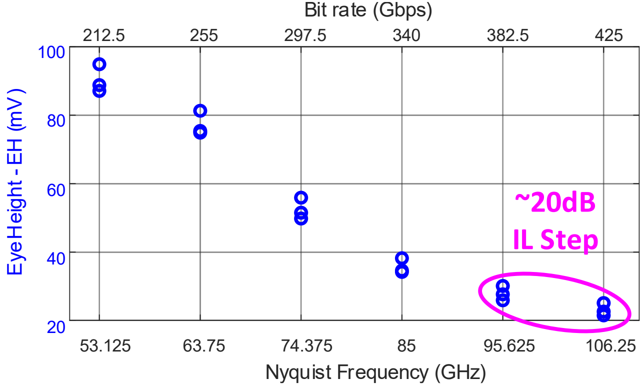
DUT1 – Meas. Stripline Chan. Emu.



Channel Emulator

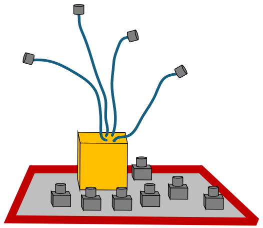




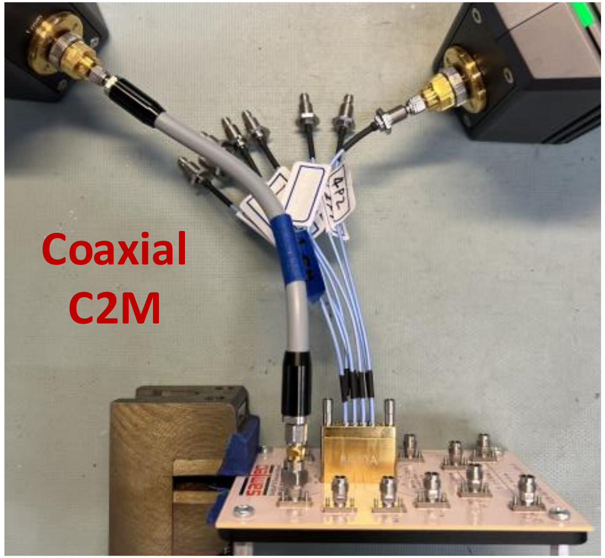


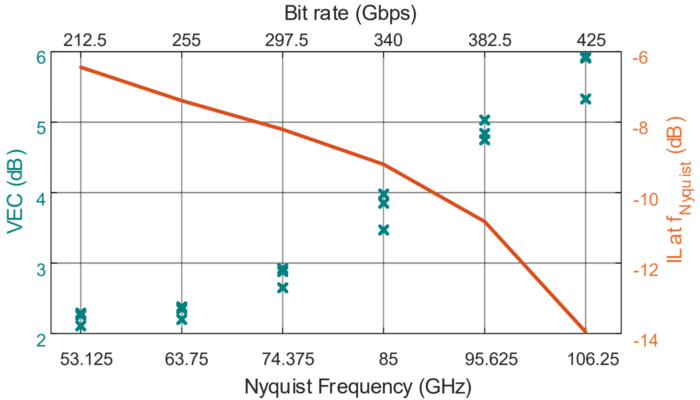
400G Class SerDes Eq. maintains eye height metrics across the -20dB IL step with expected pJ/bit penalty.

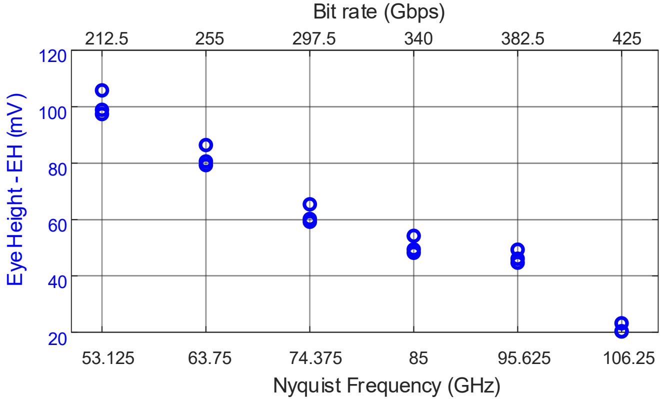
DUT2 – COAXIAL CHIP-TO-MODULE



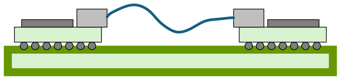
DUT2 – Measured Coaxial C2M



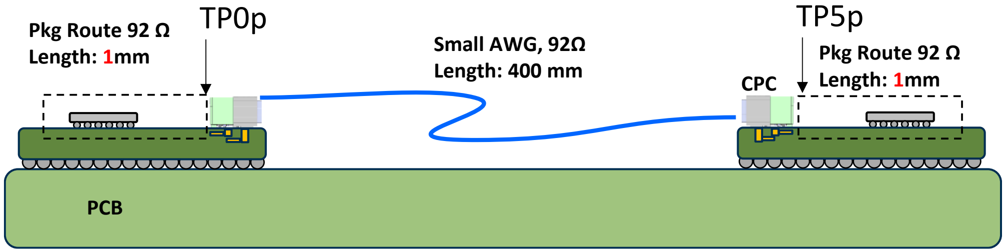




DUT3 – CO-PACKAGED CABLE



DUT3 – Sim. CPC C2C



Pkg Route 92 Ω
Length: 1mm

TP0p

Small AWG, 92Ω
Length: 400 mm

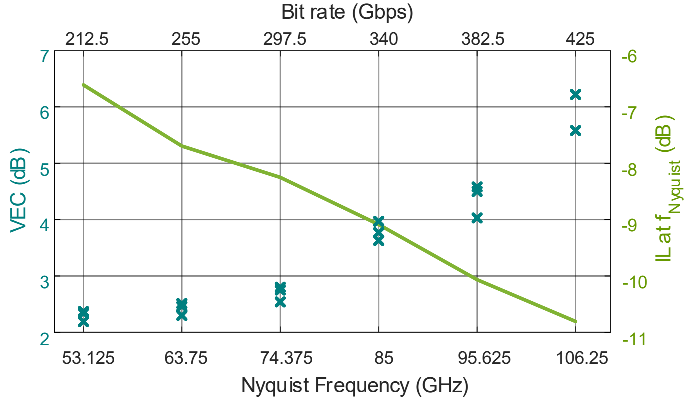
TP5p

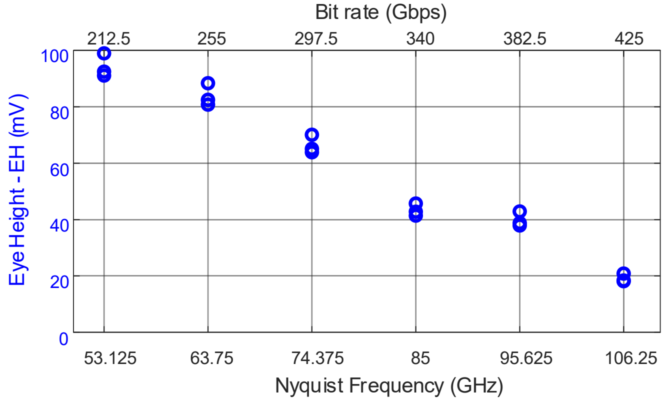
CPC

Pkg Route 92 Ω
Length: 1mm

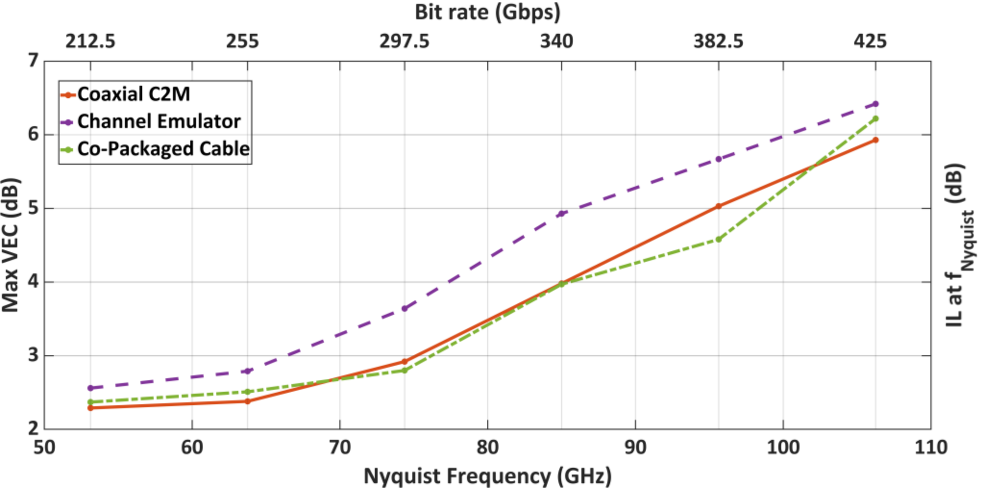
PCB

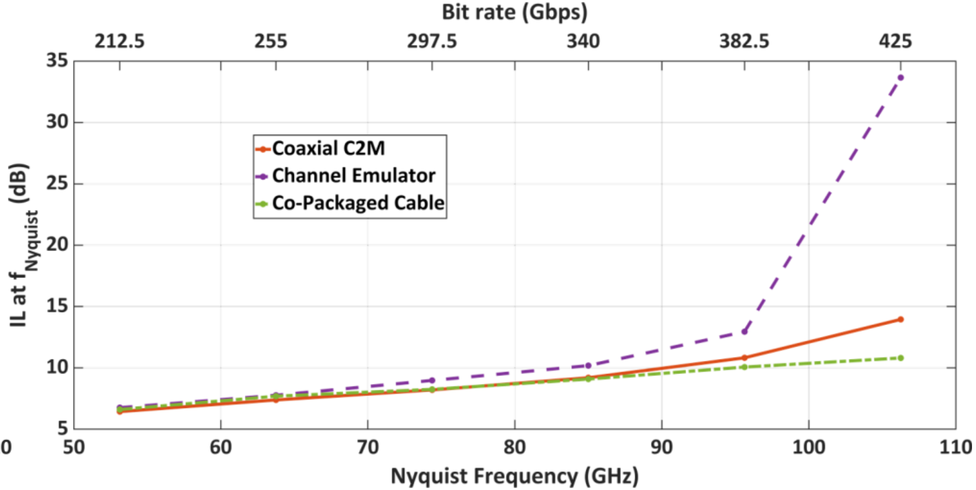
CPC Channel Simulation

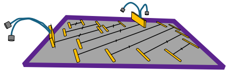




VEC and IL at Nq Do Not Correlate > 100 GHz

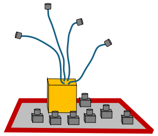






DUT1 – Meas. Stripline Chan. Emu.

DUT 1



DUT2 – Measured Coaxial C2M

DUT 2

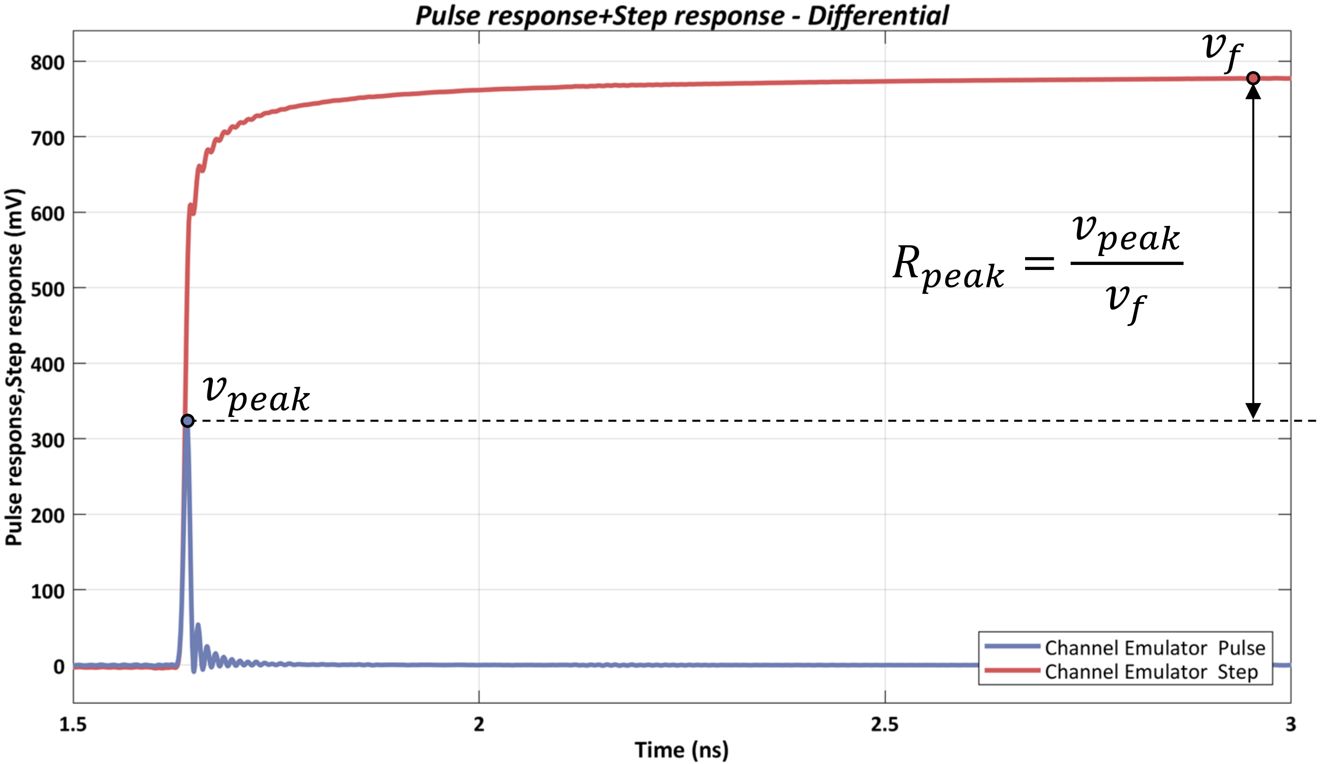
DUT3 – Sim. CPC C2C

DUT 3

Baseband signaling over Sub-Nyquist channels causes miscorrelation in channel performance prediction when using IL at Nq.

Rpeak: Ratio of Pulse Peak (v_{peak}) to Steady State Voltage

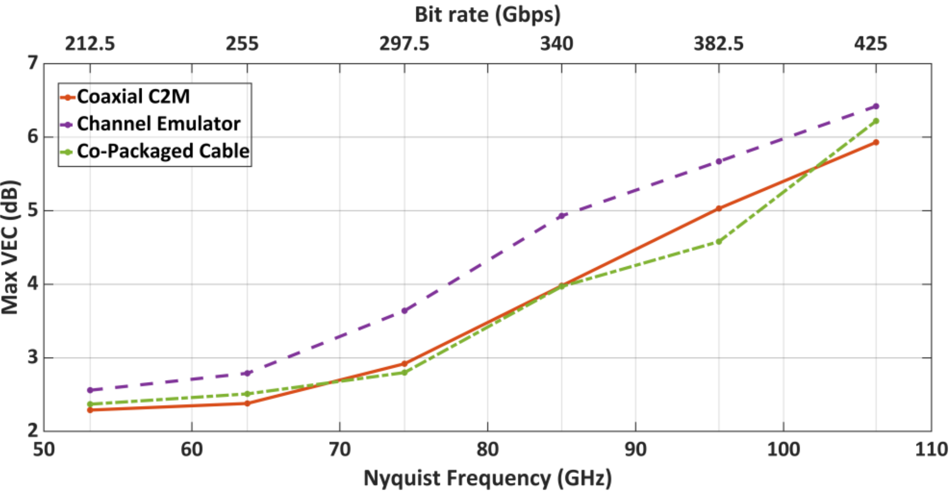
Novel application of Rpeak to the channel sparameter as an alternative to IL at Nq.

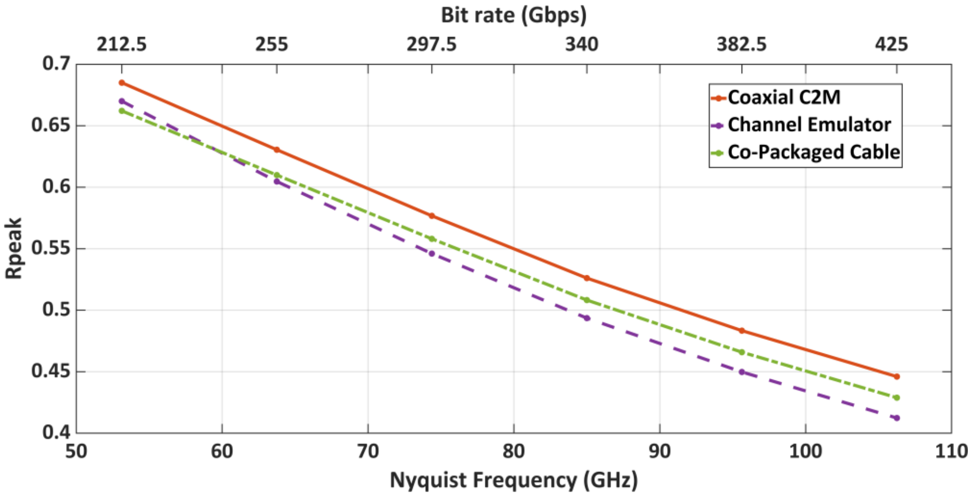


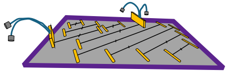
$$R_{peak} = \frac{v_{peak}}{v_f}$$

Rpeak for Tx and Hosts defined in: IEEE Std 802.3ck – 2022: *100 Gb/s, 200 Gb/s, 400 Gb/s Electrical Interfaces Task Force,* Annex 151, Eq 163A-9

COMPARISON (VEC and Rpeak)

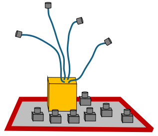






DUT1 – Meas. Stripline Chan. Emu.

DUT 1



DUT2 – Measured Coaxial C2M

DUT 2

DUT3 – Sim. CPC C2C

DUT 3

Rpeak offers a better indication of signaling recovery. Additional ISI bounding metrics can compliment Rpeak.

CONCLUSIONS AND DISCUSSION

Improvements in ISI recovery capability (χ_{ISI})

- This work demonstrated an acceptable VEC for a sub-Nyquist 425Gbps channel.
    - Pre-silicon measurement emulation setup with test fixtures
    - Further ongoing work to optimize a channel given sub-Nyquist components.
- Evolve emulation setup to real HW in the loop as component/fixture technology mature.
- Rpeak is becoming a predictive metric for signal recovery compared to insertion loss.
- Near-Nyquist pulse-shaping filters allow the transmitter to occupy less bandwidth while still delivering the required symbol energy.
    - Transmitter-side precoding techniques may offload early ISI cleanup from the receiver.
- IO intensive compute applications favor engineered solutions. And at baseband, they challenge the notions of spectral efficiencies.

Thank you!

QUESTIONS?