Welcome to

DesignCon® 2026

WHERE THE CHIP MEETS THE BOARD

Conference
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Santa Clara Convention Center

Expo
February 25–26, 2026

Lessons Learned at 224 Gbps

Steve Krooswyk, (Samtec)
John Calvin, (Keysight)
Todd Bermensolo, (Alphawave/Qualcomm)
Liam Parkes, (Samtec)
Moderator: Greylan Smoak, Samtec

SPEAKERS

Steve Krooswyk

SI Engineer, Samtec

Liam Parkes

Application Engineering Manager for Emerging Technologies, Samtec

John Calvin

Strategic Planner, Network and Data Center Infrastructure, Keysight

Todd Bermensolo

Principal Engineer and SerDes IP product leader , Alphawave/Qualcomm

Moderator

Greylan Smoak

SI Engineer, Samtec

TOPICS

- **SI learnings**: Steve Krooswyk:
- **Test & Measurement**: John Calvin
- **Silicon IP implementations & interoperability**: Todd Bermensolo
- **System issues, customer's point of view**: Liam Parkes
- **Q&A**

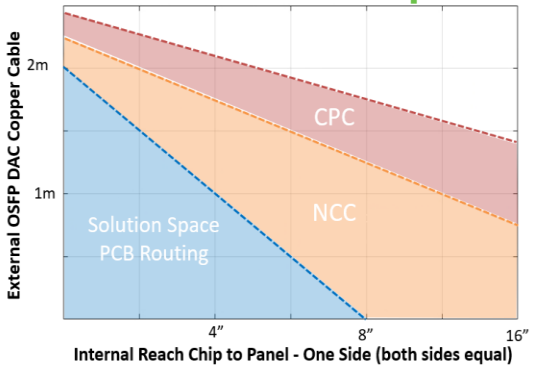
SI learnings

Steve Krooswyk
Senior SI Engineer Samtec

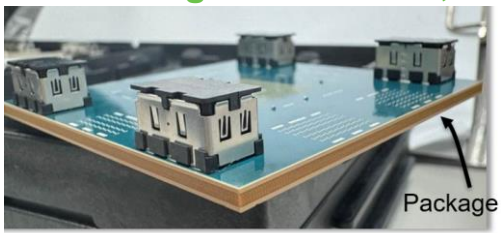
224G Key Learnings

- Early head-winds questioned near-chip ‘through the board’ feasibility
- Prototyping the industry’s smallest CPC connector faces impedance & mechanical robustness questions
  - ➡ New metal housing, footprint grows a little bit
- We’re not in vacuum - partnerships aid in design success
- Everyone is concerned with solder robustness
  - ➡ Validation vehicles build the confidence
- CPC assembly order depends on validation strategy
- Difficult to design Si validation fixtures with at least 67GHz de-embedding capability for connectors & cable
- Ultra low skew twinax cable – development and test

224G Solution Space



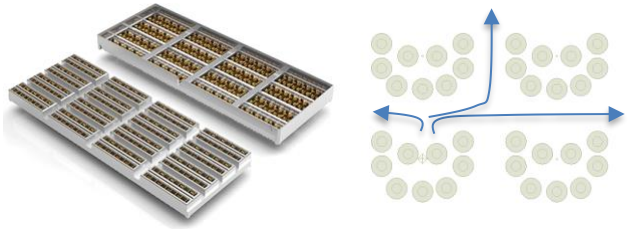
First Package Attachment, 2024



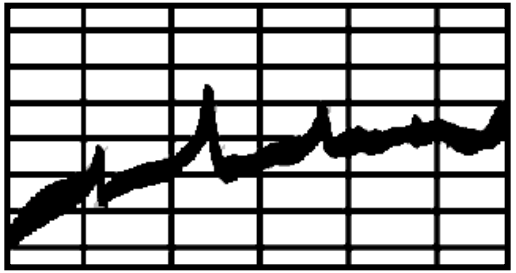
224G Key Learnings

- Through the package and onto the board would be too much loss, right?
  - Aggressive foils & materials 1.3-1.5db\inch make near chip and SMT OSFP possible
- Near chip cables & mezzanines need flexibility to manage cable bend, PCB loss, and PCB skew reduction
  - >2.0mm between rows balances flexibility & density
- Edge cards in legacy offerings like OSFP will have crosstalk resonances below Nyquist frequencies
  - Full link analysis shows little sensitivity from resonance
- OSFP form factor update to reduce edge card wipe extended OSFP lifespan into 224G-PAM4

On the Board Flexibility



Crosstalk Resonances Have Negligible Effect on Margins



224G Key Learnings

- Increased silicon capabilities enhance noise rejection enable 40dB reach
  - Rx FFE w\ MMSE optimization and MLSD capabilities
  - Improved package loss over previous generation
  - Creative asymmetric package budgets to achieve greater reach
- We all asked “What is skew?”
  - Greater tolerance over the last generation
  - More meaningful metrics (SCMR) over normalized Sdc
- Increased interoperability in the standards for interconnect
  - Common mode noise requirements may not need to be as restrictive
  - Trending validation through ERL, more meaningful specs w\ modal ERL
- Open Source COM – enhanced community participation

Test & Measurement

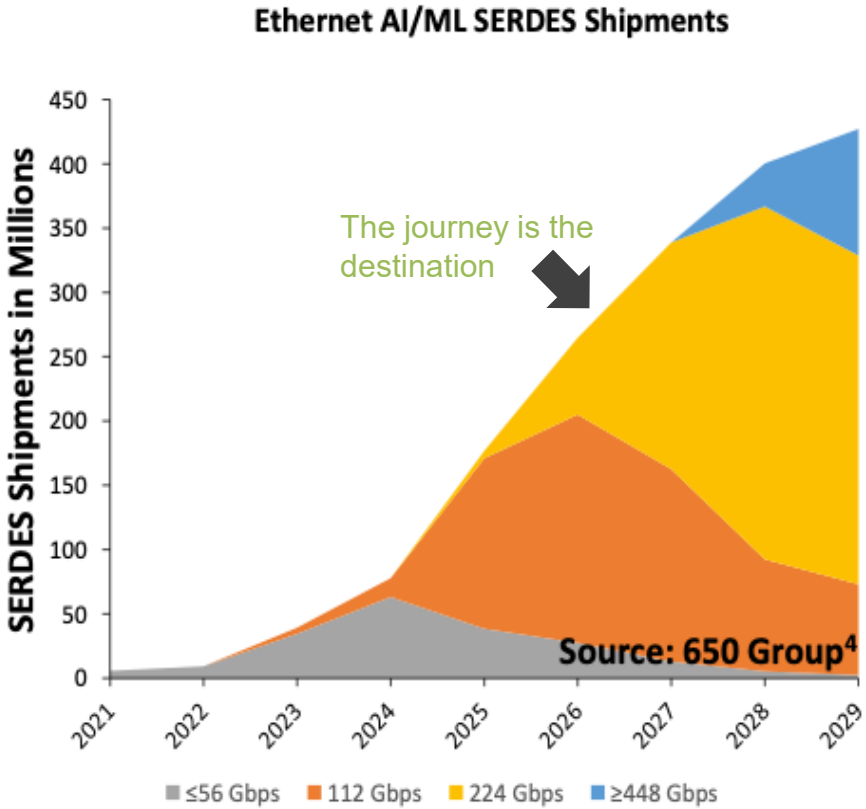
John Calvin
Strategic Planner Keysight Technologies

Test & Measurement:

- The AI industry has created a wave between the collision of the high-performance computing needs of large language models and our collective knowledge of signal transmission and computational physics
- At the physical layer the systematic doubling of the signaling Nyquist frequency into higher loss regions has necessitated increasingly sophisticated Tx and Rx equalization systems
- Measurement technology is tracking these advances and has made leaps in improving measurement accuracy and repeatability, which has been essential to this ecosystem

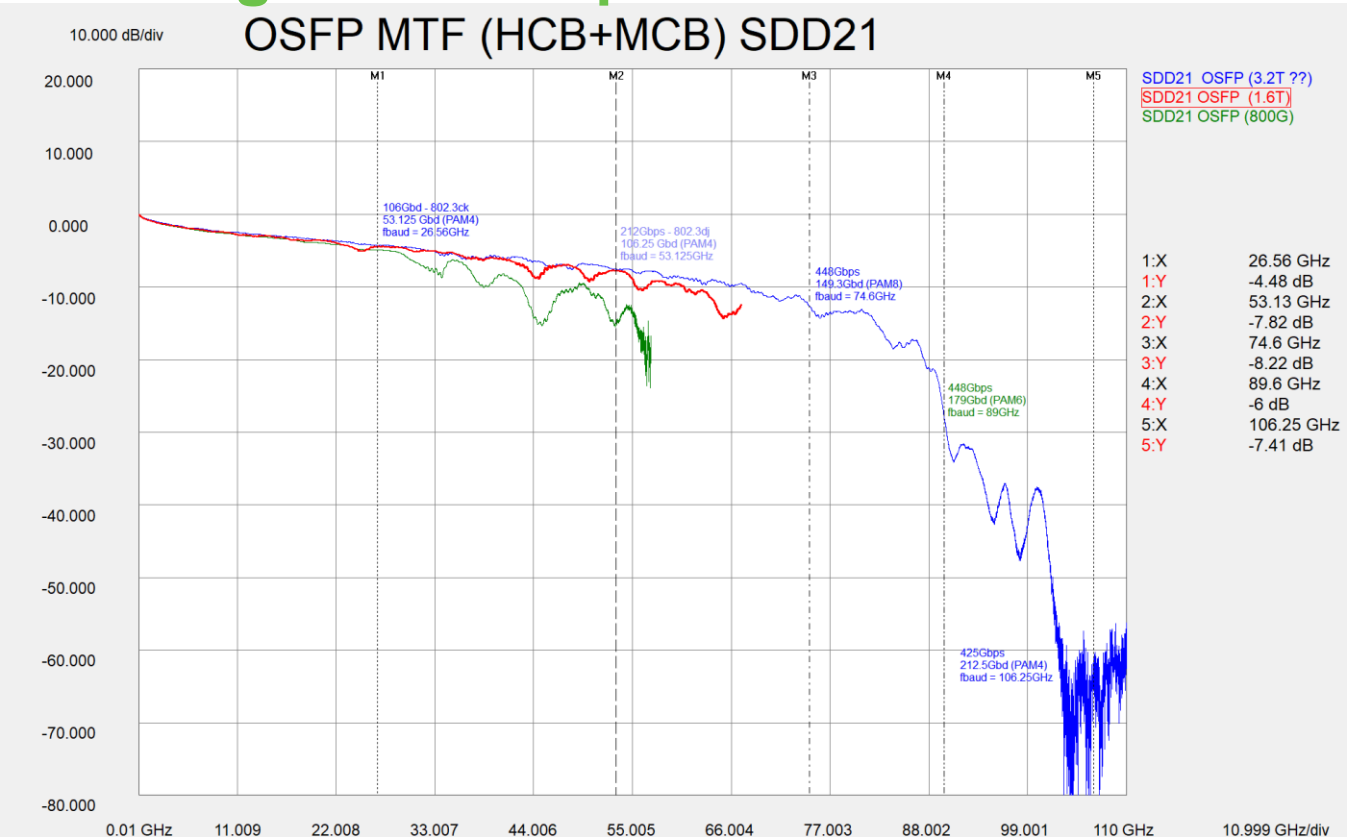
Industry Cycles are Compressing

- The Back-end scale-up part of this ecosystem is expanding 100x faster than front-end or scale-out.
- Due to scale-up interconnects now being measured in 100E6 units, power consumption and link reliability have become principal design parameters
- Everyone is getting into this business because.. How many $1.6T markets are there with over 25% growth?
- Many companies are jettisoning their 6G sea-anchors and focusing 448G and 880Gbps technology revolution for scale-up networking.

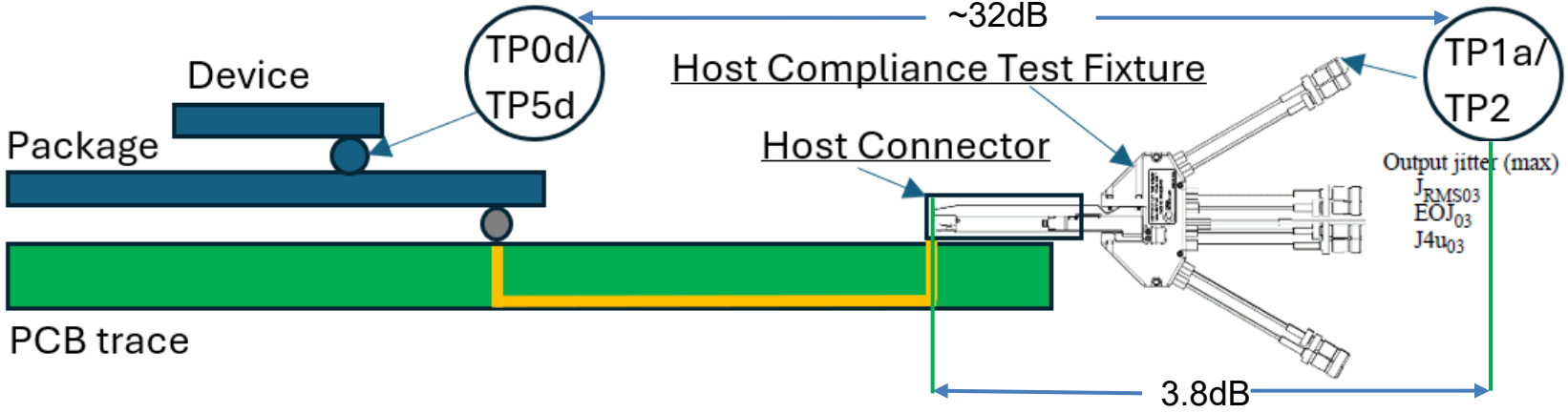


High Speed Networking.. Channel performance evolution

- The edge of the electrical channel map as we know it today ends at 120GHz.
- Moving into higher transmission speeds will require learning about dielectric and transmission properties for new electro-mechanical assemblies and materials.



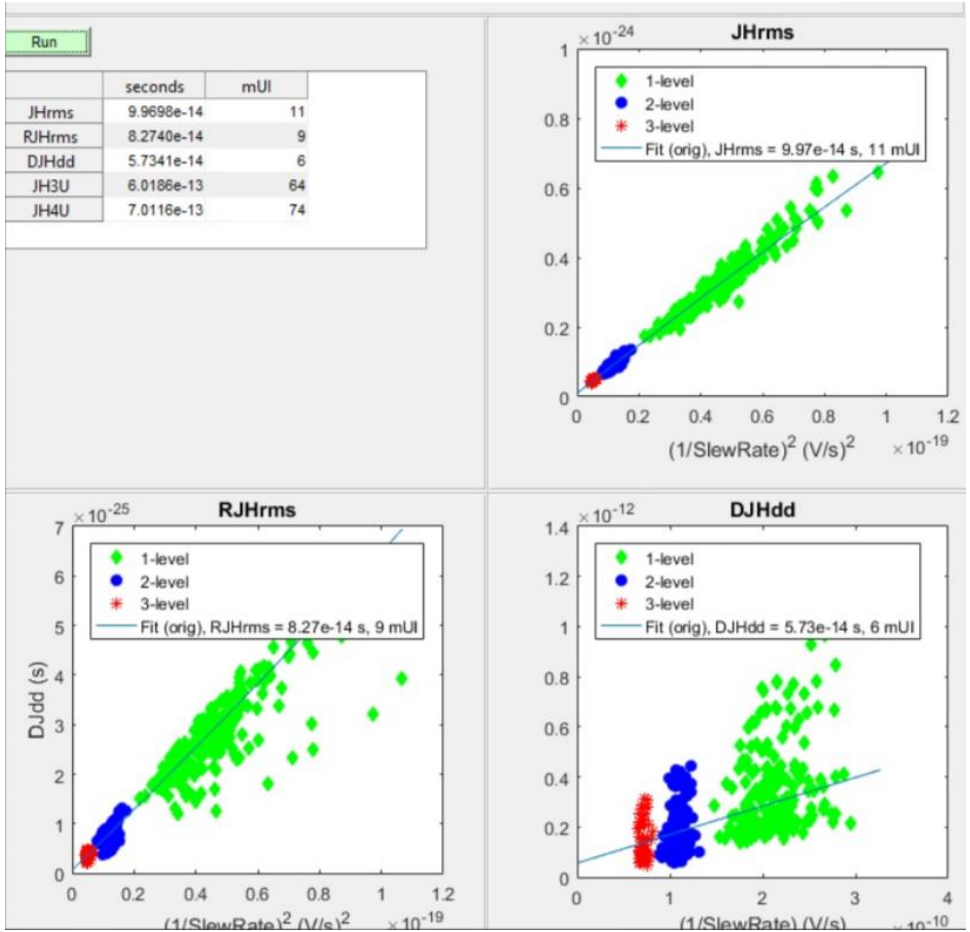
IEEE 802.3dj D2.0 TP0d->TP1a/TP2 loss



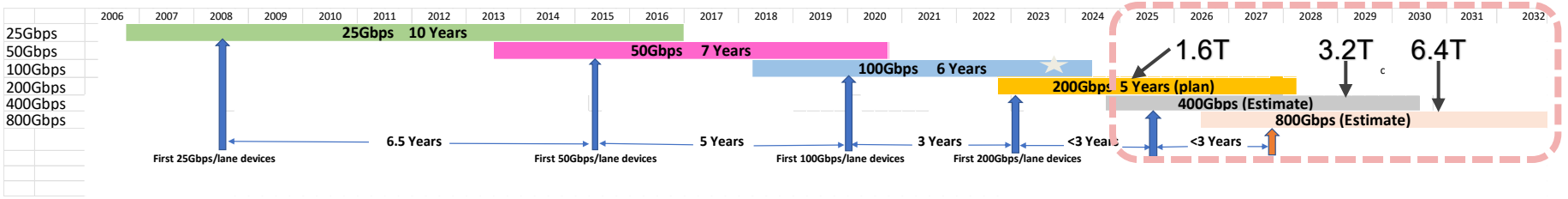
- The worst-case chip-to-module loss in 802.3dj (212Gbps/lane) in nominally 32dB. Recall our last generation this number was nominally 15dB. This 50:1 electrical signal loss makes high precision measurements “complicated”.

Advances in Phase Only Jitter (POJ) J4U

- As was originally committed in : Gines 01/09/2025: [JHRMS technical overview and proposal for channel independent Jitter measurements] .. An improved method of J4u extraction was proposed that is “Channel loss independent”
- At the November 10 - 14, 2025 IEEE 802 plenary All IEEE 802.3 Task Force session a new Jitter technique for an improved JH4u methodology was ratified.



The High Speed Networking Crystal Ball



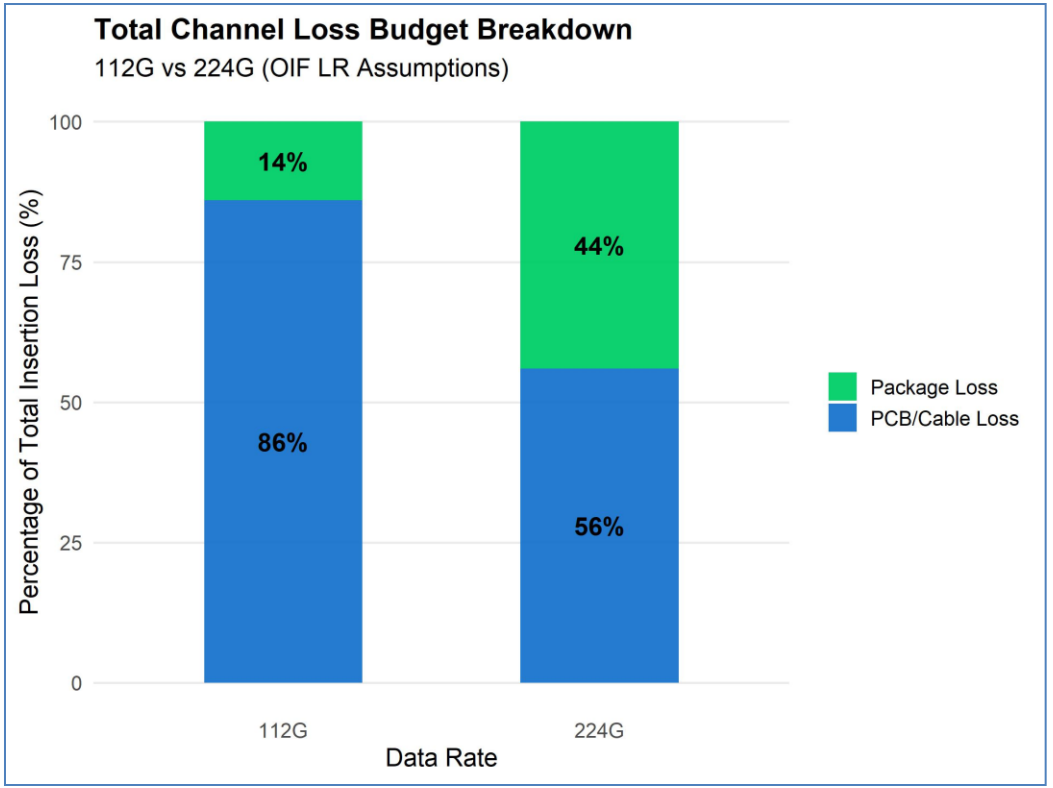
- The good old days of 10 year design cycles at a given speed are now a thing of the past. The current technology design cycle is cycling presently at around 3 years between next generation silicon releases.
- The Test Equipment field is ramping up to follow this cadence. Lot's of new tools are on the roadmap.
- Working in the physical sciences of signal transmission now suddenly the cool thing to be doing.
- Within 10 years we will be building single lane signaling solutions at 5Tbps. The traditional "brick walls" have actually been opportunities for disciplined engineering organizations to out-maneuver their lesser competitors.

Silicon IP implementations & interoperability

Todd Bermensolo
SerDes IP Product Leader, Alphawave Semi/Qualcomm

Package Matters

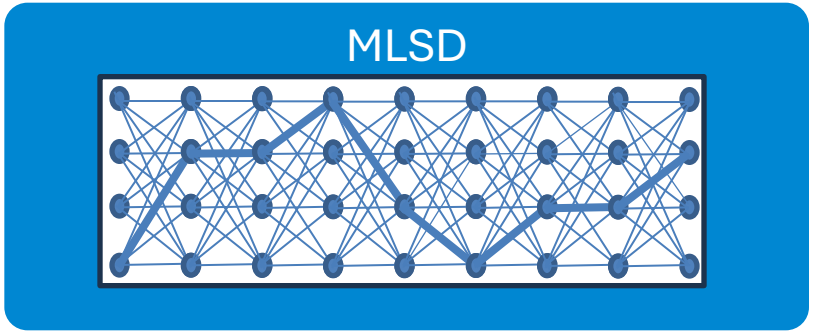
- The Package is the New Bottleneck
  - Standard Evolution: Shift from Ball-to-Ball (112G) to Die-to-Die (224G/OIF) compliance definitions reflects the critical impact of the package.
- Loss Budget Shift:
  - At 112G, package loss was a manageable overhead (~14% of budget).
  - At 224G, package insertion loss can consume 40%+ of the total 40dB channel budget.

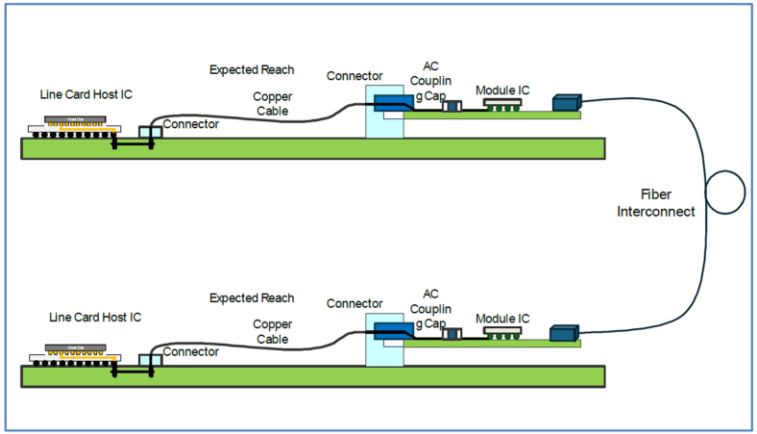


Silicon IP Implementation Challenges

- Silicon IP features
  - Maximum Likelihood Sequence Detection. Relies on sequence detection versus symbol-by-symbol detection.
  - MLSD was optional at 112G, now required at 224G-LR.

- Interoperability
  - Linear Pluggable Optics (LPO) is becoming pain point.
    - *LPO is challenging because it removes the DSP safety net. While this reduces power and latency, it fundamentally changes the interoperability model from a "digital link" to an "analog" one.*
    - *Host SerDes to handle the combined electrical and optical channel impairments directly.*
    - *At 200G (802.3dj), the physics of signal loss and bandwidth limitations make this "analog" link incredibly difficult to standardize.*

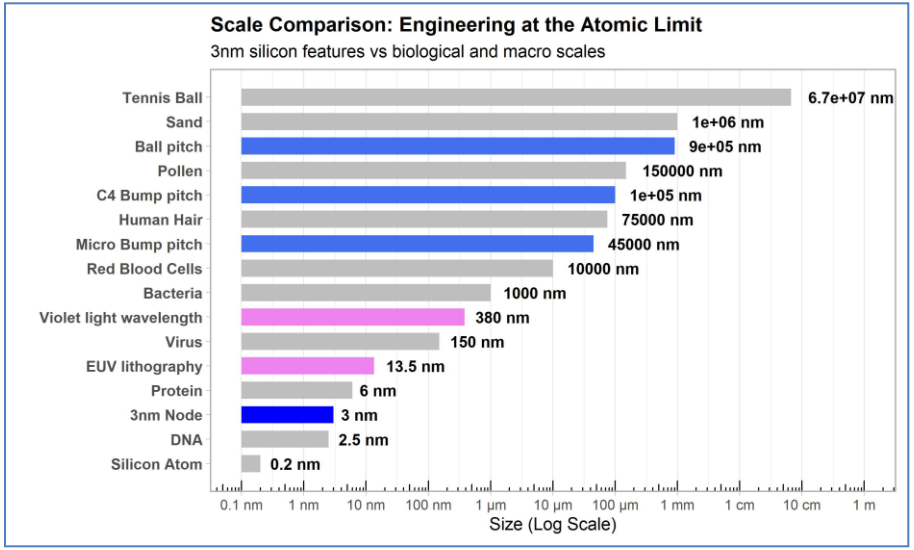


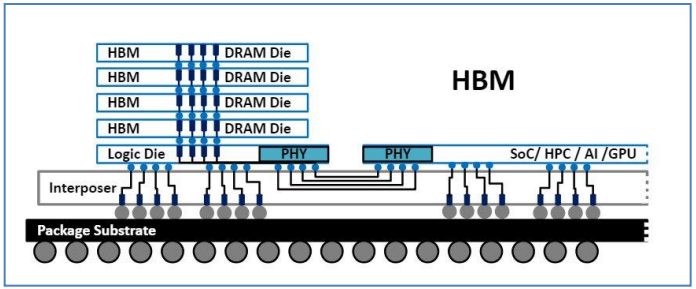


- Source: OIF Linear IA

Power & Area Efficiency

- Advanced silicon process nodes required:
  - Achieving acceptable pJ/bit targets for 224G mandates migration to 3nm silicon nodes.
  - Added cost and IP complexity.
- Advance packaging (2.5D) to increase density:
  - System-on-package: compute, memory, I/O
  - 224G applications driven by AI factories. Better performance and efficient if you integrate.
    - *Multi-die solutions can go larger than single die solutions.*
- Physical Scale: To improve power and area efficiency, we are engineering down to the atomic limit.
  - Silicon bump pitch is comparable to width of human hair.
  - 3nm silicon feature is comparable in width to a strand of human DNA.





https://awavesemi.com/redefining-xpu-memory-for-ai-data-centers-through-custom-hbm4/ --- 11.15.2024

System Issues and Customer Point of View

Liam Parkes

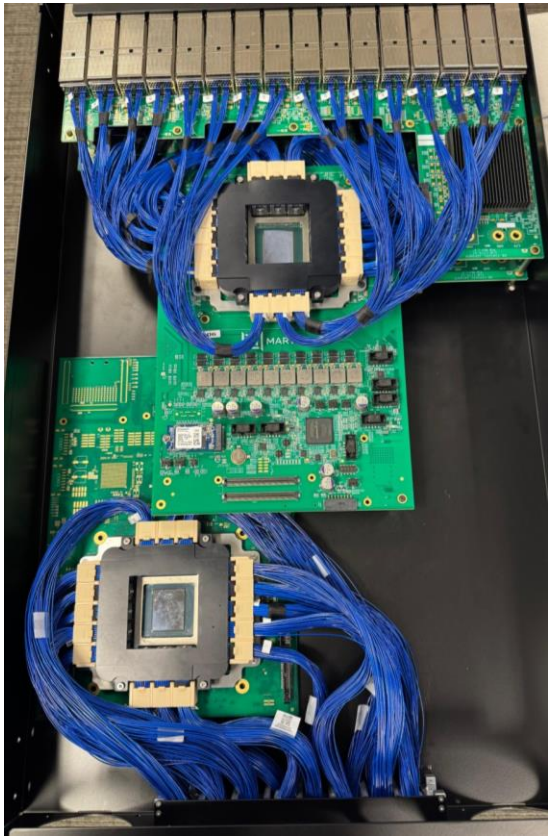
Application Engineering Manager for Emerging Technologies at Samtec

System Issues, Customer POV

- 224G systems are moving even more signals to FlyOver style cabling
- Cable size increasing to minimize loss, DP per connector increasing to maximize density
  - In Samtec's case, 112G typically used 32 DP of 34 AWG wire, 224G is using 64 DP of 32 AWG wire
  - Other solutions go larger!
- Design engineers need to develop a plan for cable install early in the process
  - Samtec offers complimentary assistance with cable routing design

System Issues, Customer POV

- Integration between Samtec & customer is critical to program success
- SI rules for next-gen systems, but the system still has to be built!
  - Manufacturability & rework must be considered
- High levels of customization enables next gen system architectures
- Full suite of products necessary to meet the market's needs
  - Product
  - Support
  - Delivery



Thank you!

QUESTIONS?

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MORE INFORMATION

- Achieving 224 Gbps PAM4: New Interconnect Methods to Ensure Signal Integrity (white paper)
- Are 1mm Precision RF Connectors Required for 224 Gbps (DesignCon Best Paper)

Samtec Booth #939
Keysight Booth #1039