Developing a Test Fixture for 200G with Pathway to 400G

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ABSTRACT

While industry organizations, such as OIF and IEEE, develop and formalize standards for 400 Gbps signaling, a currently available method to examine and extrapolate the behavior of 400+Gbps signals could be extremely useful when making design decisions about future 400Gbps architectures and test platforms. This paper details the development of an ultra-high bandwidth 200 Gbps multi-lane test platform that offers the additional benefit of serving as an early development tool for 400 Gbps characterization in the lab.

Keywords: 448Gbps, 224Gbps, 400G, PAM4, Test Fixture

1. INTRODUCTION

Test and integration engineers working on 224 Gbps PAM4 designs will also be considering performance requirements for devices and systems using emerging 400 Gbps signaling. While industry organizations, such as OIF and IEEE, develop and formalize standards for 400 Gbps signaling, a currently available method to examine and extrapolate the behavior of 400+Gbps signals could be extremely useful when making design decisions about future 400Gbps architectures and test platforms. This paper details the development of an ultra-high bandwidth 200 Gbps multi-lane test platform that offers the additional benefit of serving as an early development tool for 400 Gbps characterization in the lab [1].

2. RELATED WORK

This work is supported by work presented at DesignCon 2024 and DesignCon 2023.

3. DESIGNING 110GHZ TEST PLATFORMS

This project began with defining a component evaluation board for the new Samtec BE90 compression-mount test assembly. The BE90 (and its predecessors, including the BE70) are often used in SerDes evaluation and characterization. The development of this evaluation board later led to the concept of the Bulls Eye® ISI multi-lane SerDes channel emulator test fixture.

The BE90 Test System Evaluation Board (Figure 1) was designed to test the 90 GHz, Bulls Eye® Double Row, High-Performance Test System which is optimized for operation up to 90 GHz in support of 224 Gbps PAM4 SerDes testing.

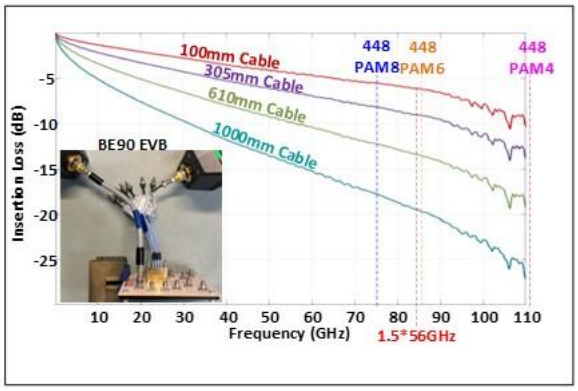

Figure1. BE90 Evaluation Board Frequency Response

Specifically, 224G PAM4 signaling standards call out 1.5 times Nyquist frequency for test fixtures. This is the red line at 84GHz in Figure 1. 224G device transmitter characterization would need this much test and measurement bandwidth for accurate statistical noise measurements. In test environments, however, opportunity exists to characterize receive signal metrics after long lossy channel with less stringent fixture bandwidth requirements [2].

Considerations in the board design included analysis of the waveguide and signal transmission region of the board, as well as the ground ring shape when using thru vias. The board includes a 35mm skip layer for HDI routing, stacked micro via coaxial breakout regions, and the compression coaxial interface for the BE90 test assembly. The BE90 test assembly is then equipped with up to two rows of variable length RF047 coax with a 1.0mm coaxial connector.

4. 448 GBPS PATHFINDING

When analyzing the performance of the evaluation board, the team extended insertion loss measurements out to 110GHz in order to consider performance in the context of future 448 Gbps signals (see Figure 1). This measured analysis of the evaluation board has implications for 448 Gbps pathfinding exercises, particularly in terms of PAM6/8 modulation investigations and assessments.

If 448 Gbps systems use PAM4 signaling (as in 224Gbps), data in Figure 1 implies that would require more than 112 GHz of interconnect bandwidth. However, increasing the pulse amplitude modulation preserves the data rate by growing the symbol time length (slowing down) and adding more logic levels, thus avoiding the need for 112 GHz interconnects.

Figure 1 includes dotted lines where the likely modulation schemes for 448 Gbps PAM8 (blue), PAM6 (orange) and PAM4 (pink) would occur. This type of data collection and extrapolation are important because standards groups are considering 86.6GHz PAM6 versus 112GHz PAM4 concepts for next generation 448Gbps signaling. This data shows that there's also a candidate solution at 74 GHz, PAM8.

Very few test fixtures have the roll-off-free bandwidth to 110GHz shown in Figure 1 that is required to investigate this problem. This issue is explored in detail in [2]. To summarize, previous generations of standardization have set a bandwidth minimum target as ¾ of the baud rate by specifying a 4th order Butterworth filter with a cutoff (fr) set to this frequency to represent the receiver bandwidth needed.

For 112 Gbps PAM4 signaling, the baud rate is 56 GBd, so the bandwidth requirement target is 42 GHz. Following this historical trend, the bandwidth for 224 Gbps PAM4 would be set to 84 GHz which bypasses 67 GHz max frequency VNAs and the 1.85 mm V-band connectors (limited to 72 GHz) and requires a 110 GHz VNA and 1.0 mm W-band connectors. The work in [2] concludes that it depends on the design case if 110GHz will be required for 224 Gbps testing. For 448 Gbps, the test fixture bandwidth will surely be larger than signalling Nyquist frequency.

While the BE90 test fixture tested in Figure 1 cannot provide data beyond 110 GHz due to the limitations of the 1-mm connection system (which most of the industry, instrumentation, and labs use), it is possible to extrapolate performance required for 448G signal analysis due the resonant-free log linear response out to 110GHz.

5. INTEGRATED EM TO SYSTEM CHANNEL DESIGN FLOW

Our IP approach manages the entire “BW stack” from the electromagnetic domain, to the circuit domain (assemblies), to the system domain (channels). Our team works with test and measurement and materials science partners [3] as well as participates in interoperability forums and high-speed serial channel standard development such as IEEE 802.3 and OIF-CEI to ensure we attain the necessary performance metrics.

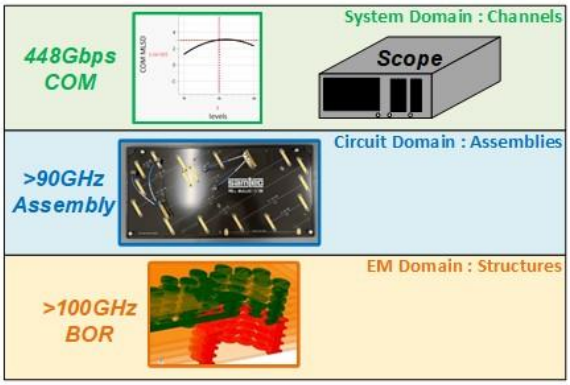

Figure2. Layered IP BW Stack Management

In the electromagnetic domain, a DC-100GHz resonance free breakout region (BOR) design connects to buried striplines at PCB scale dimensions (Figure 2, bottom) [4].

When moving into the circuit domain, we recognized that a significant amount of bandwidth margin will be required to support 448 Gbps designs. For example, five cascaded 90GHz parts will provide much less than 90GHz in a chain, because each one contributes passband loss/ripple. So 448 Gbps assemblies will likely need >100GHz structures and components in order to deliver >90GHz assemblies.

Once the design advances to the system domain, there is an increasing need to assess high bandwidth component performance in terms of its impact on statistical system level SerDes channels. Here is where Channel Operating Margin (COM; Figure 2, top) analysis proves very useful as it has become a statistical channel analysis method well adopted across silicon interface IP and system suppliers.

6. 90GHZ SERDES CHANNEL EMULATORS

Once the evaluation board was developed and the performance analyzed, the team began designing a multi-lane test fixture using the same principles of design (Figure 3). The goal of the test fixture was to provide test and integration engineers with multilane SerDes channel emulation to over 90GHz of linear bandwidth.

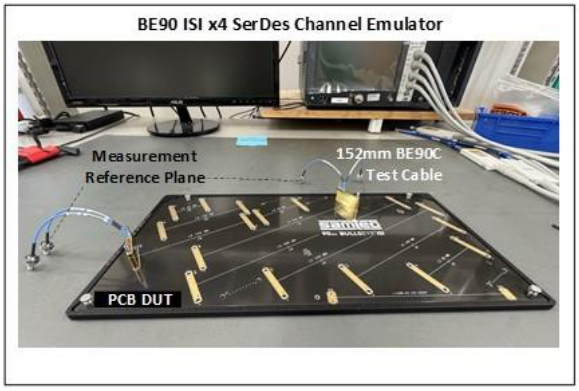

Figure3. BE90 ISI test fixture for 224Gbps PAM4 (56GHz Nyquist) and 448Gbps PAM6 (86.6GHz Nyquist) data rates.

The design theory for the BE90 ISI Test Fixture was to treat the physical design capture as hierarchical from the EM structure domain up through the highly ordered and gridded assembly placement and route. This allowed the team to place and integrate the IP, such as via breakout regions and transitions, rapidly in the PCB, bringing the wide bandwidth through the entire assembly across multiple lanes in parallel.

The platform consists of 11 devices under test (DUTs) of stepped PCB stripline length: a matrix of 9 on the topside and 2 long s-shaped tracks on the backside. Each DUT length contains a x8 single-ended (SE) bus with adjacent wires being driven as true/compliment differential pairs. Thus, each lossy DUT channel length supports simultaneous test verification and characterization of up to x4 SerDes quads.

The nine stepped-length topside DUTs were designed to test 448G PAM6 signals with 86GHz Nyquist frequency. The two long DUT lengths on the back side were assumed too lossy for 448G operation and target 224G LR backplane channel types. The design target is all 11 DUTs pass 224G COM with a stretch goal that the 9 topside DUTs have enough bandwidth for passing COM at 448G PAM6 given reasonable assumptions about die load scaling.

The test fixture is equipped with precision RF coaxial compression interfaces, which enables high amounts of high bandwidth cable to board IO in a small area. The real estate savings in the arrayed coaxial component footprint over SMA-style cable to board terminations then translates into more usable PCB real estate.

The extra PCB real estate enables the extension from single lane DUTs to bus-width DUTs. This makes it possible for parallel, multi-lane SerDes testing. In contrast, multilane test fixtures populated with rigid board-mount single test points would require much more board real estate for the same IO count. Additionally, the compression mate interface of the x4 SerDes cabling is accomplished with two simple thumb screws translating into significant ease of use and lab throughput.

6.1. Configurable Multi-Lane High Speed Assembly Testing

Emerging SerDes device test and characterization requires precision RF metrology-grade capabilities, but they also need multiple lanes (X4, X8, X16) because it is a digital application. The BE 90 ISI Test Fixture accomplishes this by including the configurable cable length and 1.00mm coaxial cable termination inside the lossy channel reference plane.

The tradeoff for unlocking configurability while preserving performance is that extremely low loss channels (<10dB at Nyquist) become unachievable. This is due to the inclusion of the cable loss in series with the shortest PCB DUT lengths. This tradeoff is generally considered acceptable because most SerDes verification is for higher loss channels under more stress. Finding a traditional solution that provides high bandwidth and precision can become prohibitively expensive when thinking about scaling that test solution to the multiple lane counts instantiated in SerDes IP.

In contrast, a configurable SerDes channel emulator allows more agility to keep pace with the rapid channel equalization methods now enabled by DSP-based SerDes. One configuration option is to stagger adjacent channel cable lengths in order to add fine-adjust loss steps on the order 0.25-0.5dB inside the coarser PCB ladder steps.

6.2. Test Fixture Assembly Level Performance

The performance of the BE90 ISI Test Fixture is given below. All measured channels have a -1dB

BW roll off from equation-based performance to 90GHz (Figure 4) with very low insertion loss deviation (ILD) to the 84GHz 224G test fixture specification limit. Additionally, with the assembly level resonances occurring above 100GHz, there is enough real hardware channel bandwidth to address early 448Gbps PAM6 channel analysis and device feasibility testing.

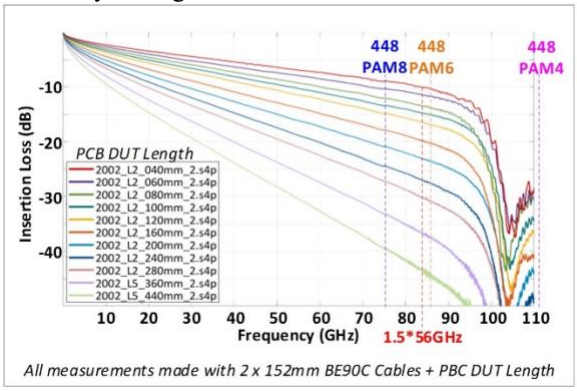

Figure4. BE90 ISI test fixture's measured performance showing linear fixture bandwidth to and through 84 GHz, the specified bandwidth from OIF for 224 Gbps PAM4 testing.

7. ANTICIPATING THE NEEDS OF 448GBPS DEVICE TESTING

The team began designing the platform before standards bodies had begun 400G pathfinding projects. This meant that there was limited frequency domain channel guidance for establishing design targets. We evaluated the design in the pulse domain, designing the test channels to provide similar 5.8ps pulse responses for 448G PAM6 data signals to existing 224 Gbps channels (8.8ps pulse responses).

Once standards bodies began formal 400G pathfinding efforts and some industry consensus was established around initial 448G COM assumptions, we extended our analysis from the pulse domain to the complete statistical channel. 448G PAM6 statistical channel COM results confirmed the design decisions managed from the EM structure domain up through the complete assembly hit their targets.

In Figure 5, the 5.8ps pulse responses of the 11 stepped DUT lengths is given along with the corresponding COM score. As expected, the two longest DUTs intended for 224G LR testing are too lossy to pass the 3dB COM threshold at 448G data rates. The shorter 9 DUT matrix on the topside of the assembly provides a test environment capable of 448G PAM6 SerDes device characterization.

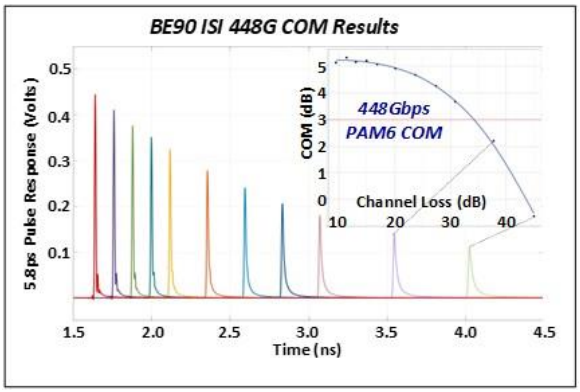

Figure5. BE90 ISI Test Fixture COM Analysis

8. CONCLUSIONS

The result of the design of the evaluation board and the associated multilane test fixture is that engineers have viable building blocks to test and simulate a complicated assembly. The tools represent some of the best empirical measurements available, and they provide enough bandwidth precision to perform next-generation device characterization.

The next step is to further refine SerDes noise models as industry identifies and converges on agreed upon 448 COM parameters in standards bodies.

ACKNOWLEDGMENT

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