

# **Evolving Small Form Factor Architecture for The SOSA™ Technical Standard**

**SWaP considerations drive the evolution of the Small Form  
Factor in rugged embedded systems.**

*The Open Group FACE™ and SOSA™ US Air Force  
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### **Executive Summary**

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Going faster with open standards may mean higher data rates, shorter design cycle times, or smaller architectures that reduce size, weight, and power. VNX is a small form factor (SFF) standard that is based on VITA 74, an inherently rugged module standard with a compelling size, weight, and power (SWaP) proposition, making it perfect for many military and aerospace applications.

The VNX form factor has been selected by a consortium of manufacturers, integrators, defense, and academics professionals as a SFF standard to be included in the new Sensor Open Systems Architecture (SOSA) Technical Standard. VITA 90 is an evolution of VITA 74 and will add functionality to the base standard.

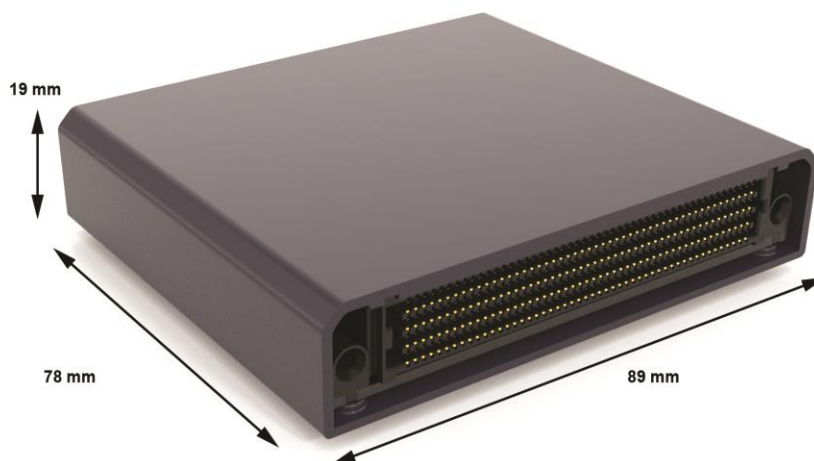
In this document we review this latest SFF architecture and what is included in VITA 90. We discuss options for applying this SFF standard as well as implementation concerns, such as thermal considerations and rugged space applications.

### **The Latest Rugged Small Form Factor Module Standard**

#### **VNX to VNX+**

VNX has been included in the new SOSA Technical Standard, Version 1.0, Sections 13.4 “SOSA Plug-In Cards (PICs) Using VNX” published in the fall of 2021.

A baseline VITA 74 and VITA 90 module in its simplest form is shown in Figure 1 and is approximately the size of a deck of ordinary playing cards. Both standards have an electronic architecture similar to VITA 65, also known as OpenVPX. The VNX+ standard adds coaxial RF and optical connectivity, bringing the essential tenants of VITA 65 (OpenVPX) to SFF applications.



*Figure 1: Typical VITA 74.0 / VITA 90.0 19mm Baseline Configuration Module*

*(Image Courtesy of Samtec)*

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### **Designing for the Future Now**

SOSA Version 1.0, Section 1.6 is working to extend the SOSA architecture to form factors used in unmanned aerial vehicles (UAVs), drones (both ground and air), unmanned underwater vehicles (UUVs), and small spacecraft and satellites (e.g., cube satellites, rovers, etc.).

For this reason, VNX is designed to bring standards-based commercial-off-the-shelf (COTS) technology to the space electronics community. VITA 90.5, also known as SpaceVNX+ (“Space VNX Plus”), is a member of the VITA 90 VNX+ family of standards and a direct descendant of the draft standard, VITA 74.4 (SpaceVNX).

VNX+ boasts improved signal integrity and provides backplane copper connectivity for high-speed fabrics such as PCIe 4.0 at more than 16 GT/s, as well as optical MT, coaxial RF, and video signaling. SpaceVNX+ will be a standard describing an inherently rugged module that has a compelling space, weight, power, and cost (SWaP-C) proposition, and it is well suited for both military and commercial SmallSat, CubeSat, and other extreme environment avionic applications.

For the last two years, there has been significant collaborative effort to complete the transformation of VITA 74 into the VITA 90 family of standards to meet the technical attributes of SOSA and VITA for space, avionic, and weapons system applications.

### **History of VNX+**

The technology behind VITA 74 was initially developed by engineers at Themis Computer. Building on the successful performance of the VITA 57.1 FMC standard, engineers at Themis chose to use the Samtec high-speed, high-density SEARAY™ connector as the primary module-to-backplane interface, as well as the interface between the backplane and the front panel I/O transition board (IOTB). The right-angle female SEARAY connector was selected for the module, and the corresponding straight male SEARAY connector was selected for the backplane. This original NanoATR design defined two module sizes: a 19mm module using the 400-pin VNX connector, and a 12.5mm module using the 200-pin VNX connector configuration.

The NanoATR concept was brought to the VITA Standards Organization (VSO) to be considered for a standard that describes SFF computer and payload modules used in embedded systems designed for UAV and other rugged aerospace applications. From the beginning, the proponents always had space applications in mind, and it was no accident that the modules fit perfectly in a 1U CubeSat, and even more importantly, along the long axis of a 3U satellite. VITA 74 was published as the joint ANSI/VITA 74.0-2017 standard. The standard was given a moniker, VNX™, a name befitting the unofficial “*Nano*” derivative of VPX. In 2021, industry and defense requirements drove the development of the VNX+ standard which increased speeds and added optical and coaxial options. Similarly the high reliability variant, SpaceVNX, became SpaceVNX+.

From its inception, VNX was never intended to replace VPX. Instead, it is designed to bring the essential tenants of the VPX architecture into compute-intensive, rugged, airborne, space, and ground platforms that were physically too small to accommodate a VPX system. Early systems contained one or more single board computers (SBC) which generally employed Intel® Architecture (IA) or PowerPC® Architecture (PPC) processors, often using mezzanine system on module (SoM) processors, as well as storage, communications, and I/O built to other Modular Open Systems Architecture (MOSA) standards as directed by government

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procurement documents. A typical 4-slot VNX+ avionic image and display processor system is shown in Figure 2.



Figure 2: VITA 74 Image Processor With Optical MT Interconnects

(Image Courtesy of Elbit America)

## Options for Applying VNX+ Standard

The VNX+ base-standard is being released with a set of *dot-standards* that are designed to further optimize complex system I/O performance by adding backplane “connector modules.” These modules facilitate high-speed/high-bandwidth optical and coaxial RF/video data transmission for both inter-slot and intra-system digital signaling. They also augment the payload module standards with an accompanying standard that defines VNX-specific power supply modules.

The VITA 90.5, SpaceVNX+ standard is highlighted in this paper for its focus on flight and space considerations. For instance, the SpaceVNX+ standard specifies the electronic and mechanical considerations required to implement rad-hard and rad-tolerant VNX solutions in small spacecraft applications. In addition, the new standard adopts practices and techniques to optimize the module’s pin assignments for optimal signal integrity. It also implements the OpenVPX-style utility segment, control plane, data plane, expansion plane, and overlays that include the optical, coaxial, and specialized high-voltage isolated power contacts, as shown in Figure 3.



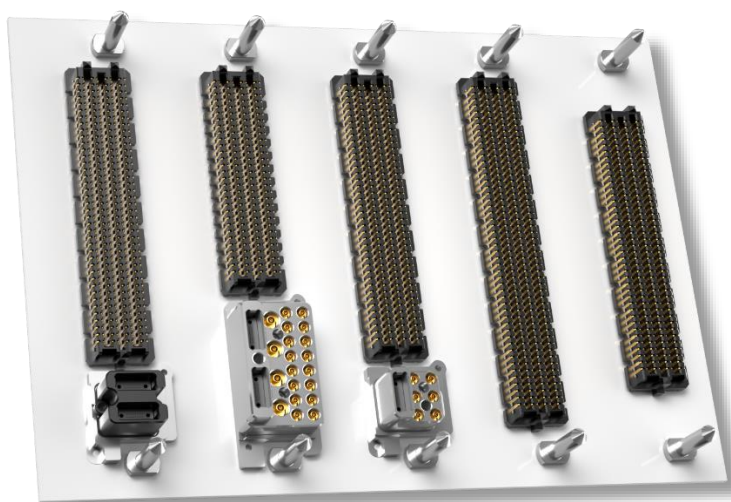
Figure 3: VITA 90 VNX+ Module Basecard With 240-Pin Connector & Full Connector Module

(Image Courtesy of Samtec)

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The VNX+ standard includes new additions to support use-cases such as signal processors, radio transceivers, graphics processors, network and fabric switches, I/O modules requiring coaxial or optical MT signaling, as well as power supply related modules. These applications will use the 240-pin and 320-pin SEARAY high-speed data connector with a full or half-connector module as defined in VITA 90.2.

VITA 90.3 introduces the VNX+ energy conversion unit (ECU) module, also known in VITA 90.5 (SpaceVNX+) as an electrical power supply (EPS) module, using a 320-Pin SEARAY connector centered in a VNX+ slot, and an optional energy storage unit (ESU) using a similarly positioned 240-pin SEARAY connector. Examples of typical VNX+ implementations are shown in Figure 4.



*Figure 4: VITA 90 VNX+ Backplane Example*

With careful engineering of the mechanical and thermal considerations, VNX+ modules can fit in many tight spaces using conventional backplanes or an equivalent cabled backplane.

## **Deployments and Considerations**

### **Modules Available or Coming Soon in the VNX and VNX+ Family of Standards**

Several modules with functionality required for compute, signal processing, communications, and I/O are available or in development. Below is a list of VNX and VNX+ modules that exist today, are currently evolving from existing VNX designs, or are new designs in development:

- Power conversion and energy storage modules for low, medium, and high-power systems
- IA compute modules with up to 11th generation dual-core Intel® Core™ i7 processors (formerly Tiger Lake), and current generation quad-core Intel® Atom™ processors

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- 8-core ArmV8 system-on-module based compute modules
- NVIDIA® GPGPU modules utilizing the NVIDIA Jetson AGX Xavier™ GPU processor
- FPGA modules using various SOCs and MPSoCs with Arm cores, using high-speed copper and optical backplane interfaces
- RF transceiver modules using RFSoc, as well as MPSoC and companion transceiver
- Rad-hard controller modules for space applications
- I/O modules for MIL-STD-1553, ARINC 429, and MIL-1394B/AS5643 data buses
- I/O modules with RS-232/422/485, CAN, and Gigabit Ethernet interfaces
- Gigabit Ethernet switches with L2/L3 and 10GbE uplink ports
- Storage modules using mSATA SSDs.
- MEMS inertial measurement units with GPS

### **Pod-Mounted Sensor Processor**

Considering the extremely limited available space inside a 5” tube (like an AIM-9 Sidewinder-sized pod), previous systems traditionally used expensive custom hardware that was hard to upgrade as threats and requirements changed. Current thinking in SOSA and other similar communities is that they require the ability to upgrade or modernize hardware to keep up with the ever-evolving threats. That requirement drives them to procure and specify standard modules with known hardware and software interfaces. Like SOSA’s MOSA standard OpenVPX, VNX+ is designed to meet those requirements.

Mil/aero integrators have discovered that the VNX+ SWaP attributes make the standard a natural fit for SFF traditionally packaged ATR-style avionics boxes. It is also well suited for pod-mounted sensor and weapon systems that require high-performance sensor interfaces in close proximity to FPGA and MPSoC signal processors, computers, radios, and platform I/O--available as COTS or modified COTS (MCOTS) MOSA modules with standardized electromechanical backplane interfaces.



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VNX+ is the only SFF backplane-centric COTS SOSA standard at this time that can be deployed as vertically oriented conduction-cooled modules on a traditional horizontal backplane, mounted longitudinally (i.e. along the long axis), within the usable area of a 5” diameter tube (as used for an AIM-9X Sidewinder sized sensor pod), or for a 6” diameter tube (as used for the Coyote, as well as other similarly small payload pods or UAV fuselages). See Figure 5.

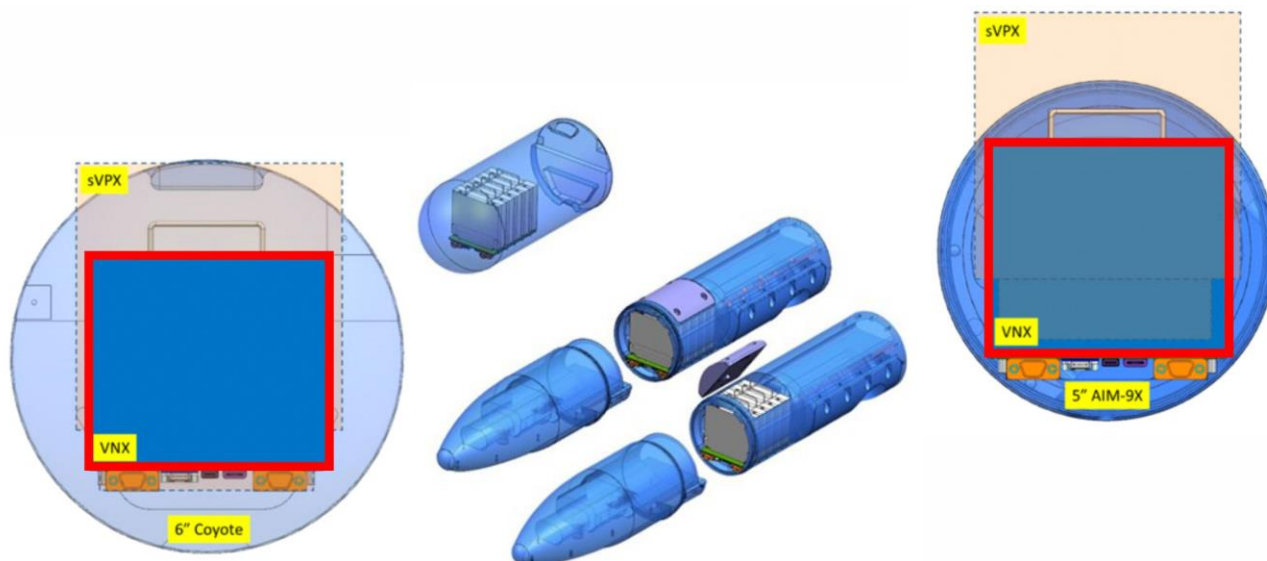


Figure 5: VNX+ Example System in Coyote & AIM-9X Pod

(Image Courtesy of Collins Aerospace)

### CubeSat Sensor Processor

Considering the tight space inside a typical 100mm square enclosure, like a traditional small sat when built in multiples of a 1U CubeSat, current systems often use “stackable hardware” that provides limited reliability and/or performance. The current thinking in SOSA (and other similar communities) drives a requirement to enable inter-module communication between 1 and 10 Gbps with the ability to continue upgrading and modernizing small satellites. This desire drives integrators to specify and procure standard modules with known hardware and software interfaces that provide the desired levels of performance. VNX+ is designed to meet those standards-driven requirements.

## ***Evolving Small Form Factor Architectures for SOSA***

Mil-aero integrators have discovered that the VNX+ SWaP-C attributes make the standard a natural fit for not only small, traditionally packaged, ATR-style avionics boxes, but also SFF space-based communications and surveillance systems requiring high-performance sensor interfaces in close proximity to FPGA and MPSoC signal processors, computers, radios, and platform I/O available as COTS/MCOTS MOSA modules with standardized electromechanical and backplane interfaces. VNX+ is the only SFF backplane-centric COTS SOSA standard at this time that can be deployed as vertically oriented conduction-cooled modules on a traditional horizontal backplane, mounted longitudinally (i.e. along the long axis), within the usable area of a 100mm square within a typical CubeSat. See Figure 6.



*Figure 6: VNX+ Example System Components in 1U CubeSat Designs*

*(Image Courtesy of Ideas-TEK and Trident Infosol)*

## **Space Use Case Considerations**

While VNX was initially targeted at tactical avionic applications, the designers set their sights higher and conceived the standard to service the extreme environment of space. SpaceVNX and SpaceVNX+ have been designed from their inception to fit within typical SmallSat envelopes. This includes 1U to 12U CubeSats, system controllers, and space rovers for critical applications requiring high levels of computing and data transfer performance. SpaceVNX+ follows the high-reliability philosophy of SpaceVPX but considers SWaP-C constraints related to small satellite and space controller missions.

The new SpaceVNX+ open modular standard provides an extensible mechanism to enable more rapid, compliant, and consequently cost-effective small spacecraft delivering these key features and benefits:

- Provide interchangeable hardware and software with standardized hardware/electrical interfaces and control/data plane protocols, reducing wiring and cabling while providing high throughput interfaces
- Enable rapid assembly with qualified plug-and-play components, as well as allowing late-load or last-minute software or hardware changes and hot-swap sensors, external boards, etc.

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- Improve the state of the art of open interfacing platforms, including wireless, suitable for small spacecraft while leveraging COTS components and materials as applicable
- Increase the reliability, durability, and performance of small spacecraft hardware and software by integrating subsystem considerations directly into the design process at the architectural level
- Provide expanded adaptivity for small spacecraft, allowing for platforms to be rapidly varied with respect to altering objectives and variable risk postures
- Deliver substantial advances in dynamically configurable and manageable onboard power generation including improvements in thermal mitigation and dissipation via module clamshells for small spacecraft

Consequently, the SpaceVNX+ in-band protocols, such as Ethernet, SpaceFibre, SpaceWire, PCI Express, Serial RapidIO (SRIO), and in-development high-performance computing modules, will enable future missions such as multiple spacecraft flying in formation to create unprecedented telescope and interferometers for imaging fainter, smaller, and more distant objects. Swarms of SpaceVNX+ assets will enable complex and time-varying networks of spacecraft and sensors that are capable of sharing rich, near-real-time streams of information to enhance space situational awareness and autonomous operations.

Using an available rad-hard EPS, a rad-hard system controller/monitor module (Piovesan et.al <sup>1</sup>, Piovesan et.al <sup>2</sup>), and various COTS, MCOTS, or rad-tolerant sensor, processor, and I/O modules, low SWAP-C, rad-tolerant systems are being developed by several organizations.

## **Implementing This New Form Factor**

### **High Performance in Extreme Environments, on a Budget**

The VNX+ makes it possible to implement a reliable high-performance architecture for small satellites and spacecraft, using highly capable COTS parts in conjunction with lower cost radiation hardened/tolerant supervision circuits/ICs, as well as built-in redundancy, to protect the system from radiation effects like single-event latch-up (SEL) and total ionizing dose (TID).

The utility plane is used mostly for power distribution and system supervision. Signals include the power rails, system management, control signals, clock distribution, and a new construct: unique external I/O (UEIO). UEIO employs a collection of I2C, SPI, and GPIO signals to make structured external I/O easier, and it is making its debut in VNX+ systems. The control plane provides a path for system-level control traffic, generally SERDES GbE for terrestrial applications, but SpaceVNX provides the opportunity to replace the Ethernet with SpaceWire if needed. The data plane provides a high-bandwidth pipe to transfer data between system modules (e.g. 10Gb Ethernet), but it can be similarly replaced by SpaceFibre.

The expansion plane provides another path for high-bandwidth data between paired entities such as graphics processors, co-processors, and sensor interfaces. Generally, protocols such as PCIe, Aurora, GP-LVDS, and SFPDP are used in terrestrial applications, but SpaceVNX+ will also allow SpaceFibre and Serial RapidIO (SRIO). An overlay segment is defined to allow for functionality (as would be allowed using an XMC segment on a VPX module), where I/O comes off a secondary mezzanine in an orderly manner to pre-defined backplane locations for differential pairs and single-ended signals. This overlay also provides the opportunity to support CAN bus, SpaceWire, and single-ended GPIO signals to enhance the options for system monitoring in space applications. See Figure 7.

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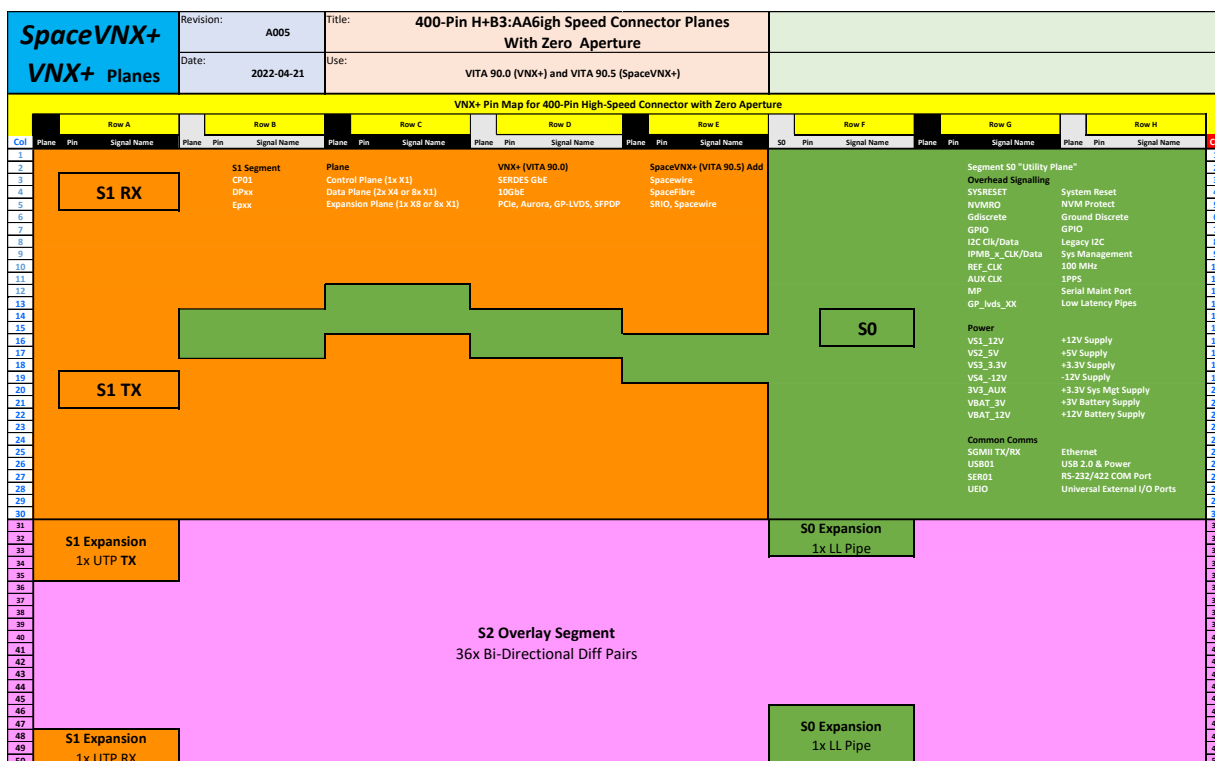


Figure 7: High-level Plane Diagram for VNX+ and SpaceVNX+

### SpaceVNX+ Implementation Approach

An approach to address space reliability (especially radiation tolerance) within the VNX/VNX+ framework consists of combining rad-hard (or tolerant) semiconductors and redundancy, as well as circumvention and recovery approaches (Piovesan et.al <sup>1</sup>, Piovesan et.al <sup>2</sup>). Cost-effectiveness is a critical design parameter; therefore, complex rad-hard components tend to be less attractive alternatives to implementing high-performance solutions for this market. However, radiation tolerance is important to provide guarantees of mission success. An attractive approach to address this trade-off is to implement an architecture that uses rad-hard/tolerant components in the simpler but more critical subsystems of the spacecraft (e.g. housekeeping), while leveraging redundancy and circumvention and recovery (when desired) in the most complex subsystems of the spacecraft (e.g., mission processing). This approach is represented in Figure 8. Note that criticality is understood as tolerance to down-time, where more critical systems are allowed minimal down-time (if any) and less critical system can have sporadic periods of down-time.

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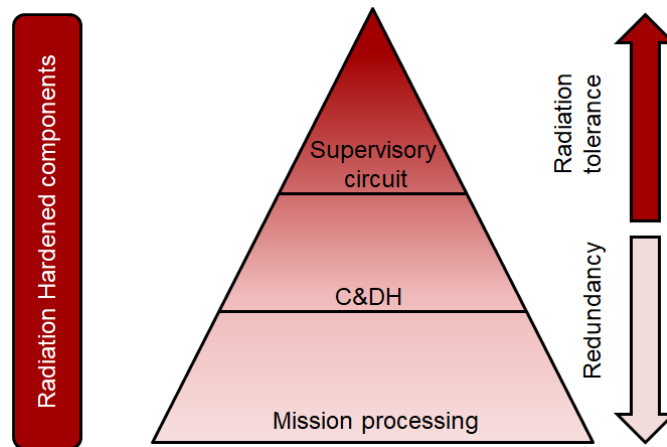


Figure 8: High-level architecture for a cost-effective high-reliability system using VNX+ (Piovesan et.al<sup>2</sup>)  
(Image courtesy of IDEAS-TEK).

An example approach for implementing a high-reliability mission computer with extended I/O functionalities combines a rad-hard system controller with commercial single board computers and I/O modules. See Figure 9. These modules are interconnected using a redundant high-speed serial system (e.g., PCIe) that provides fault-tolerant capabilities in the case of module failures. SEL protection is achieved by including overcurrent protection in the modules that is supervised by the rad-hard system controller (Piovesan et.al<sup>2</sup>).

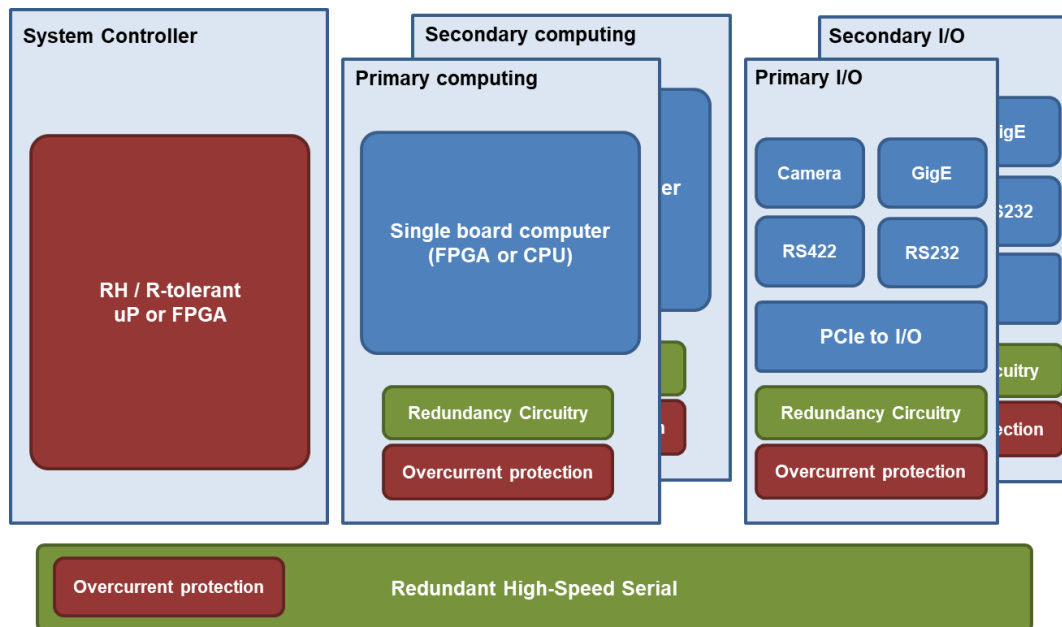


Figure 9: Hardware used to validate the approach described in this section (Piovesan et.al<sup>2</sup>)  
(Image courtesy of IDEAS-TEK).

## Evolving Small Form Factor Architectures for SOSA

The approach described in this section has been implemented and validated under radiation with hardware already in production. The system used for validation consisted of a rad-hard system controller module (based on a rad-hard MCU), and multiple FPGA modules, which consist of rad-hard latch-up protection, a commercial FPGA card, and Gigabit Ethernet Interfaces (See Figure 9). This system was tested for radiation tolerance and radiation mitigation, demonstrating the capability to extend the system life by using fault-tolerance methods. See Figure 10.

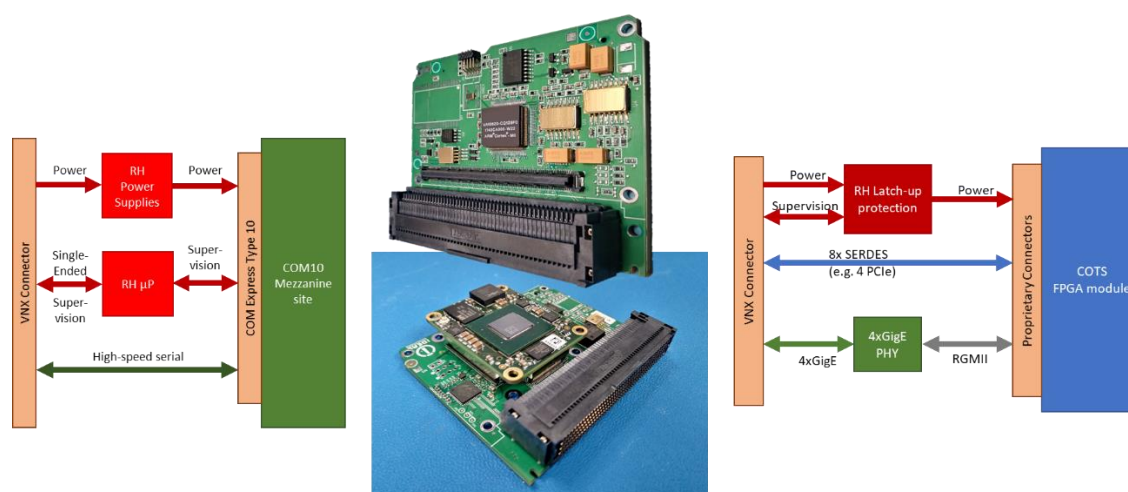


Figure 10: Hardware used to validate the approach described in this section (Piovesan et.al.<sup>2</sup>)  
(Image courtesy of IDEAS-TEK).

## Achieving VNX+ Thermal Performance Targets in Flight

When VITA 74 was first released, the designers of the VNX standard assumed that the practical power limit for the 19mm module should be arbitrarily pegged at a conservative 20W. As time went on and integrators started building actual systems in ever-smaller platforms, performance demands inevitably increased, and the use of one or more 20 to 25W processor modules became commonplace. These systems employed heat sinks consisting of nominally sized heat radiating fins coupled with minimal airflow. Testing proved that well-designed VNX systems could be qualified to meet typical mil-aero environmental requirements.

But how small is small enough? Demands to fit in ever-tighter spaces, as well as requirements to operate in the vacuum of space have forced engineers to look at new cooling methodologies, and those searches pointed to a non-traditional solution, the oscillating heat pipe (OHP). The OHP provides a high heat transport capability and enables effective heat transport in modules such as used in SpaceVNX+ applications. A flat-plate heat pipe (FHP), which is an OHP with check valves designed for microgravity conditions, has been tested and evaluated on-orbit since 2012 as one of the Small Demonstration Satellite-4 (SDS-4) missions. The FHP operated successfully for more than four years on-orbit; its performance matched the results seen in ground applications (Makiko Ando et. al.<sup>3</sup>).

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To understand the thermal limits of individual modules constructed using differing cooling strategies, studies are being conducted to define the upper power dissipation boundaries of practical VNX+ signal processing modules. Figure 11 shows initial thermal modeling that employs three different thermal conduction strategies (intentionally exceeding the expected module capabilities) in an effort to bracket the design limits of the three different materials. Three power dissipation levels, 35W (“Low Power”), 55W (“Medium Power”), and 95W (“High Power”) are modeled, with initial results showing that the “all-aluminum” module shells with a simple thermal interface will result in unmanageable temperature rises at all specified power limits.

VITA 90 VNX+ Module Shell Material Thermal Study			Aluminum			Copper			Oscillating Heat Pipe		
Power	Component	Watts	Rise °C	Ambient °C		Rise °C	Ambient °C		Rise °C	Ambient °C	
				+55 C	+71 C		+55 C	+71 C		+55 C	+71 C
High 95W	FPGA	80	145	200	216	68	123	139	49	104	120
	Optical CODEC	7	132	187	203	71	126	142	39	94	110
	NVM	5.2	125	180	196	60	115	131	39	94	110
Med 55W	FPGA	40	86	141	157	49	104	120	38	93	109
	Optical CODEC	8	88	143	159	52	107	123	39	94	110
	NVM	5.2	78	133	149	40	95	111	28	83	99
Low 35W	FPGA	20	63	118	134	40	95	111	32	87	103
	Optical CODEC	10	66	121	137	43	98	114	35	90	106
	NVM	5.2	55	110	126	30	85	101	22	77	93
Legacy VNX (est.) 25W	CPU 4C Atom	15	54	109	125	38	93	109	30	85	101
	Support Logic	5	40	95	111	35	90	106	32	87	103
	NVM	5	40	95	111	27	82	98	21	76	92

Figure 11: Modeled Data Bracketing Thermal Performance of VNX Modules with Material Variances  
Note – All values are °C rise above heat sink temperature

The moderately advanced thermal mitigation techniques, using copper as the thermal conductor, limit the temperature rise to manageable levels for modules dissipating up to 50 to 60 Watts. The highly advanced thermal mitigation techniques show significant improvements in thermal transport, demonstrating a near 20°C improvement in temperature rise for modules dissipating up to 95 Watts. Note that the example analysis uses two precision heat sinks that are assumed to be in very good contact with two of the three available module cooling faces (i.e., using the two module side faces, but not the handle face). Initial modeling results can be seen in Figure 12.

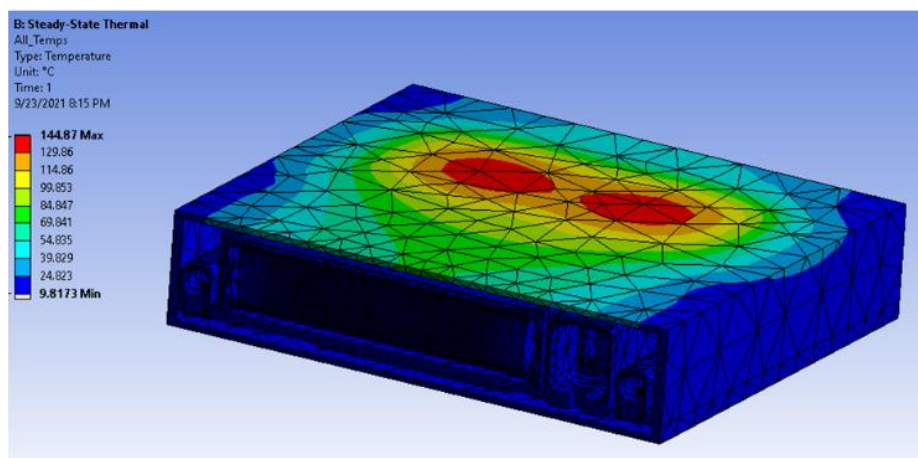
In practice, optimal results would be achieved by using all three cooling faces and minimizing the thermal resistance between the VNX module’s cooling faces and the corresponding heat sinks. The type and quality of the selected heat sink will vary depending on the space available and system thermal performance requirements. A practical system could be cooled using a highly efficient heat exchanger or cold plate, in contact with an optimized thermal transfer material, which is in contact with all three VNX module cooling faces. The thermal transfer material selected can range from a layer of compressible thermal interface material (TIM) to a thin layer of highly efficient thermal grease.

Considering the mechanical envelope studies discussed earlier, coupled with a little algebraic extrapolation, it appears that a system will require a reasonable number of high-power SFF modules. Each of these modules may dissipate 60 to 80W or more, which must be constrained in a very small package (such as a CubeSat or SmallSat). These applications may now be built using a standards-based architecture employing practical



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advanced cooling technologies, such as OHPs, to carry the heat away from the module to the dissipating thermal interface.



*Figure 12: Modeled Data Bracketing Thermal Performance of VNX Modules*

This technology has been proven to transport heat with a small temperature gradient, and if properly positioned, to essentially create an isothermal interface to designated heat transfer locations. Use of OHP technology should allow multiple modules to each spread their thermal load evenly across their primary thermal interfaces. These high-power use-cases are being verified through continued modeling and laboratory testing. Test results and use-case examples showing the expanded limits of the VNX+ power dissipation envelope will be published.

## **Conclusion**

As mil-aero communities move to smaller, more intelligent platforms, the requirement to build smaller systems becomes ever more important. To get the optimized SFF architecture, there is a shift away from custom electronics towards COTS and MCOTS solutions. To minimize the effort required to upgrade systems through the use of common hardware, communications, and control interfaces, it is necessary to build hardware that can be conformant with MOSA standards from ANSI/VITA, SOSA, HOST, and other consortiums. VNX+ is being designed and implemented with all of these requirements in mind.



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5. Technical Standard for SOSA™ Reference Architecture, Edition 1.0 (C212), published by The Open Group, September 2021; refer to: [www.opengroup.org/library/c212](http://www.opengroup.org/library/c212)

## ***Evolving Small Form Factor Architectures for SOSA***

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Andy is an Associate Director in the Collins Aerospace Mission Systems Advanced Technology Center. His previous work ranges from devices for advanced RADAR systems to GaN and SiC devices for electric vehicles and RF PAs for CREW systems. His current pursuits include Multi-Function RF systems to provide stand-in capabilities in attritable platforms by leveraging the scalability of open standards across disparately resourced platforms.

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Mehmet Adalier is the Founder of Antara Teknik LLC. He leads the innovation and development of interoperable, efficient, and secure communications and assured cross-domain solutions on Earth and in Space. He is currently driving delay/disruption tolerant solutions for cislunar and deep space communications utilizing SpaceVNX+.

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Dr. Piovesan is the Director of Engineering and co-founder at IDEAS-TEK. He is currently leading the efforts to develop and deploy radiation-tolerant computing and communication systems in small spacecraft. His technical background includes electronic systems, communication systems, cyber-physical systems, and robotic swarming.

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Dr. Vera is the CEO and co-founder of IDEAS-TEK. He specializes in high reliability and high-performance systems for space applications. Dr. Vera has participated and led a myriad of programs ranging from the development of an integrated circuit (e.g., Radiation Hardened by Design, next generation RISC) to complete computing systems for space payloads and satellites.

Pawan Seth, Director  
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Pawan is the director and cofounder of Trident Infosol, a company specializing in standards based, small form factor embedded electronics for the avionic, vetronic, navtronic, and space environments. Pawan holds a Masters in Electrical Engineering from the University of Delhi.

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For more than 20 years, he has defined, designed, developed, and tested high-performance copper, RF and optical interconnect for a number of embedded computing applications. Additionally, he and his wife champion STEM education, advanced manufacturing techniques and community outreach via their non-profit maker space. John holds a bachelor's degree in mechanical engineering from the University of Louisville.

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### **About The Open Group FACE™ Consortium**

The Open Group Future Airborne Capability Environment™ Consortium (the FACE™ Consortium), was formed as a government and industry partnership to define an open avionics environment for all military airborne platform types. Today, it is an aviation-focused professional group made up of industry suppliers, customers, academia, and users. The FACE Consortium provides a vendor-neutral forum for industry and government to work together to develop and consolidate the open standards, best practices, guidance documents, and business strategy necessary for acquisition of affordable software systems that promote innovation and rapid integration of portable capabilities across global defense programs.

Further information on the FACE Consortium is available at [www.opengroup.org/face](http://www.opengroup.org/face).

### **About The Open Group SOSA™ Consortium**

The Open Group SOSA™ Consortium enables government and industry to collaboratively develop open standards and best practices to enable, enhance, and accelerate the deployment of affordable, capable, interoperable sensor systems. The SOSA Consortium is creating open system reference architectures applicable to military and commercial sensor systems and a business model that balances stakeholder interests. The architectures employ modular design and use widely supported, consensus-based, nonproprietary standards for key interfaces.

Further information on the SOSA Consortium is available at [www.opengroup.org/sosa](http://www.opengroup.org/sosa).

### **About The Open Group**

The Open Group is a global consortium that enables the achievement of business objectives through technology standards. With more than 870 member organizations, we have a diverse membership that spans all sectors of the technology community – customers, systems and solutions suppliers, tool vendors, integrators and consultants, as well as academics and researchers.

The mission of The Open Group is to drive the creation of Boundaryless Information Flow™ achieved by:

- Working with customers to capture, understand, and address current and emerging requirements, establish policies, and share best practices
- Working with suppliers, consortia, and standards bodies to develop consensus and facilitate interoperability, to evolve and integrate specifications and open source technologies
- Offering a comprehensive set of services to enhance the operational efficiency of consortia
- Developing and operating the industry's premier certification service and encouraging procurement of certified products

Further information on The Open Group is available at [www.opengroup.org](http://www.opengroup.org).