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A Signal Integrity Case Study for PICMG COM-HPC Mini Modules

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***Abstract*— Embedded computing developers face new design challenges implementing high-speed protocols like 100 GbE, USB4, PCIe 5.0, DDR4/5, and more. This paper introduces fundamental signal integrity (SI) concepts like insertion loss, return loss, and crosstalk, and relates them to a case study of the connector design for the COM-HPC Module Base Specification Revision 1.2 featuring the new COM-HPC Mini form factor.**

Keywords— COM-HPC Mini, Insertion Loss, PICMG, Embedded Computing, COM-HPC 1.2

I. INTRODUCTION

Embedded computing developers face new design challenges implementing high-speed protocols like 100 GbE, USB4, PCIe 5.0, DDR4/5, and more. The PICMG® COM-HPC® Mini specification addresses the low-power, small-footprint needs of next-generation embedded applications using these advanced protocols. Designing the connector to support this specification required a deep understanding of signal integrity, power, and materials design.

II. COM-HPC® MODULE SPECIFICATION REVISION 1.2

In October 2023, PICMG ratified the COM-HPC 1.2 specification, which added the COM-HPC Mini form factor for cost-effective, rugged, low-power designs (Fig. 1).

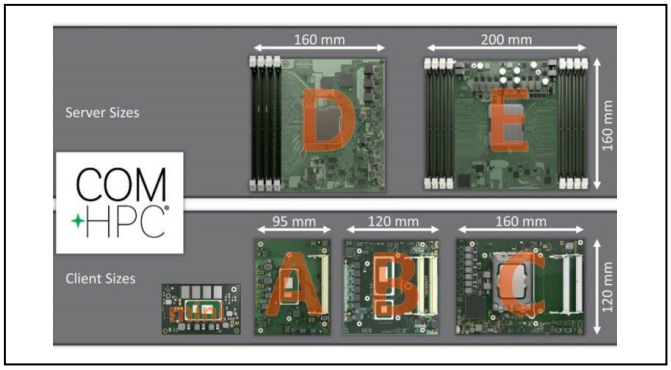

Fig. 1. COM-HPC server and client form factors, including the COM-HPC Mini introduced in COM-HPC Revision 1.2. (Figure courtesy of PICMG.)

Target applications include autonomous mobile robots, drones, portable 5G test and measurement equipment, and industrial automation.

COM-HPC is significant because it enables high-performance, small-form-factor designs that support high bandwidths and a variety of interfaces. An important distinction of COM-HPC Mini modules is that they use only one high-speed 400-pin COM-HPC connector instead of the two used on COM-HPC Client/Server modules. As a result, a COM-HPC Mini connector can still transfer the latest high-bandwidth interfaces, such as fully featured USB 4.0, Thunderbolt, PCIe 4.0/5.0, as well as 10 Gbit/s Ethernet.

A single COM-HPC Mini connector can support [1]:

- 16x PCIe lanes (PCIe 4.0 or PCIe 5.0)
- 2x 10 Gbps NBASE-T Ethernet ports
- 8x SuperSpeed lanes (for USB4/ThunderBolt, USB 3.2, or DDI)
- 8x USB 2.0
- 2x SATA ports (shared with PCIe lanes)
- 1x eDP
- 2x DDI

III. SIGNAL INTEGRITY METRICS

To achieve the connector performance and support the data rates required of COM-HPC Mini specification, it is critical to analyze signal integrity parameters (particularly insertion loss, return loss, and crosstalk) as well as their effects on the resulting loss budget [2]. Below is a brief explanation of these key terms.

A. S-Parameters

S-parameters, also known as scattering parameters, are a unified set of frequency-domain network characteristics. The total number of available S-parameters for characterizing a specific electrical device are determined by its number of ports.

S-parameter models can be used to make performance assessments and/or can be used directly to synthesizes full channel expected behavior. From S-parameters, numerous SI characteristics can be extracted including insertion loss, return loss, and crosstalk (Fig. 2)

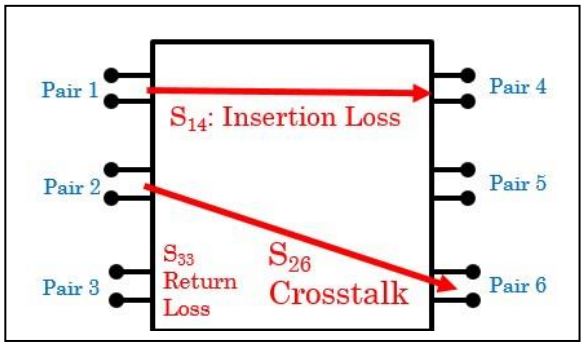

Fig. 2. S-parameter measurements give an indication of an electrical device's performance, in terms of insertion loss, return loss, and crosstalk. This figure identifies three relationships of interest in a six-port device under test.

B. *Insertion Loss*

In the frequency domain, the attenuation or gain of a signal transferred through a passive medium is described by the ratio, converted to dB, of the output voltage to input voltage. For passive devices, the attenuation is denoted as insertion loss (IL) and is often expressed as a negative number for attenuation. In a two-port device under test (DUT), insertion loss is the magnitude of S21 in an s-parameter matrix where the nomenclature "21" refers to the signal observed at port 2 when excited at port 1.

For large components, like cables, printed circuit boards (PCBs), or packages, IL is a significant portion of the overall channel insertion loss and must be evaluated against interface requirements. When combined with the IL of smaller components and vertical transition through the PCB (vias), this holistic system loss is referred to as the "loss budget."

C. *Return Loss*

Return loss (RL) is another frequency domain characterization of a device by its s-parameter matrix as the ratio (expressed in dB) of output voltage to input voltage but at the same port as excited. It is therefore a description of reflected noise at a port due to impedance mismatch within a device against a reference value (Fig. 2).

Although RL is contained in the characterization of insertion loss, it is often helpful to view it separately as the noise originating from DUT impedance mismatch. As the absolute value of DUT impedance mismatch becomes greater than the reference impedance, RL increases in the positive (less negative) direction. Reference impedances are most often 50 Ω, 46.25 Ω, or 42.5 Ω, depending on the application.

D. *Crosstalk*

Crosstalk is unwanted coupled noise that a signal lane experiences from other nearby lanes or sources. This can be further broken down into the aggressor signal direction where far end crosstalk (FEXT) aggressors are traveling in the same direction as the victim signal and near end crosstalk (NEXT) aggressors are opposite traveling aggressors. Every part of the interconnect, from chip to chip, is a potential source of crosstalk. Most applications desire crosstalk levels of -40 dB through Nyquist frequency (Fig. 2).

IV. Case Study: Designing a Connector to Support COM-HPC

Before the COM-HPC specification, small footprint, embedded applications frequently used the popular PICMG COM-Express® specification, which was ratified in 2005. COM-Express continues to serve as a preferred embedded computing family of form factors for many embedded applications. COM-Express connectors were limited to PCIe 3.0 (8 GT/s) performance. The latest enhancements of the COM-Express 3.1 specification support PCIe 4.0 (16 GT/s) performance. However, a new specification and new connectors were needed to support the latest high-bandwidth protocols. Thus, COM-HPC was developed. This section reviews the development of the connector that supports this specification.

A. *Connector Details*

The new COM-HPC connectors feature an open pin field, meaning designers are free to specify differential pair, single-ended signals, and power signals through the same connector. The benefits of open-pin-field technology appealed to the PICMG COM-HPC Technical Working Group for its system and interface flexibility.

The latest base COM-HPC specification defines three pinout types: COM-HPC Server, COM-HPC Client, and COM-HPC Mini (Fig. 1). COM-HPC Client and Server Modules use two 400-pin high-performance connectors for a total of 800 pins. COM-HPC Mini size uses a single 400-pin connector (Fig. 3).

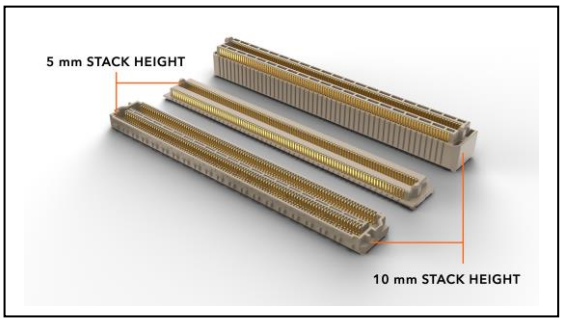

Fig. 3. COM-HPC Mini size uses a single 400-pin connector. The male carrier plugs vary to allow for either a 5mm or 10mm stack height.

The connectors support up to 65 PCIe 5.0 lanes that deliver two x32 PCI Express Links of throughput, as many as eight 25GBASE-R Ethernet channels, 40 Gbps USB4/Thunderbolt data transfer speeds (20 Gbps in each direction using two Tx pairs and two Rx pairs), 80 Gbit/s (DP80) DisplayPort signals, and more.

The female module receptables are employed at a standard height. The male carrier plugs vary to allow for either a 5 mm or 10 mm stack height. The 5mm stack height enables slim module and carrier design. The 10mm stack height enables maximum component density with IC placement on the bottom of the COM-HPC modules and the top of COM-HPC carriers.

During the development of the COM-HPC connector, several PICMG member companies requested improved crosstalk and more ground vias but with the same GSSG density. Our analysis found that increasing the row-to-row spacing in the middle row by 0.2mm helped mitigate crosstalk and allowed for the additional ground vias (Fig. 4). A secondary advantage of this approach is that it eases routing vertically or horizontally.

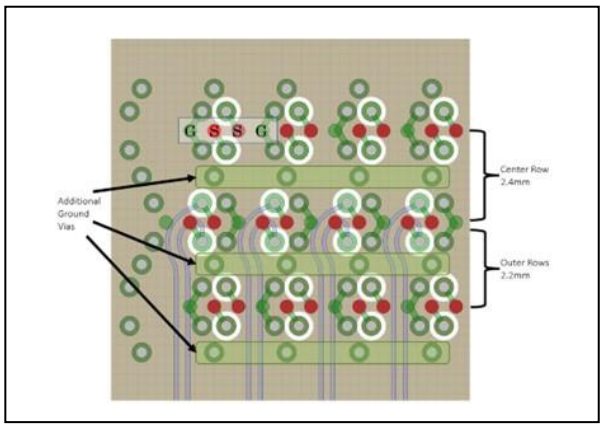

Fig. 4. Increasing the row to row spacing on the COM-HPC Mini connector maintains density while allowing more ground vias, reducing crosstalk, and easing differential routing.

B. *Loss Budget*

The COM HPC Signal Integrity Sub-Group worked in parallel with the main group and addressed the loss budgets for high-speed interfaces. This group created component models in ANSYS® HFSS™, built and simulated channel topologies, and documented the results in loss budget tables.

The first step consisted of building and solving module and carrier PCB models in ANSYS HFSS to create s-parameter models. Some models created included: module and carrier PCB models, COM-HPC 10mm and 5 mm stack height connector models, and differential via and stripline models (Fig. 5)

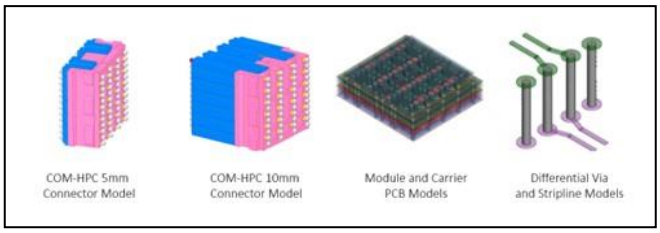

Fig. 5. In order to perform signal integrity analysis, 3D Models were built and solved using ANSYS® HFSS™ to create S-parameters models, then shared between member companies for consistency.

The COM HPC Signal Integrity Sub-Group was then able to build channel models which involved concatenating the component models into an entire channel model that would be common to COM-HPC Server, Client and Mini applications.

Now that the realistic synthesized channels were built, simulations could be run to see how components and the channel would perform based on the COM-HPC channel topologies and protocols. Our study focuses on the performance of the COM-HPC connector with regards to PCIe 5.0 protocol.

The PCI-SIG PCI Express Card Electromechanical Specification Revision 5.1 defines insertion loss of the PCIe 5.0 CEM connector to be roughly 1.5dB at 16 GHz. Initial simulation results of the COM-HPC 1.2 connectors showed that insertion loss was well within that range (Fig. 6).

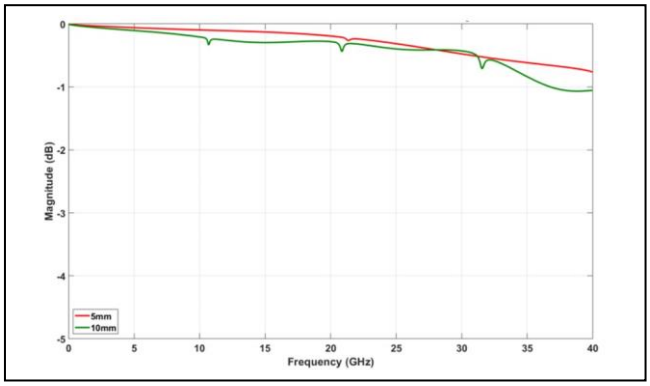

Fig. 6. COM-HPC Mini connector only insertion loss for 5mm (red) and 10mm (green) stack heights.

The PCI-SIG PCI Express Card Electromechanical Specification Revision 5.1 defines return loss of the PCIe 5.0 CEM connector to be roughly 15 dB at 16 GHz. Initial simulation results of the COM-HPC 1.2 connectors showed return loss greater than 15 dB out to 25 GHz (Fig. 7).

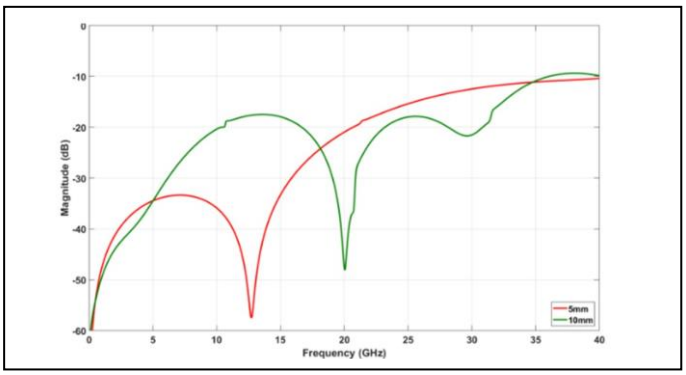

Fig. 7. COM-HPC Mini connector only return loss for 5mm (red) and 10mm (green) stack height

The insertion loss and return loss plots (Fig. 8 and Fig. 9) change when the connector breakout region (BOR) details are included. For reference, BORs typically include PCB traces,

vias, via construction, and ground planes in the vicinity of the connector. Samtec often recommends a specific BOR for a specific mated connector set. BORs can vary by application.

In the case of COM-HPC connectors, the results obtained below are dependent on the Samtec-recommended BOR (Fig. 4).

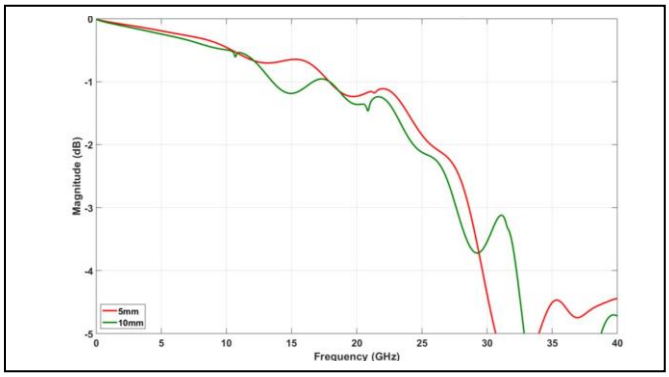

Fig. 8. COM-HPC Mini connector + BOR insertion loss for 5mm (red) and 10mm (green) stack height

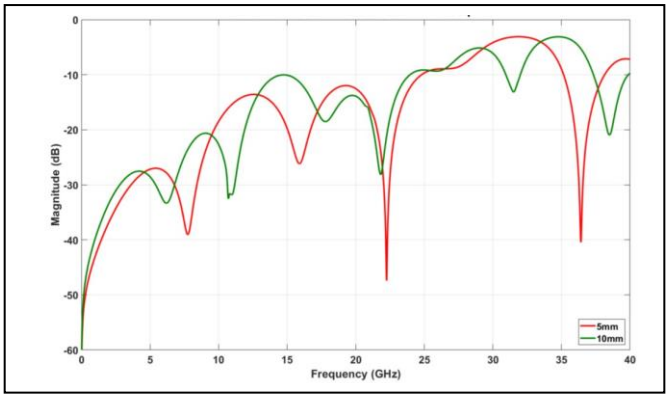

Fig. 9. COM-HPC Mini connector + BOR return loss for 5mm (red) and 10mm (green) stack height

Our analysis of the SI performance of the COM-HPC connectors provides design assurance to the embedded computing developer that COM-HPC connectors will support high-speed protocols like 100 GbE, USB4, PCIe 5.0, DDR4/5, and more.

There may be other connectors along the high-speed signal path. Embedded computing developers should use available s-parameter models to perform component-level and channel-level simulations for their specific designs.

C. Connector Enhancements

The COM-HPC 1.2 specification is particularly well suited for rugged applications. Recently, weld tabs were added to the COM-HPC connectors to improve their ruggedization and reliability. They attach to the COM-HPC modules and carriers using the standard reflow process used for surface-mount parts. The weld tabs increase the maximum pull and shear force across the connector while reducing stress on the connector contacts. The result is improved mechanical strength of the connector for a secure connection to the PCB.

COM-HPC connectors are soon likely to feature a non-solder ball option. Removing extra solder from the connector BGA connections simplifies and improves the manufacturing process; this simple design results in tightly coplanar tails. This tail design increases the solderable area and retention. Other advantages include uniform joints, better spacing and improved SI performance [3].

V. CONCLUSION

This paper offers an introduction to fundamental SI concepts and parameters for the embedded computing developer. The results presented in this paper offer design assurance that COM-HPC connectors are more than capable of supporting high-speed protocols specified on COM-HPC Server, Client and mini form factors now and in the future.

ACKNOWLEDGMENT

The authors want to recognize the work of Burrell Best, Madhu Rengarajan, and Brandon Wong in preparing this analysis.

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