

# Millimeter Wave Design: Optimizing Performance in RF Compression Mount Connectors White Paper



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# Abstract

In millimeter wave designs, compression mount connectors can be used to avoid problems commonly associated with solder variations. However, when using compression mount connectors, the potential impact of pin compression and/or misalignment on electrical performance at high frequencies should be considered. Using modeled and measured data, this white paper investigates how misalignment and pin compression could impact a real-world design. It also explains how to detect and avoid issues in order to optimize performance and complete a successful design.

#### **Authors**

**Michael Griesi** received his B.Sc. and M.Sc. in Electrical Engineering focused on signal integrity from the University of South Carolina and has 20 years of experience across a broad background in electromagnetics spanning design, simulation, validation, and automation in digital high speed, wireless and passive RF applications. Michael is the RF Design & Simulation Engineering Manager at Samtec.

**Zak Speraw** is an RF Design Engineer at Samtec with a focus on signal integrity and extensive industry experience in design, optimization and measurement of high-speed digital and RF interconnects along with high-speed PCB breakouts.

**Edwin Loy** is a Senior Opto-Mechanical Design Engineer at Samtec. He received his B.Sc. in Mechanical Engineering at the University of California, Berkeley and has 25 years of experience in mechanical design, packaging, and process development of optoelectronic components. Edwin has a passion for first principles design methods using simulation and measurement for experimentation and validation.

**Sage Wronowski** received his B.Sc. in Physics from West Chester University of Pennsylvania. Sage is an RF Design Engineer at Samtec with 5 years of experience with RF interconnects. Areas of expertise include modeling, design, testing, and simulation of RF interconnects.

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## Introduction

Compression mount connectors have notable advantages over soldered connections for millimeter wave designs. For instance, they avoid the potential performance degradation of solder reflow, enable high-performance millimeter-wave frequencies, provide flexibility during PCB design, offer high reliability, and can be reused [1].

One of the most common concerns regarding the use of compression mount RF connectors is: what impact does pin compression and/or misalignment have on the system performance? The answer is complicated by the fact that it can be hard—or even impossible—to see if pin compression is occurring or if the connector is misaligned.

#### **The Concern with Pin Compression**

When a compression mount connector is lowered and placed onto a PCB, the connector is then "mounted" by bolting the connector to the PCB through non-plated drill holes. The signal pin contacts the PCB before the connector body grounds to the PCB copper (Figure 1). What is important to understand: as we tighten the mounting hardware, does the pin push into the PCB? And if so, does it impact the PCB layers within a degree of concern that will degrade electrical performance of the connector or PCB launch?



Figure 1: The left image shows the connector mounted on a PCB while the right image shows that the pin makes contact with the PCB before the body, which highlights the concern over potential compression of the pin into the PCB when torqued in place.

We used EM simulation in HFSS to determine the possible sensitivity of pin compression, simulating pin compression through a hypothetical compression depth. The evidence suggests that electrical performance would be sensitive to pin compression. When the pin and pad are flush, the VSWR is optimal with nominal impedance (see Figure 2). In Figure 2, the upper left chart shows impedance in the time



domain, and the lower left chart shows that VSWR simulation results from DC to 90 GHz are 1.2:1 or better throughout the bandwidth at 0 mil compression (blue trace).

Figure 2: In a hypothetical simulation, when the pin and pad are flush, VSWR is optimal with normal impedance (right side of figure shows HFSS simulation, left side shows performance). As the pin pushes the pad into the dielectric, the pad couples with the return plane, impedance changes, and VSWR increases as a result. Note that as the pad is pressed further into the dielectric (1.4 mil), the performance degrades to 1.6:1 VSWR at 90 GHz.

In the second iteration of this simulation, if the signal pad has a small degree of pin compression (0.7 mil below the surface of the PCB and pushed into the dielectric), it couples with the return plane. The impedance changes and VSWR increases (see Figure 2, red trace). At around 50 ps along the signal trace where the signal transitions from connector into PCB, there was more capacitance, so the impedance was lower, which impacts VSWR. Interestingly, the impact to VSWR was minimal from DC to 65 GHz. However, after 65 GHz, VSWR increases to 1.4:1 at 90 GHz, as compared with 1.2:1 at nominal.

In the third and final iteration in this study, the pad was modeled to experience 1.4 mil compression (Figure 2, green trace). At 50 ps, the impedance profile again shows a greater decrease. In this case, VSWR begins to increase with respect to nominal as early as 40 GHz, reaching an increased maximum of 1.6:1 at 90 GHz, as compared with 1.2:1 at nominal.

This study confirms that if pin compression occurs, bandwidth and performance could be impacted. At this point in the study, pin compression was hypothetical. To predict if it could occur and to what degree, further study was needed. So, we embarked on a project to create detailed models to answer the questions: Can we accurately predict mechanical compression and what do we learn? What is the electrical impact of mechanical deformation and what can be done to minimize that impact?



## **Modeling Pin Compression**

To explore the possibility and extent of mechanical pin compression, we imported the connector and PCB model shown in Figure 1 into Ansys Mechanical. After applying typical model preparation steps, such as joining vias with planes, applying material properties, and refining a tetrahedral mesh, we used a Bolt Pretension simulation to relate the torque applied to the mounting bolt to an axial force, effectively "mounting" or tightening the connector in place (Figure 3). It is important to note that recommended torque values are provided with connector prints; in this case, the recommended mounting torque was 0.5 to 0.8 inch-pounds.



*Figure 3: A Bolt Pretension simulation relates the torque to an axial shrinkage.* 

In line with the recommended mounting torque, a nominal 0.6 inch-pounds of torque (≈257 N) was applied to the bolts. This model used material characteristics for Isola's Tachyon 100G in the PCB dielectric layers. Interestingly, the results showed only a small deformation, which correlated well with physical cross section images (Figure 4). However, it was also noted that the internal bead construction inside the connector deformed, and manufacturing tolerance allowed the pin to displace, ultimately minimizing pin compression into the PCB, which was promising news for our hypothetical electrical simulations.







Figure 4: The left image shows some minor deformation at the top of the PCB copper with minimal compression of the pad into the dielectric which correlated well with physical cross section. The right image shows the internal connector bead flexing away from the PCB as highlighted by the red curve.

We considered two more cases to determine the possible impact of either over-torquing during mounting or a relatively softer PCB material. For the over-torqued case, 0.9 inchpounds of torque ( $\approx$ 386 N) was applied. The result was very interesting and showed the PCB warping around the connector without increasing pin compression. More surprisingly, the softer PCB dielectric material also resulted in the PCB warping around the connector without increasing, but this time with only 0.2 inchpounds of torque ( $\approx$ 100 N) applied (Figure 5). This means PCB warpage may be the primary concern rather than pin compression.





Figure 5: The left image shows the PCB warping around the connector which has been observed in similar compression mounted connectors as shown in the right image.

Ultimately, the conclusions of these simulations were:

- 1. Using the recommended 0.5 to 0.8 inch-pounds of torque when mounting the connectors minimized pin compression to some minor deformation at the top of the PCB copper rather than excessive displacement of the entire pad into the dielectric.
- 2. Over-torquing and softer PCB materials led to PCB warpage (rather than excessive pin compression).

3. Visual inspection can provide users with feedback to determine unintended PCB warpage.

The next step was to use these results to simulate the potential impact on electrical performance. We exported the resulting mesh from Ansys Mechanical in an STL format.

# **Preparing Ansys Mechanical results for Ansys HFSS Electrical Simulation**

It was necessary to convert the many facets of the large mechanical model in the STL file into something more suited for an EM simulation while still maintaining the mechanical deformations. This was accomplished by importing the STL into Ansys Discovery and using several facet tools, such as auto-skin and fit spline, to replace the many facets with smooth surfaces and convert to a solid model (Figure 6).





Figure 6: The left image highlights all the small "facet" segments represented as individual sheet objects, and the right image shows the "cleaned" model without the small segments represented as smooth solid models.

To verify the cleaned solid geometry was a reasonably accurate representation of the original faceted geometry, we used the Deviation tool in Ansys Discovery to quickly compare the geometry with a color-coded overlay. We set a tolerance of 2/10,000 of an inch on the dielectric and 1/10,000 inch on the trace. Figure 7 shows the match by color (green is within tolerance), confirming the resulting clean geometry was in fact an accurate representation of the original model exported from Ansys Mechanical.





Figure 7: A comparison between the original detailed mechanical model and the "cleaned" model for EM simulation showed excellent correlation.

While it is possible to quickly convert an STL into a solid model with a simple right-click of the model objects in the modeler tree, the result is a very large model that can be difficult to impossible to import and solve in an electromagnetic field solver like HFSS. The value and motivation behind this intermediate model preparation step was to ensure the model could be solved in HFSS efficiently. In this case, this step resulted in a 5X reduction in file size (compared with a simple STL to Parasolid conversion), a 5X reduction in HFSS project file size, a 4X reduction in HFSS solve time, and a 2X reduction in HFSS solve memory for the cleaned model as compared to the faceted model.

#### **Impact to Electrical Performance**

Once reliable models were created, the next step was to determine the impact of the mechanically deformed geometry on electrical performance. To collect baseline characteristics, we examined the performance of an ideal PCB model with no torque, no simulated pin compression, and no PCB deformation (Figure 8).





*Figure 8: When the pin and pad are flush and there is no torque, the VSWR is optimal with nominal impedance.* 

Next, we evaluated the model with 0.6 inch-pounds of torque (Figure 9). The image in the top right panel shows the PCB warpage in the layer stack. The upper left of Figure 9 shows the impedance profile in the time domain (red trace) compared to nominal (blue trace).





*Figure 9: We found that 0.6 in-lbs of torque (red trace) lifted the impedance profile slightly (top left) but the impact on VSWR was minimal (bottom left).* 

Note that the impedance surprisingly increases around 50 ps, where we transition from the connector to the board, as compared to the nominal case. However, it is important to keep in mind that the mechanical model includes some flex in the connector bead that leads to additional displacement of the center contact along the length of the connector, which is observed as an increase in the impedance profile around 25 ps as compared with nominal. So, while unexpected, this makes sense when considering contact displacement was ignored in the hypothetical simulations, which further emphasizes the value and insight gained from the mechanical simulations.

The resulting deviation in impedance as compared with nominal might imply an increase in reflections and therefore increase in VSWR. However, since the general trend of the impedance was still quite similar to the nominal case, the impact on VSWR was minimal. Keep in mind that 0.6 inch-pounds of torque is within the recommended mounting torque of 0.5 to 0.8 inch-pounds, concluding that following the recommended range mitigates the chance of degrading electrical performance when mounting.

The third model (Figure 10) with 0.9 inch-pounds of torque was slightly higher than the Samtec stated torque range. The impedance showed some minor deviation compared to the 0.6 inch-pounds of torque model. The resulting VSWR shows similar correlation to the previous two models until we approach 90 GHz. All three cases have a VSWR better than 1.4:1 throughout the entire bandwidth.



Figure 10: The over-torqued 0.9 in-lbs model (green trace) results in a larger impact on VSWR, especially at higher frequencies.



The most surprising risk to electrical performance was a direct result of the unexpected PCB warpage for over-torqued and/or soft PCB materials. Increased PCB warpage could create a cavity between the connector and PCB, with an increase in PCB warpage corresponding to a change in the cavity's geometry. The image on the left of Figure 11 shows E-fields plotted over a sheet which occupies the largest space of the cavity between the connector and the PCB.



Figure 11: Increased PCB warpage creates a cavity, and electromagnetic leakage into a cavity can lead to electrical suckout and degrade performance.

The resulting field plot reveals a cavity that extends outside the signal path, which leads to a new concern: a cavity can potentially lead to a suckout and ultimately reduce the usable bandwidth of the connector.

#### **The Concern with Misalignment**

Throughout this paper so far, we have covered pin compression and PCB warpage, but these are not the only parameters to consider when using compression mount connectors.

The remaining concerns for compression mount connectors have to do with misalignment. There are three degrees of freedom in how a compression mount connector could be misaligned: side to side, back and forth, and rotational (see Figure 12). We conducted research to determine how these types of misalignments influence performance.





Figure 12: Compression mount connectors have three potential types of misalignment: side to side, back and forth, or rotational. Our research aimed to determine the electrical impact from these types of misalignments.

To determine the impact of side-to-side misalignment, we compared 2 mil and 4 mil misalignments to a nominal connector centered perfectly on the PCB pad (see Figure 13). At a 2 mil offset (red trace), there was a very slight change in impedance and VSWR when compared to the optimal positioning (blue trace). When the misalignment moved to 4 mil (green trace), the impedance dropped as coupling between the body and the trace increased. This is notable in the impedance profile, but the VSWR change was negligible. The results indicate a very low sensitivity to electrical degradation caused by side-to-side misalignment.





*Figure 13: Despite moving the connector as far as 4 mil from its optimal (blue trace) position, the impact on VSWR of side-to-side misalignment is quite low.* 

The next step was to examine back and forth misalignment. As in the previous analysis, we began with optimal placement, then moved the connector towards the back of the pad by 4 mil, and then moved the connector towards the front of the pad by 4 mil. Figure 14 shows the performance impacts. Moving towards the back of the pad by 4 mil showed significant impact on the impedance profile (red trace), indicating higher inductance. That was associated with significant reflections in the frequency domain and serious impact on the VSWR across the band of operation, with VSWR increasing with frequency.

If we move the connector forward, we are now moving 4 mil towards the transmission line and away from the pad. We see more coupling between the pin and the reference plane (green trace in the TDR/impedance profile) and the VSWR in bottom left starts to degrade at lower frequencies than previously observed, with significant degradation above 65 GHz. The results indicate high sensitivity to front-to-back misalignment.



*Figure 14: Front-to-back misalignment analysis shows high sensitivity, particularly when the connector is moved towards the transmission line.* 

The third type of misalignment is rotational. We were able to use measurement for this analysis because it is possible to see the microstrip escape from the connector (Figure 15) and determine any misalignment. We began with a nominal case (blue trace) and compared it to a rotational misalignment (red trace) in Figure 16.





*Figure 15: A properly aligned connector to the microstrip trace (left) versus a rotational misalignment (right).* 



Figure 16: Rotational misalignment had significant midband electrical degradation.



The dip in the impedance profile (red trace in Figure 16 top) was associated with some midband degradation in the VSWR (red trace in Figure 16 bottom), somewhere around 20-30 GHz. This demonstrates there is some sensitivity to rotational misalignment.

## **How to Ensure Proper Alignment**

While it is reasonably easy to see rotational misalignment, it is nearly impossible to see back and forth misalignment, which was shown to be the most sensitive parameter per our analysis above. So how can a designer ensure that a connector pin is placed properly on the pad?

For that, Samtec has added alignment features to connectors [2], which appear as notches in the corner of Samtec's vertical compression mount connectors (see Figure 17). These work in conjunction with a fiducial that can be etched into the PCB.



*Figure 17: Alignment features in Samtec's vertical compression mount connectors work with fiducials to ensure alignment to the center pin.* 

Specifically, the copper etch is defined on the PCB footprint, then the connector is aligned to that etch during assembly (Figure 18). The image in the bottom right of Figure 18 shows where the connector was mounted. If you look closely, there is only a single blemish in center of the pad, which means the connector was properly placed the first time. Since proper alignment is critical to electrical performance, having alignment features on the connector can ensure reliable performance.





*Figure 18: Using fiducials (bottom left) combined with PCB etching (top left) enables assemblers to properly place connectors the first time (right).* 

# **Proving Performance**

To test out the alignment analysis and reliability of the alignment features in <u>Samtec</u> <u>1.35mm compression mount connectors</u>, the final step was to measure performance. Results showed a healthy margin between measured performance and targeted specifications (see Figure 19).



Figure 19: The results above used automatic fixture removal (AFR) on the measurement to isolate the connector and PCB launch on the top layer of a 6-layer Tachyon 100G. Black lines (left) show maximum VSWR specifications, demonstrating that the connector performance is well within specification.

# **Final Takeaways**

When using compression mount connectors, it is important to remember these key points:

- Mechanical pin compression can occur, but PCB warpage might occur first
- PCB warpage can lead to electrical suckouts
- For maximum performance, follow the recommended mounting torque and visually inspect for warpage, particularly around the edge of the connector
- For maximum performance and ease of installation, use compression mount RF connectors that are equipped with alignment features

For questions related to your design, please contact <u>RFgroup@samtec.com</u>.

#### Resources

- 1. "What are Solderless Compression Mount Connectors?" Everything RF.
- 2. "<u>How to Reliably Align Compression Connectors for mmWave Applications</u>," Jean-Jacques DeLisle, IXS | Microwave Journal March 2023