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Finding Reflective Insertion Loss Noise and Reflectionless Insertion Loss

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Abstract

As work begins in designing interconnects at 112 Gbps, channel specification metrics need to be revisited to ensure that the different parameters that lead to eye opening degradation are quantified realistically. This paper identifies the pitfalls of the insertion loss deviation which utilizes a fitted attenuation profile and is not able to distinguish between the reflections and coupling to resonant structures. This alternate approach utilizes the power scattering matrix theory in finding the insertion loss noise due to reflections by solving simultaneous equations for the zero reflection termination. This physics based approach is ideal for interconnect characterization pertaining to reflections.

Author (s) biography

Hansel Desmond Dsilva is a Staff Signal Integrity Engineer at Achronix Semiconductor Corporation. His responsibilities include high speed channel design pertaining to modelling methodology and tool development. Prior to this, he was at Intel Corporation in USA working on system modelling of different high speed interfaces including PCI Express®, Intel® Ultra Path Interconnect (UPI), Ethernet, DDR and Intel® Omni-Path Fabric Interconnect. The work on system modelling at Intel lead to a number of department recognition awards for the capital saved through introduction of novel methodologies in enabling customers to validate hardware. He received a Master of Science degree (with thesis) in Electrical Engineering from San Diego State University in 2015 and a Bachelor of Engineering degree in Electronics and Telecommunication Engineering from Don Bosco Institute of Technology, Mumbai University in 2013. He has written a number of papers for a number of IEEE and electronic industry focused conferences. He believes in innovating through collaboration and never shies from listening to others thought process in challenging his own.

Sasikala J is a Senior Package Design Engineer at Achronix Semiconductor Corporation. She has worked in high speed signaling which includes DDR4, GDDR6, PCIe Gen5 and other interfaces, power distribution and worked on high density buildup style packages for 10+ years. She has handled several package development projects that supported complex SoC meant for diverse end applications. She has a B.E. Electronics Engineering from Maharaja Institute, Anna University.

Abhishek Jain is a Senior Signal Integrity Engineer at Achronix Semiconductor Corporation. His responsibilities involve Signal and Power Integrity for Serial and Parallel Interfaces pertaining to Package development. He has a Master of Technology Degree in VLSI and Embedded System specialization from IIT-Delhi and a Bachelor of Engineering degree in Electronics and Telecommunication Engineering from Maharaja Agrasen Institute of Technology, GGSIPU.

Amit Kumar is a Principal Engineer at Achronix Semiconductors Corporation. His responsibilities include signal integrity of package and board and handling customer

board recommendations. He received his Bachelor of technology degree in Electronics and Communication Engineering from Vellore Institute of Technology, Vellore.
Richard Mellitz is presently a Distinguished Engineer at Samtec, supporting interconnect signal integrity and industry standards. Prior to this, he was a Principal Engineer in the Platform Engineering Group at Intel. Richard was a principal member of various Intel processor and I/O bus teams including Itanium®, Pentium®, PCI Express®, SAS®, and Fabric (Ethernet, IB, and proprietary). Additionally, he has been a key contributor for the channel sections IEEE802.3 backplane and cabling standards, and for the time domain ISI and return loss standards for IEEE802.3 Ethernet, known as COM (Channel Operating Margin) and ERL (Effective Return Loss), which are now an integral part of Ethernet standards due to Rich's leadership. He founded and chaired an IPC (Association Connecting Electronics Industries) committee delivering IPC's first PCB loss test method. Prior to this, Rich led industry efforts at IPC to deliver the first TDR (time domain reflectometry) standard which is presently used throughout the PCB industry. Richard holds many patents in interconnect, signal integrity, design, and test. He has delivered numerous signal integrity papers at electronic industry design conferences.

Adam Gregory is a Signal Integrity Engineer at Samtec. He is involved in modeling and analysis of high speed differential signaling channels. He received a BSEE and MSEE at the University of South Carolina.

Beomtaek Lee joined Intel in 1997. He is currently a senior principal engineer in Data Center Group (DCG). He worked on power delivery and EMC design for Pentium®II, Pentium®III and Pentium®4, front side bus (FSB) development for Itanium®2 and Xeon® processors, external memory interface (XMI), Scalable Memory Interconnect (SMI) and Intel® QuickPath Interconnect (QPI) developments for Intel datacenter platforms. He has been working on PCI Express, Intel® Ultra Path Interconnect (UPI), Ethernet, Intel® Omni-Path Fabric Interconnect and Optical interconnect developments for Intel datacenter platforms. He received his Ph.D. in electrical engineering from The University of Texas at Austin in 1996.

Background

Today's industry demands high performance and high density interconnects in targeting high data rates (25 Gbps+). At such high data rates, each component of the channel plays a vital role and can lead to noise in the channel, leading to eye opening degradation. This in turn has created the need to characterize the impact of each channel component to inter-symbol interference (ISI), reflections and crosstalk.

Minimizing the reflections is especially important in channel performance as the signal to noise ratio (SNR) gets impacted with reflections and PAM4 signaling is more sensitive to reflections than NRZ signaling. This work introduces the effective insertion loss noise (RILN) metric to characterize the amount of reflections in a mated test fixture (MTF) for IEEE 802.3cd specification evaluation as an alternative to the insertion loss deviation (ILD) metric.

The channel operating margin (COM) and effective return loss (ERL) are used in IEEE 802.3 channel compliance testing. COM is a figure of merit for a channel derived from measurement of its scattering parameters. COM is related to the ratio of a calculated signal amplitude to a calculated noise amplitude. ERL is characterized as a figure of merit for the electromagnetic wave reflection from a device or a channel input or output. COM and ERL, help to address the compensable and un-compensable ISI by considering Tx and Rx equalizations in the analysis for higher speed SerDes developments.

The component level reflections have wider implications than the channel ISI and hence the need to optimize the impedance profile at a component level in ensuring least amount of impedance discontinuities in a channel. Connector and component designers often use ILD versus frequency or figure of merit of ILD (FOM_{ILD}) in evaluating for reflections.

In the first section, the usage of ILD is stated and its limitation is covered with misbehavior at high frequency beyond 10GHz. In the second section, an overview of ILD and FOM_{ILD} is stated. The third section introduced RILN and FOM_{RILN} with power wave scattering matrix theory, which was used in zeroing out the reflections of the network. Also, the example of a reference package as defined by IEEE 802.3 specification is used to verify the zeroing out of the reflections. In the fourth section, an OSFP and QSFP28 mated test fixture is evaluated for ILD and RILN along with the corresponding figure of merit, which presents the confidence in utilizing the RILN methodology for interconnect optimization. In the fourth section, FOM_{RILN} is used to evaluate the end-to-end channel performance, which presents the RILN methodology valid for components and end-to-end channel evaluation in quantifying the amount of reflections.

This paper will present a methodology for dissecting loss and reflection from a measured S-parameter insertion loss or partitioning the loss and reflections when optimizing interconnects in meeting specification compliance.

Problem statement

Insertion loss deviation (ILD) is used to evaluate the noise in the insertion loss due to reflections. However, ILD becomes too high at high frequency and it becomes irrelevant in evaluating high speed SerDes design such as 56Gbps and 112Gbps signaling. This limits the usage of ILD metric in optimizing the channel component to minimize noise due to reflections.

Fig. 1 shows an example of evaluation of a component for ILD. It can be seen that the fitted insertion loss deviates in the low frequency and high frequency. This paper identifies the pitfalls of ILD which utilizes a fitted attenuation profile and is not able to distinguish between the reflections and coupling to resonant structures. This becomes especially evident at high frequencies.

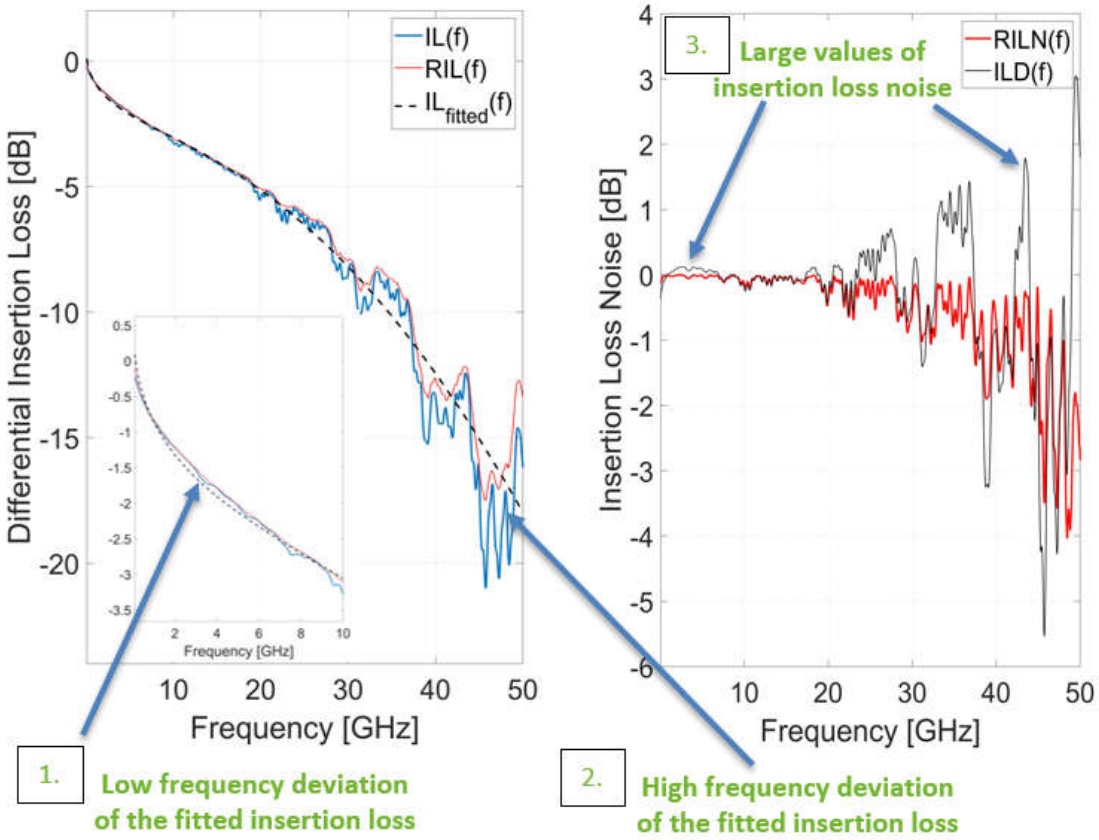

Figure 1. Insertion loss deviation predicting large noise due to reflections in the high frequency.

As an alternative to ILD, RILN is introduced by mathematically computing optimal termination which is frequency dependent and inducing zero reflection at both ends of the channel. With the concept of RILN and zero reflection it becomes possible to dissect loss induced noise and reflection induced noise from measured or simulated S-parameter insertion loss data.

What is figure of merit of ILD?

IEEE 802.3 standard for Ethernet specifies ILD and FOM_{ILD} [1]. ILD is the deviation of the insertion loss across frequency in quantifying the reflections of a channel. FOM_{ILD} is a quality factor of a channel for reflections. FOM_{ILD} helps to understand how close a component represents a transmission line characteristics for a given data rate. FOM_{ILD} depends on the data rate.

ILD utilizes a fitted attenuation profile in calculating the deviation of the insertion loss. It is decibel difference between the measured insertion loss $IL(f)$ and fitted attenuation profile $IL_{fitted}(f)$ which is given by (1).

$$ILD(f) = IL(f) \quad IL_{fitted}(f) \quad (1)$$

The fitted insertion loss as a function of frequency is given by (2).

$$IL_{fitted}(f) = a_0 + a_1\sqrt{f} + a_2 f + a_4 f^2 \quad (2)$$

Where,
a_0, a_1, a_2 and a_4 are the fitted insertion loss coefficients.

The fitted insertion loss coefficients are then given by (3).

$$\begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ a_4 \end{bmatrix} = (F^T F)^{-1} F^T \mathrm{L} \quad (3)$$

Where,

The weighted frequency matrix F is given (4).

$$F = \begin{matrix} 10^{-IL(f_1)/20} & \sqrt{f_1}10^{-IL(f_1)/20} & f_1 10^{-IL(f_1)/20} & {f_1}^2 10^{-IL(f_1)/20} \\ 10^{-IL(f_2)/20} & \sqrt{f_2}10^{-IL(f_2)/20} & f_2 10^{-IL(f_2)/20} & {f_2}^2 10^{-IL(f_2)/20} \\ \dots & \dots & \dots & \dots \\ 10^{-IL(f_N)/20} & \sqrt{f_N}10^{-IL(f_1)/20} & f_N 10^{-IL(f_N)/20} & {f_N}^2 10^{-IL(f_1)/20} \end{matrix} \quad (4)$$

The weighted insertion loss vector L is given by (5).

$$L = \begin{bmatrix} IL(f_1)10^{-IL(f_1)/20} \\ IL(f_2)10^{-IL(f_2)/20} \\ \dots \\ IL(f_N)10^{-IL(f_N)/20} \end{bmatrix} \quad (5)$$

A figure of merit for a channel that is based on ILD(f) involves the integration of ILD(f) across frequency by using a window function and is given by (6). The unit of FOM_{ILD} is decibel.

$$FOM_{ILD} = \left[\frac{1}{N}\sum_n W(f_n)\, ILD^2(f_n)\right]^{1/2} \quad (6)$$

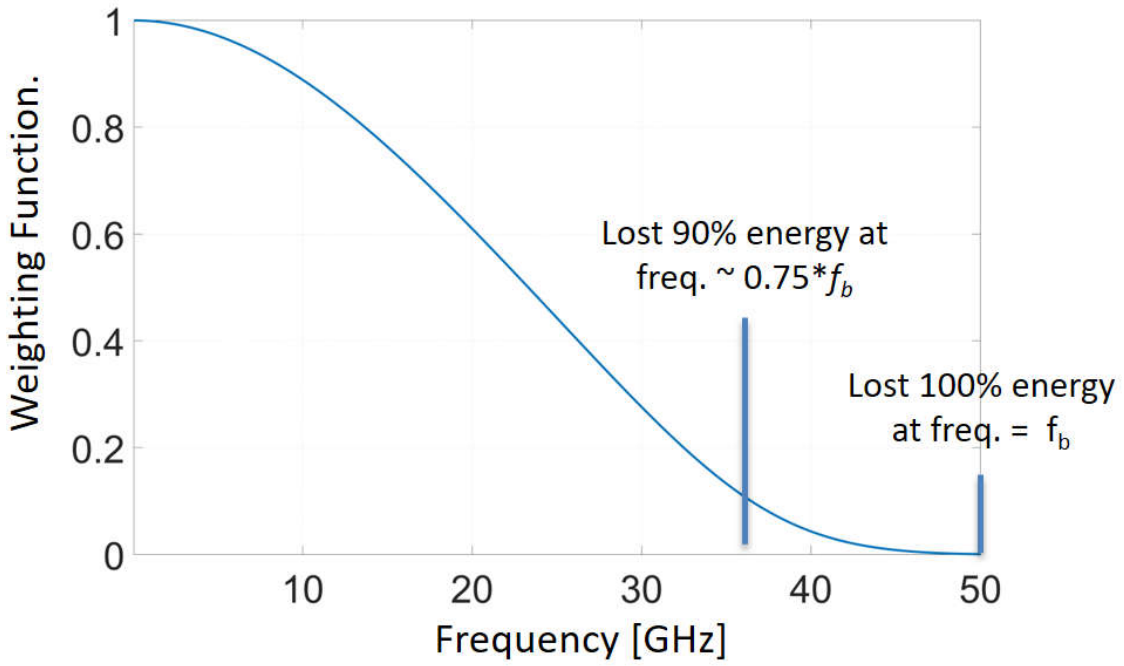

Figure 2. Weighting function for 106.25 Gbps PAM4 signaling.

The window function ($W(f_n)$) is given by (7), which represents the power spectral density of Random Bit Sequence $\left(sinc^2(f_n/f_b)\right)$, transmitter output bandwidth derived from the rise and all time $\left(\frac{1}{(1+(f_n/f_t))^4}\right)$ & receiver noise filter bandwidth $\left(\frac{1}{(1+(f_n/f_r))^8}\right)$.

$$W(f_n) = sinc^2(f_n/f_b)\left(\frac{1}{(1+(f_n/f_t))^4}\right)\left(\frac{1}{(1+(f_n/f_r))^8}\right) \quad (7)$$

Where,

f_n is the nth frequency point.
f_b is the signaling rate.
f_t is the 3 dB transmit filter bandwidth, which is inversely proportional to the 20% to 80% rise and fall time (T_t) given by the constant of proportionality using $0.2365 = T_t f_t$.
f_r is the 3 dB reference receiver bandwidth.

Fig. 2 shows the weighting function for 106.25 Gbps PAM4 signaling where f_b is 53.125 GHz, f_t is 0.2365/ (4*f_b) and f_r is 0.75*f_b. It is important to note that 90% of the energy is lost at 36.46 GHz which is approximately 0.75*f_b and that the weighting function reaches zero at frequency of f_b.

What is figure of merit of RILN?

RILN is an alternate to ILD in presenting a methodology of dissecting the loss and reflection from a measured S-parameter insertion loss from a physics perspective. It involves zeroing out the reflections at both ports of the network.

RILN is the decibel difference between the measured insertion loss and reflectionless insertion loss (RIL) which is the insertion loss corresponding to zero reflections by terminating the network with frequency dependent complex value of impedance [XYZ].

$$RILN(f) = IL(f) \quad RIL(f) \tag{8}$$

The concept of power wave scattering matrix renormalization is used in finding the frequency dependent complex values of impedance for termination in having the renormalized return loss at both ends of the component equal to zero.

Similar to FOM_{ILD}, Figure of merit of RILN (FOM_{RILN}) is the integration of RILN over frequency by using the weighting function $W(f_n)$ defined in (7). The unit of FOM_{RILN} is decibel.

$$FOM_{RILN} = \left[\frac{1}{N}\sum_{n} W(f_n)\, RILN^2(f_n)\right]^{1/2} \tag{9}$$

I. Power wave scattering matrix renormalization

The renormalization of the power wave scattering matrix which involves change in the port reference impedance and the corresponding scattering matrix changes from S to S', which is given by the following [2-4].

$$S' = A^{-1}(S \quad \Gamma^H)(1 \quad \Gamma S)^{-1}A^H \tag{10}$$

Where,

Γ and A are diagonal matrices with their n[th] diagonal term being $\widehat{\rho_n}(\widehat{Z_n})$ and $\frac{1-\widehat{\rho_n}(\widehat{Z_n})}{|1-\widehat{\rho_n}(\widehat{Z_n})|}\sqrt{|1 \quad \widehat{\rho_n}(\widehat{Z_n})\widehat{\rho_n}(\widehat{Z_n})|}$ respectively.

A^H is the Hermitian transpose of a matrix A.

The hat, ^, implies that the terms are complex numbers.

It is important to note that $\widehat{\rho_n}(\widehat{Z_n})$ is the power wave reflection coefficient of the new n[th] port reference impedance ($\widehat{Z_n}'$) with the respect to the complex conjugate of the original nth port reference impedance ($\widehat{Z_n}$) which is given by the following [4].

$$\widehat{\rho_n}(\widehat{Z_n}) = \frac{\widehat{Z_n}' \quad \widehat{Z_n}}{\widehat{Z_n}' + \widehat{Z_n}} \tag{11}$$

II. Zeroing out the reflections

Zero reflections would translate to the diagonal terms of the renormalized scattering matrix (S') equal to zero. In the case of a two port network, (10) becomes the following.

$$\begin{bmatrix} 0 & S'_{12} \\ S'_{21} & 0 \end{bmatrix} = \begin{bmatrix} \frac{1-\widehat{\rho_1}(\widehat{Z_1})}{|1-\widehat{\rho_1}(\widehat{Z_1})|}\sqrt{\left|1 \quad \widehat{\rho_1}(\widehat{Z_1})\widehat{\rho_1}(\widehat{Z_1})\right|} & 0 \\ 0 & \frac{1-\widehat{\rho_2}(\widehat{Z_2})}{|1-\widehat{\rho_2}(\widehat{Z_2})|}\sqrt{\left|1 \quad \widehat{\rho_2}(\widehat{Z_2})\widehat{\rho_n}(\widehat{Z_n})\right|} \end{bmatrix}^{-1} * \left(\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} \widehat{\rho_1}(\widehat{Z_1}) & 0 \\ 0 & \widehat{\rho_2}(\widehat{Z_2}) \end{bmatrix}^H\right) \left(\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \widehat{\rho_1}(\widehat{Z_1}) & 0 \\ 0 & \widehat{\rho_2}(\widehat{Z_2}) \end{bmatrix}\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}\right)^{-1} \begin{bmatrix} \frac{1 \quad \widehat{\rho_1}(\widehat{Z_1})}{|1 \quad \widehat{\rho_1}(\widehat{Z_1})|}\sqrt{\left|1 \quad \widehat{\rho_1}(\widehat{Z_1})\widehat{\rho_1}(\widehat{Z_1})\right|} & 0 \\ 0 & \frac{1 \quad \widehat{\rho_2}(\widehat{Z_2})}{|1 \quad \widehat{\rho_2}(\widehat{Z_2})|}\sqrt{\left|1 \quad \widehat{\rho_2}(\widehat{Z_2})\widehat{\rho_2}(\widehat{Z_2})\right|} \end{bmatrix}^H \tag{12}$$

This leads to the following two equations by equating the diagonal terms of the left hand side and right hand side of (10).

$$\left(S_{11} \quad \widehat{\rho_1}(\widehat{Z_1})\right)\left(1 \quad \widehat{\rho_2}(\widehat{Z_2})S_{22}\right) + \widehat{\rho_2}(\widehat{Z_2})S_{12}S_{21} = 0 \tag{13}$$

$$\left(S_{22} \quad \widehat{\rho_2}(\widehat{Z_2})\right)\left(1 \quad \widehat{\rho_1}(\widehat{Z_1})S_{11}\right) + \widehat{\rho_1}(\widehat{Z_1})S_{12}S_{21} = 0 \tag{14}$$

With a further reordering of (13) and (14), it can be shown that these two equation are similar as that in [4]. The concept of power waves for maximum power transfer is used intensively for amplifier design but not much has been utilized for signal integrity applications.

In solving the simultaneous equations (13) and (14) together, it leads to the following quadratic equations.

$$\begin{aligned} &\widehat{\rho_1}^2(\widehat{Z_1})\left(S_{11} + S_{11}S_{22}S_{22} \quad S_{12}S_{21}S_{22}\right) + \\ &\widehat{\rho_1}(\widehat{Z_1})\left(1 + S_{11}S_{11} + S_{11}S_{22}S_{12}\,S_{21} \quad S_{12}S_{21}S_{12}\,S_{21}\right. \\ &\left.S_{11}S_{22}S_{11}\,S_{22} + S_{12}S_{21}S_{11}\,S_{22} \quad S_{22}S_{22}\right) + \\ &+\left(S_{11} \quad S_{22}S_{12}\,S_{21} + S_{22}S_{11}\,S_{22}\right) = 0 \end{aligned} \tag{15}$$

$$\begin{aligned} &\widehat{\rho_2}^2(\widehat{Z_2})\left(S_{22} + S_{22}S_{11}S_{11} \quad S_{12}S_{21}S_{11}\right) + \\ &\widehat{\rho_2}(\widehat{Z_2})\left(1 + S_{22}S_{22} + S_{11}S_{22}S_{12}\,S_{21} \quad S_{12}S_{21}S_{12}\,S_{21}\right. \\ &\left.S_{11}S_{22}S_{11}\,S_{22} + S_{12}S_{21}S_{11}\,S_{22} \quad S_{11}S_{11}\right) + \\ &+\left(S_{22} \quad S_{11}S_{12}\,S_{21} + S_{11}S_{11}\,S_{22}\right) = 0 \end{aligned} \tag{16}$$

This will lead to two solutions for $\widehat{\rho_1}(\widehat{Z_1})$ and $\widehat{\rho_2}(\widehat{Z_2})$ and the right solution is chosen based on the requirement that $|\widehat{\rho_1}(\widehat{Z_1})| < 1$ and $|\widehat{\rho_2}(\widehat{Z_2})| < 1$ given the real part of the impedance is to be positive. By knowing the reflection coefficient the corresponding impedance can be found by (9).

The application of the frequency-dependent complex values of impedance for the channel termination through the presented power wave scattering matrix theory leads to zero reflections at both the transmitter and receiver ports of the network & the corresponding insertion loss of this network may be called as the reflectionless insertion loss (RIL) of the network which is given by the below equation.

$$RIL = S21' = \frac{\left(\frac{1 \quad \widehat{\rho_1}(\widehat{Z_1})}{|1 \quad \widehat{\rho_1}(\widehat{Z_1})|}\sqrt{|1 \quad \widehat{\rho_1}(\widehat{Z_1})\widehat{\rho_1}(\widehat{Z_1})|}\right)}{\frac{1 \quad \widehat{\rho_2}(\widehat{Z_2})}{|1 \quad \widehat{\rho_2}(\widehat{Z_2})|}\sqrt{|1 \quad \widehat{\rho_2}(\widehat{Z_2})\widehat{\rho_n}(\widehat{Z_n})|}}.$$

$$\frac{\left((S_{21})(1 \quad \widehat{\rho_2}(\widehat{Z_2})S_{22}) + \left(S_{22} \quad \widehat{\rho_2}(\widehat{Z_2})(\widehat{\rho_2}(\widehat{Z_2})S_{21})\right)\right)}{\left((1 \quad \widehat{\rho_2}(\widehat{Z_2})S_{22})(1 \quad \widehat{\rho_1}(\widehat{Z_1})S_{11}) \quad \widehat{\rho_1}(\widehat{Z_1})\widehat{\rho_2}(\widehat{Z_2})S_{12}S_{21}\right)} \quad (17)$$

III. Verification on zeroing out the reflections

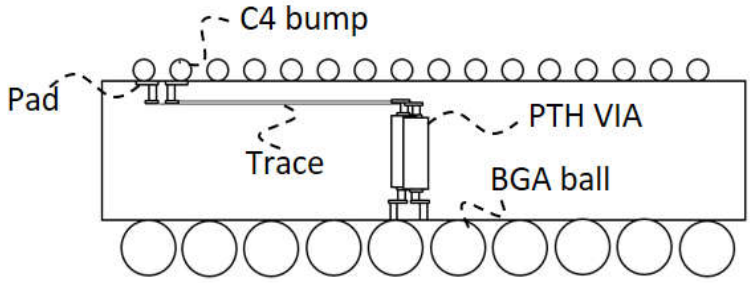

Figure 3. Reference package overview.

In verifying the derived (13) and (14), the reference package model defined by the IEEE 802.3 Ethernet specification [5]. Fig. 3 gives an overview of the reference package model, which consists of a controlled collapse chip connection (C4) bump, trace of 30 mm length and 87.5 Ohm differential impedance, plated through hole (PTH) Via of 1.8 mm length and 92.5 Ohm differential impedance & ball grid array (BGA) ball. The C4 and BGA ball capacitance corresponds to 110 fF and 80 fF respectively.

Fig. 4 shows the right frequency-dependent complex values of impedance for zero reflections, the insertion loss with zero reflections and the return loss plot.

The frequency-dependent impedance characteristics for the launch from the BGA ball appears to have an inductive peak in the 10 GHz to 20 GHz frequency range due to the

launch seeing an inductive PTH via right after the capacitive BGA ball followed by trace. While for the launch from the C4 bump side, the inductive PTH via is at the far end and its inductive effect gets canceled out due by the trace. These frequency dependent complex values for impedance at the ports of the network can provide valuable information to designers when designing the termination of a channel.

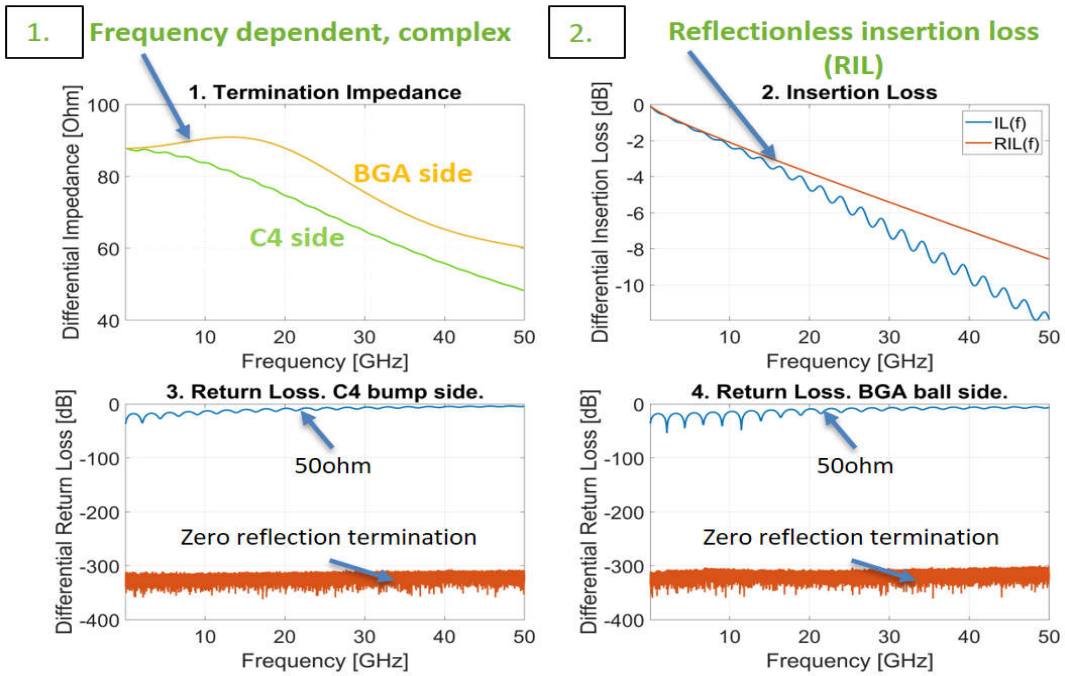

Figure 4. Terminating for zero reflections: 1. Termination Impedance; 2. Insertion Loss; 3. Return loss from C4 bump side; 4. Return loss from BGA ball side.

This verifies the derived (15) and (16) in finding the needed frequency-dependent complex values of impedance in terminating the network corresponding to zero reflections through the power wave scattering matrix theory. Further it does indeed appear that one is able to dissect loss and reflections from a measured S-parameter insertion loss or in turn be able to properly account for loss and reflections.

IEEE802.3cd mated test fixture evaluation for ILN

The IEEE 802.3cd copper twin axial cable specification calls out for checking the FOM_{ILN} of the mated test fixture in accounting for reflections [1]. The test fixtures for the transmitter, the receiver, and the cable assembly measurement are specified in a mated state to enable connections to measurement equipment as illustrated in Figure 5.

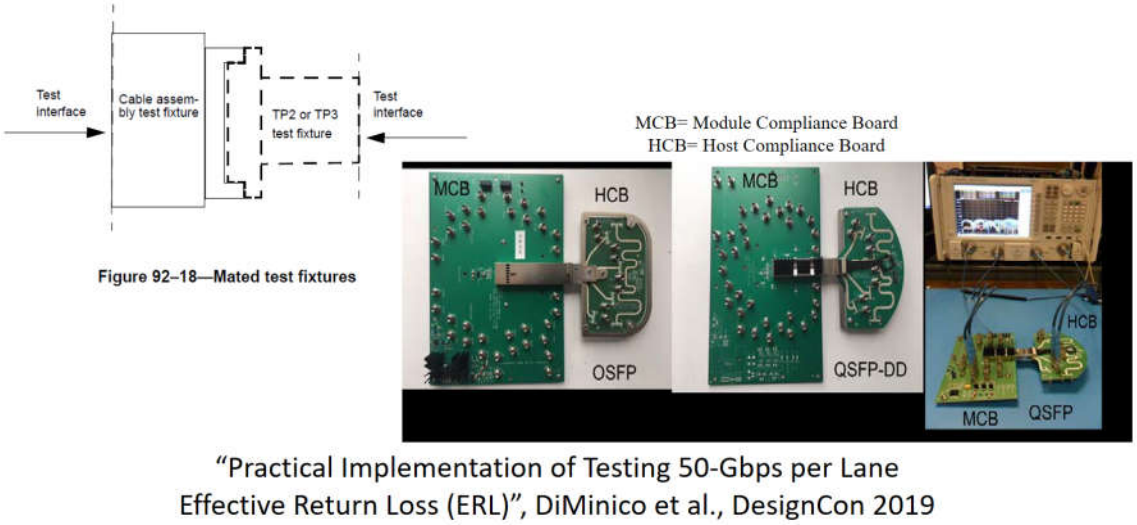

Figure 5. Mated test fixture overview: MCB= Module Compliance Board and HCB= Host Compliance Board.

An Octal Small Formfactor Pluggable (OSFP) and Quad Small Form-Factor Pluggable 28 (QSFP28) mated test fixture is evaluated for FOM_{ILD} and FOM_{RILN} in presenting a real world application. The S-parameter was takes from the IEEE P802.3ck 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force Public Area [XYZ].

Fig. 6 shows the measured insertion loss along with the $IL_{fitted}(f)$ and RIL(f). It can be seen that the fitting of insertion loss is fairly good till 10 GHz and after which there appears significant deviation given the fitting is not able to keep up with the high frequency response.

Fig. 7 shows the insertion loss noise profile in comparing ILD(f) and RILN(f). It can be seen that ILD(f) predicts high noise in the high frequency region. Further ILD(f) has positive and negative dB values while RILN(f) has only negative dB values given it models the physics of the system by using a reflectionless insertion loss where the insertion loss corresponds to zero reflections.

Table. 1 summarizes the figure of merit of the mated test fixture for 56 Gbps PAM4 operation. It can be seen that the FOM_{ILD} is higher than FOM_{RILN}, which may be explained as the fitted insertion loss appears to have perturbations in the low and high frequency. The IEEE 802.3cd MTF specification calls out a figure of noise for insertion loss noise to be less than 0.13 dB and given the high value of FOM_{ILD} there may be false

failures due to badly fitted insertion loss. This gives confidence in helping interconnect designers to migrate in using RIL(f) and FOM_{RILN}.

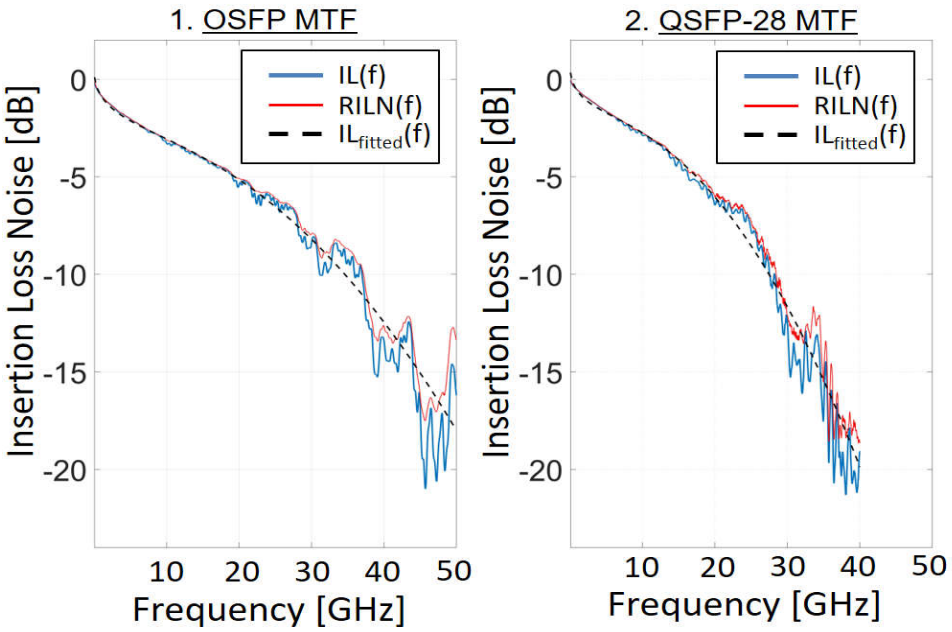

Figure 6. Insertion loss profile of an OSFP and QSFP28 mated test fixture.

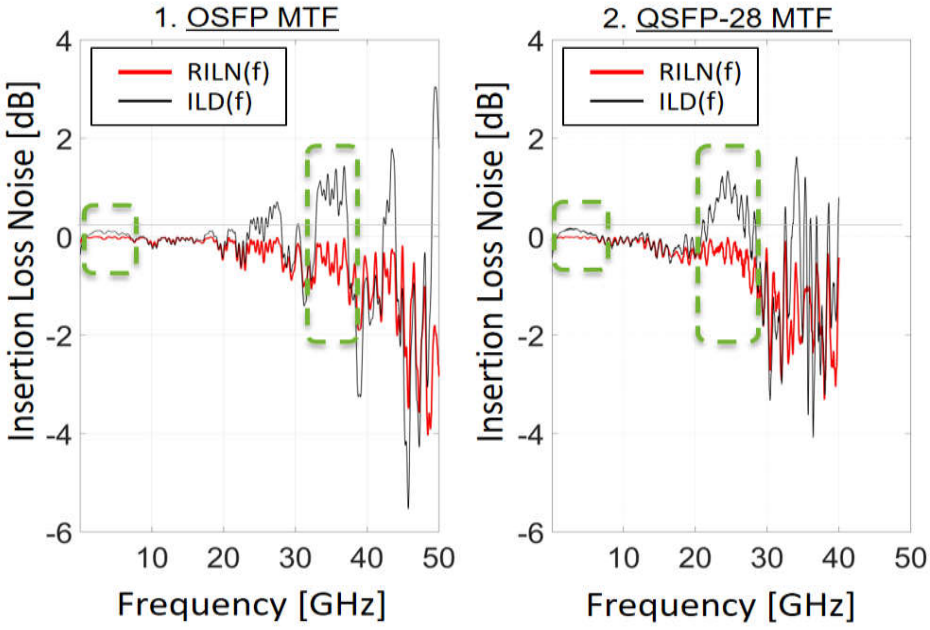

Figure 7. Insertion loss noise profile of an OSFP and QSFP28 mated test fixture.

56 Gbps PAM4	OSFP MTF	QSFP28 MTF
FOM_{ILD}	0.064 dB	0.090 dB
FOM_{RILN}	0.042 dB	0.071 dB

Table 1. Figure of merit of the mated test fixture.

PCB via evaluation with ILN and RILN

Return loss (RL) or time domain reflectometry (TDR) is used to verify the reflections while optimizing a component or DUT such as PCB via, connector, etc. It is difficult to tie either RL or TDR to a data rate and, thus, it is not recommended to be used as a quality factor for reflections. FOM_{RILN} and FOM_{ILD} can be applied for PCB via performance evaluation at given date rate. In this example it is shown that FOM_{RILN} can be used for evaluating via performance evaluation while FOM_{ILD} does not work.

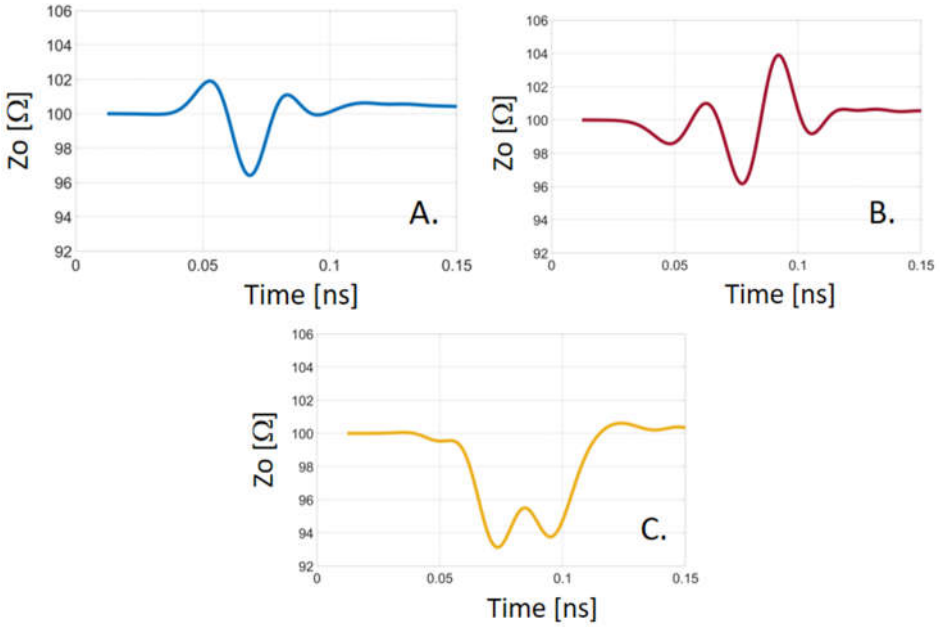

Figure 8. Three VIA optimization TDR profiles: A, B and C.

Fig. 8 shows TDR profiles of three PCB via structures. By looking at TDR plots it is difficult to compare the via performance; (A) it shows best impedance matching, (B) it shows inductive compensation right after capacitive dup, and (C) it shows capacitive dip but least impedance variation. (C) can be mated with ~95ohm channel impedance for best performance at first glance.

Fig. 9 shows insertion loss, return loss and pulse response of three via structures. As shown in the figure, it is difficult to quantify the reflections at given data rate either on frequency domain with insertion loss and return loss or on time domain with pulse response.

FOM_{RILN} can be used to evaluate PCB via for reflections. The benefit of using FOM_{RILN} is that it provides a quality factor in quantifying the amount of reflection at given data rate. Fig. 10 shows the evaluation of the three via structures for reflections in operating at 25, 56 and 106.25 Gbps PAM4 signaling through FOM_{RILN} and FOM_{ILD}. It is observed that FOM_{RILN} values seem more reasonable as it increases with data rate while FOM_{ILD} does not appear to trend well. Through FOM_{RILN} it can be seen that via structure A appears to have relatively lower reflections and may be implemented in designing a system to be operated at 25, 56 and 106.25 Gbps PAM4 signaling.

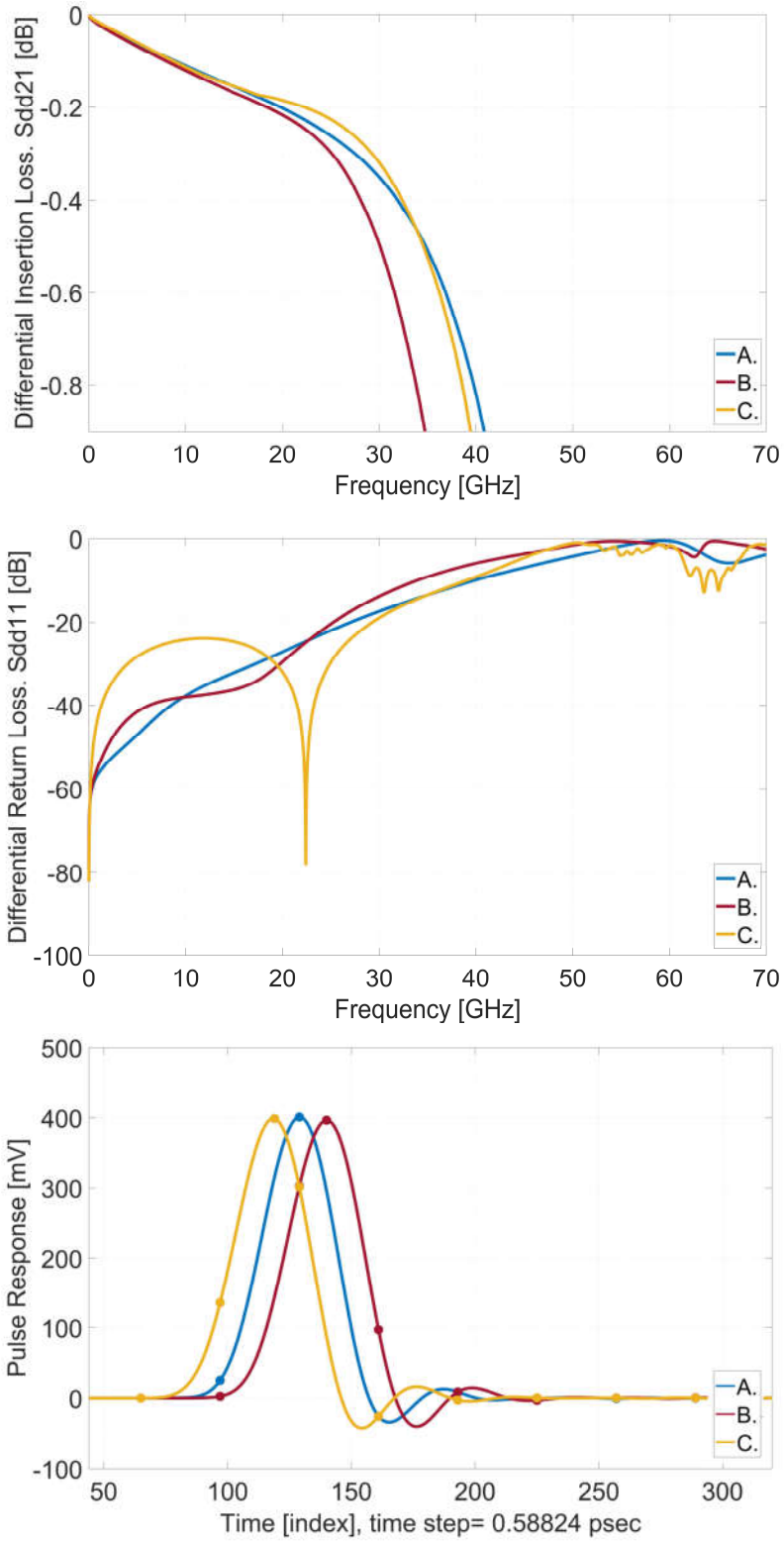

Figure 9. VIA optimizations insertion loss, return loss and pulse response profile.

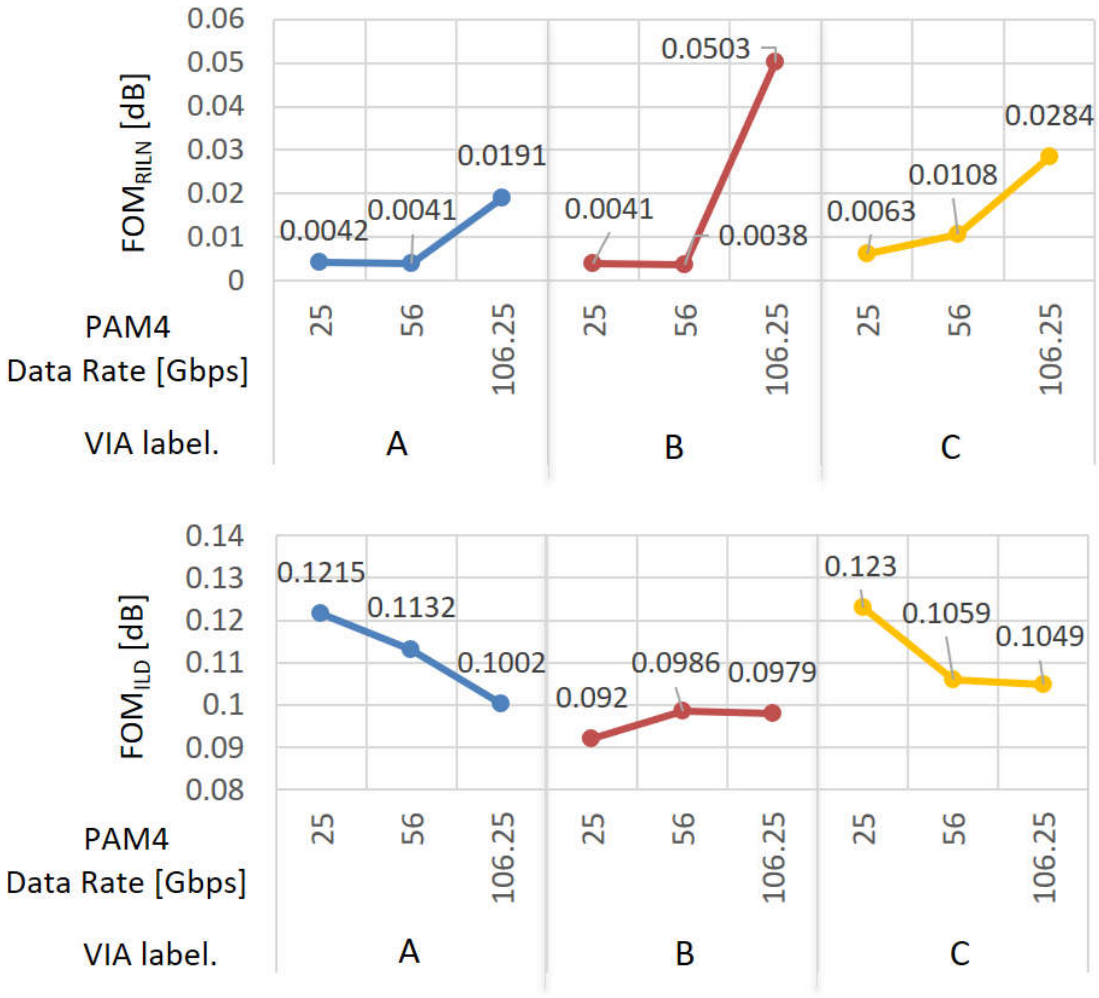

Figure 10. Evaluation of the three via structures for reflections using FOM_{RILN} and FOM_{ILD}.

End-to-end channel evaluation with ILD and RILN

Next, COM, FOM_{ILD} and FOM_{RILN} are evaluated with a cabled backplane channel, which operates at 106.25Gbps PAM4 signaling and the study is performed by varying package trace length, package impedance and on-die resistive termination. Fig. 11 shows the cabled backplane channel model which was taken from the IEEE P802.3ck 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force Public Area [5].

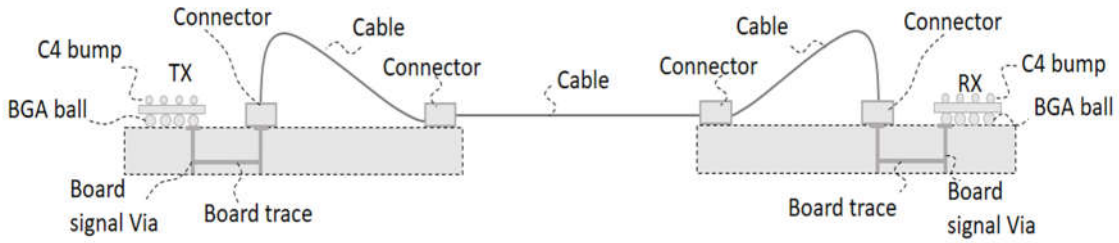

Figure 11. End-to-end cabled backplane channel.

Table. 2 shows the eighteen cases which are generated by varying package length, package impedance, PTH impedance and on-die resistive termination. given an overview of the eighteen cases generated by varying the package definition and on-die resistive termination in capturing the value for end-to-end COM, FOM_{ILD} and FOM_{RILN}. Fig. 12 shows end-to-end COM, $FOMR_{ILN}$ and FOMILD of the eighteen cases.

Case	Package Trace Length/ Zo	PTH Length/ Zo	On-die resistive termination
1.	12mm/90Ω	1.8mm/ 95 Ω	45Ω
2.			50Ω
3.			55Ω
4.	12mm/ 100Ω	1.8mm/ 105 Ω	45Ω
5.			50Ω
6.			55Ω
7.	12mm/ 110 Ω	1.8mm/ 115 Ω	45Ω
8.			50Ω
9.			55Ω
10.	30mm/ 90Ω	1.8mm/ 95 Ω	45Ω
11.			50Ω
12.			55Ω
13.	30mm/ 100Ω	1.8mm/ 105 Ω	45Ω
14.			50Ω
15.			55Ω
16.	30mm/ 110Ω	1.8mm/ 115 Ω	45Ω
17.			50Ω
18.			55Ω

Table 2. Eighteen cases generated by varying package length, package impedance, PTH impedance and on-die resistive termination.

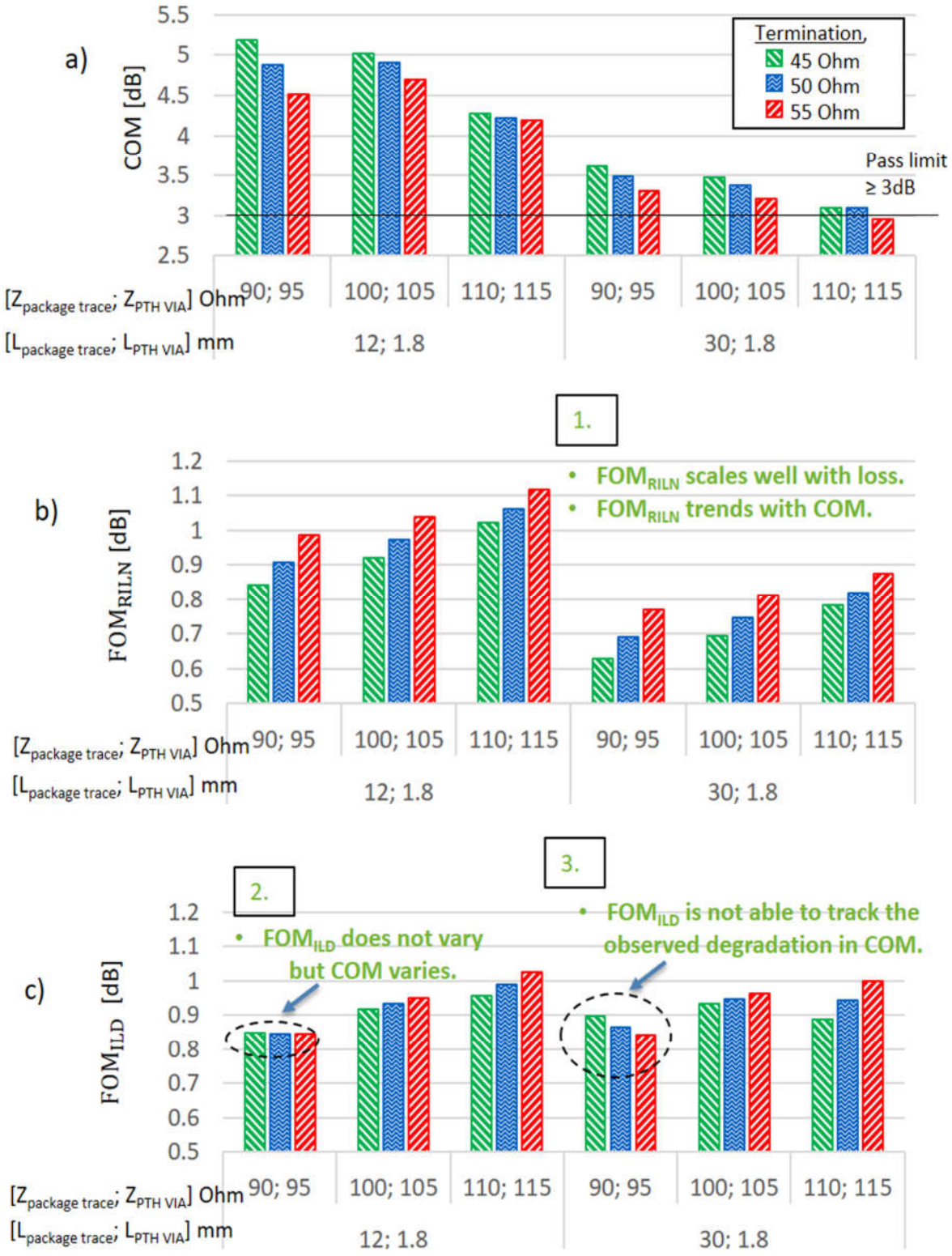

Figure 12. 106.25 Gbps PAM4 signaling sensitivity study of end-to-end COM, FOM_{RILN} and FOM_{ILD} to reflections: a) COM; b) FOM_{RILN} and c) FOM_{ILD}.

It is observed that FOM_{RILN} trends well with COM and loss in presenting a quality metric for reflections with an example of end-to-end channel. On the other hand FOM_{ILD} is not able to keep track of reflections as it does not trend with COM and loss in this example.

As part of this work, the incorporation of reference receiver equalization has not been introduced in the calculation of FOM_{RILN}. Further work will be followed to comprehend the implication of reference receiver equalization into the RILN methodology.

Conclusion

This paper presented the methodology to find termination impedances with zero return loss at both ends. It involves usage of a derived quadratic equation in finding the frequency dependent complex values of termination impedance. The methodology introduced the concept of reflectionless insertion loss (RIL) which corresponds to the measured insertion loss with zeroing out the reflections at both ends.

The concept of RIL was used to calculate the reflective insertion loss noise (RILN) which represents the insertion loss noise only due to the reflection and not the material (heat) loss of the component. Unlike the conventional fitting of insertion loss used in defining the insertion loss deviation (ILD), RILN is derived based on a physics context by zeroing out the reflections. This work may be considered as an evolution of ILD.

This paper also introduced a quality factor called the figure of merit of reflective Insertion Loss Noise (FOM_{RILN}) to quantify reflections as a function of data rate. The method is applied in evaluating reflections of IEEE802.3cd mated test fixtures and optimizing VIA structures for 25, 56 and 106.25 Gbps PAM4 signaling. The results helped to show the advantage of using FOM_{RILN} by comparing it against the conventional FOM_{ILD}. Many cases show that FOM_{ILD} is not responsive to data rate and the fitting the insertion loss shows perturbations in the low and high frequency region.

Finally, COM and FOM_{RILN} are compared with the cabled backplane channel which operates at 106.25Gbps PAM4 signaling. The results shows that FOM_{RILN} and COM are correlated well while FOM_{ILD} deviates from COM margin. The results present FOM_{RILN} as a metric that trends well with COM margin with the example of end-to-end channel.

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