A large, stylized illustration of a tiger's face and upper body, rendered in a light gray color. The tiger is looking towards the right. The illustration is positioned on the left side of the page, behind the main text.

# Pin and Blade Assignment Considerations in Samtec UDX Connectors

Rev.01

## White Paper

**May 2023**

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## Abstract

This document summarizes how the pin and blade assignment impacts power delivery and signal-to-power crosstalk in Samtec UDX6 connectors. The most universal solution is to create a pin and blade assignment that minimizes the current loops, both in the signal pins and power blades.

## Authors

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## Introduction

While the preferred pin assignment in high-speed connectors, including the Samtec AcceleRate® connector family, is well documented and understood, less support material is available on power connectors and power-signal connector crosstalk. This document summarizes some of the important considerations of pin and blade assignment in combination power and signal connectors.

The UDX6 family of connectors, for example, enables higher density designs by providing an AcceleRate high-speed connector and an upgraded mPOWER® blade connector within the same housing (see Figure 1).



Figure 1: The UDX6-10 connector.

## Potential Challenges and Recommended Solutions

In addition to the usual signal-integrity considerations, there are two potential interactions of concern related to power blades: how the blade assignment impacts the power delivery and how the pin and blade assignment impacts signal-to-power and power-to-signal crosstalk.

For power delivery, the resistance (which determines the current carrying capacity) and the loop inductance formed by the blades matter most. The resistance varies, but only slightly with the assignment of pins and blades, and it is influenced by the shape and orientation of the connecting circuit.

The inductance of the power delivery path, which influences the transient response of the power network, changes significantly with the blade assignment. If the inductance of the power delivery path matters for the application, it is typically best practice to

minimize the loop inductance formed by the power and power-return paths. (The loop inductance formed by the blades is directly proportional to the size and shape of the loop.)

If the goal is to minimize loop inductance, then assign the power and power-return (or 'GND') blades in a pattern that forms the smallest possible loop size. This can be achieved by selecting adjacent blades for power and ground. The crosstalk between power blades and high-speed signal pins also depends on the geometry of interacting power and signal loops. This interaction can be minimized by making the loops smaller, by placing them farther apart, or by forming orthogonal loops so that the magnetic coupling is minimized.

We can illustrate the above by looking at the simulated self and transfer inductances of signal pins and power blades. To examine the worst-case scenario (where signal and power conductors are closely spaced providing stronger coupling), we create a version of the connector with four power blades and four rows of ten high-speed signal pins. The connector, port numbering, and port assignment are shown in Figure 2.

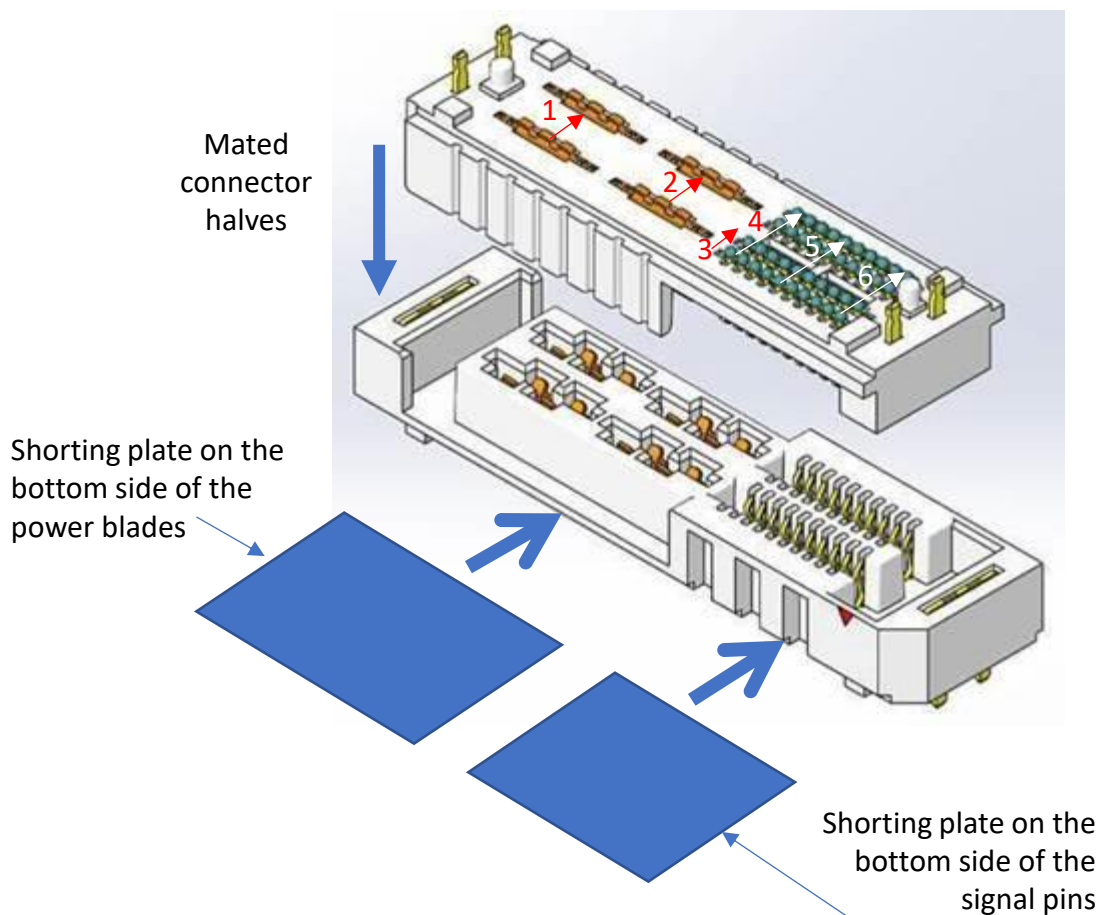


Figure 2: Setup, port numbering (red and white arrows) and port assignment on the connector.

To enable analysis of loop inductance values, we short together all four blades and all forty signal pins on the back side of the receptacle piece. This allows us to simulate the impedance of the loops formed by the pins and blades. The first two ports are assigned to the power blades, the third and fourth ports are across the signal pins closest to the blades, and port five and six are halfway and all the way down the signal block, keeping a bigger distance from the power blades.

These signal pin allocations deliberately do not follow the customary SI pinout, which would be ground-signal-ground in a row for single-ended signals and ground-signal-signal-ground in a row for differential signals. The port and pin allocations shown here illustrate what happens when larger signal-ground loops are used.

Figure 3 shows the imaginary part of the impedance extracted from the self-reflection parameters at the six ports. On the right side of the plot, the cursor readings are shown at 1 MHz frequency.

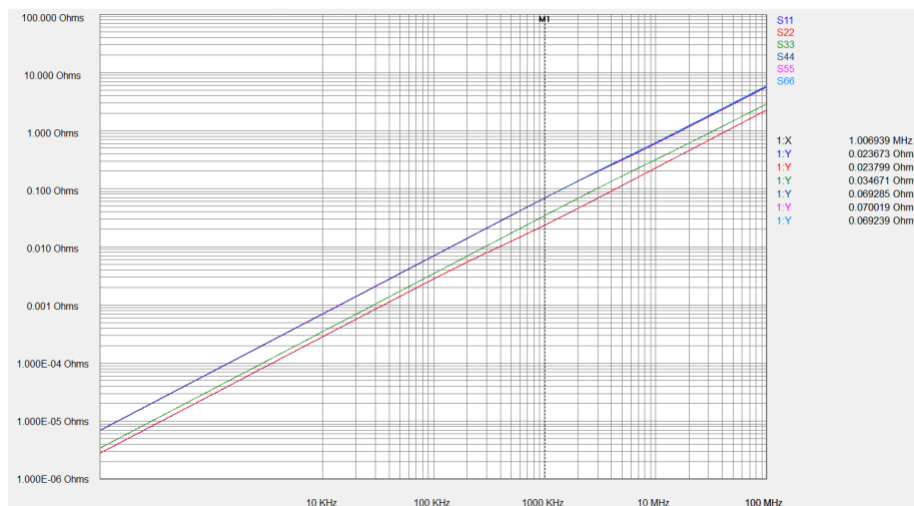


Figure 3: Simulated imaginary part of self-impedance in ohms at the six ports on the connector.

From the cursor values we can calculate the loop inductance values, as shown below:

	Impedance [Ohm]	Inductance [nH]
Port1	0.023673	3.767674968
Port2	0.023799	3.787728491
Port3	0.034671	5.518061032
Port4	0.069285	11.02705023
Port5	0.070019	11.14386996
Port6	0.069239	11.0197291

We can point out that the loop size is nominally the same in the loops of Port1 and Port2, as well as of Port4, Port5, and Port6. As a result, those inductance values match very closely. We also see that the loop size is approximately the same in both groups, but the blades form much wider current paths. Therefore, the blade inductance is lower.

The crosstalk between the power blades as well as between the power blades and signal pins can be captured by the off-diagonal elements of the S parameters. The coupling magnitude to and from Port1 is shown in Figure 4, to and from Port2 is shown in Figure 5.

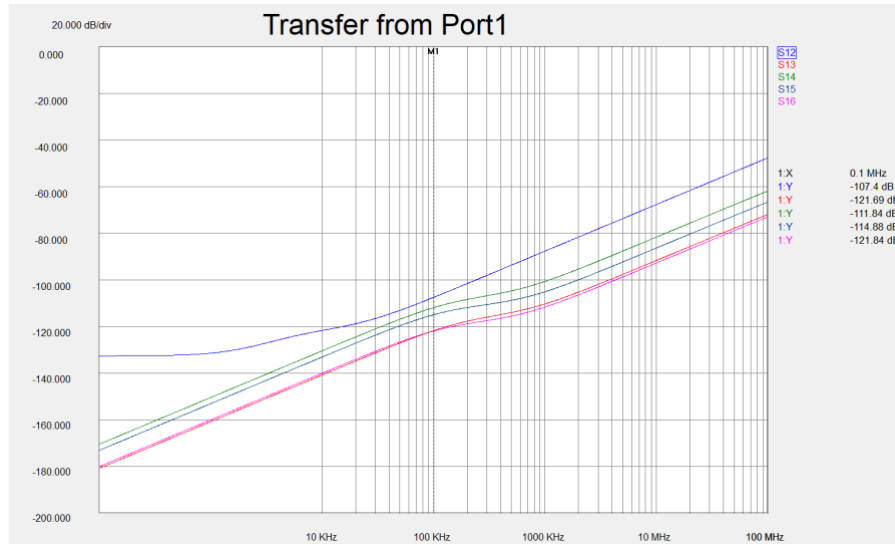


Figure 4: Transfer parameter magnitude to and from Port1 blade loop.

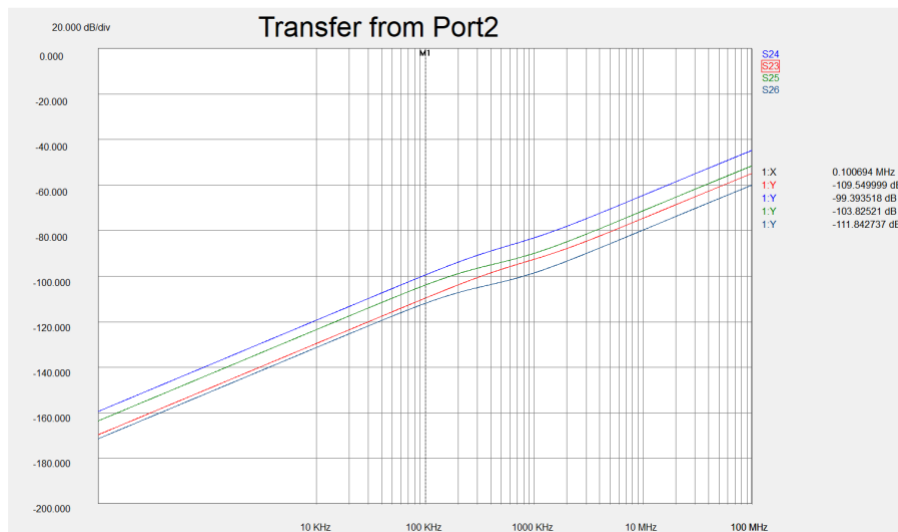


Figure 5: Transfer parameter magnitude to and from Port2 blade loop.

By comparing the data in Figures 4 and 5, we see that there is less coupling from the power blade loop that is further away from the signal pins; this is expected. Note that Figure 4 has one ‘extra’ trace, which is the coupling between blade loops at Port1 and Port2. This is ‘missing’ in Figure 5, simply because it would show the same exact values

that we see in Figure 4. Note that the Port1-Port2 coupling trace in Figure 4 flattens out at very low frequencies. This is not computational error; rather it represents the actual resistive interaction between the blade loops through the shorting plane.

It is important to remember that the S parameter values shown in Figures 4 and 5 provide the signal transfer for source and load terminations, which equal the reference impedance for the S parameters (in this case 50 ohms). For power circuits, lower reference impedance may be customary, such as 0.1 ohms. In this case, since signal pins are also involved, we kept uniformly the 50-ohm reference impedance on all ports. In a circuit, if we know the source and load impedances, we may want to recalculate the transfer parameters.

And one last detail: the above considerations looked at circuit loops, when the signal, whether it is the high-speed signal or power noise, is considered differentially between the pins or blades. Sometimes common-mode noise is also important to minimize. That can be achieved by placing the pins and blades that are 'quieter' with respect to the ambient ground structure next to each other.

## Conclusion

In a high-speed block of pins, assigning signal and ground pins adjacent to each other is the accepted norm. In the power-blade block, assigning power and ground to adjacent blades will provide two benefits. As we saw above, it minimizes the power delivery inductance and simultaneously minimizes the crosstalk between power blades and signal pins. A preferred pin and blade assignment corresponding to the above considerations is shown in Figure 6.

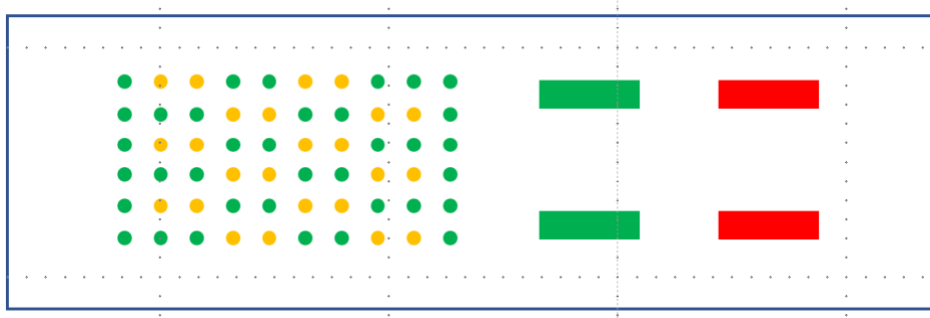


Figure 6: Preferred pin and blade assignment sketch. Green: GND, Red: PWR, Yellow: signal.

## Resources

Adam Gregory, Clement Luk, Gary Biddle, Gustavo Blando, and Istvan Novak, "[Current Distribution, Resistance, and Inductance in Power Connectors](#)," DesignCon 2020.