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New Power Integrity Benchmark for Low Impedance Structures

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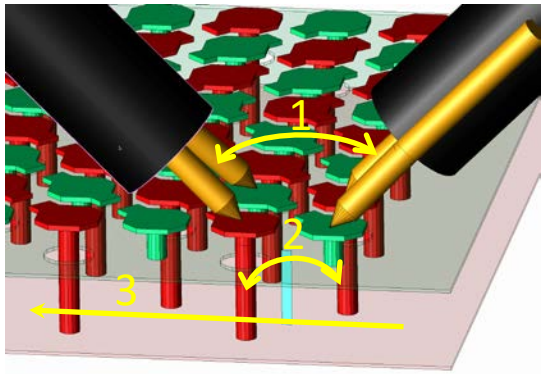
Outline

- Background and motivation
- Description of the test board
- The benchmark problem
- Board stackup
- Board layout
- PCB build options
- Early correlations
- Comparison of various builds
- Three-lab test results
- The major challenges: simulations
- The major challenges: measurement
- Summary, conclusions

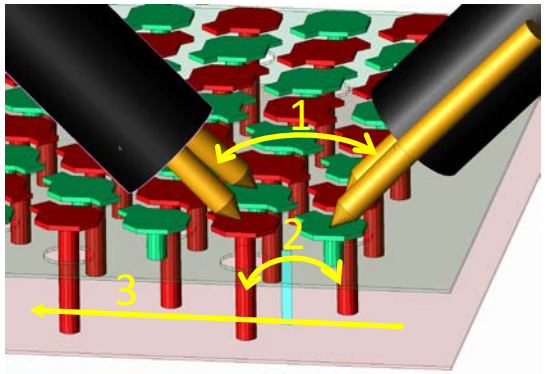
Background and Motivation

- Interfacing to high-power high-density packaging requires arrays of via fields for the power and ground networks.
- Simulating and measuring the power distribution network (PDN) through these via fields to quantify the impedance behavior is problematic, and even the simplest structures can be challenging.
- This benchmark problem is presented as a ‘Challenge Problem’ because it represents a test case near the limits of today’s methods used to correlate structure models to measurements of test vehicles - primarily because of the ultra-low impedances involved.
- Further it represents a test case where the true result is not known to a precision significantly exceeding measurement capability.



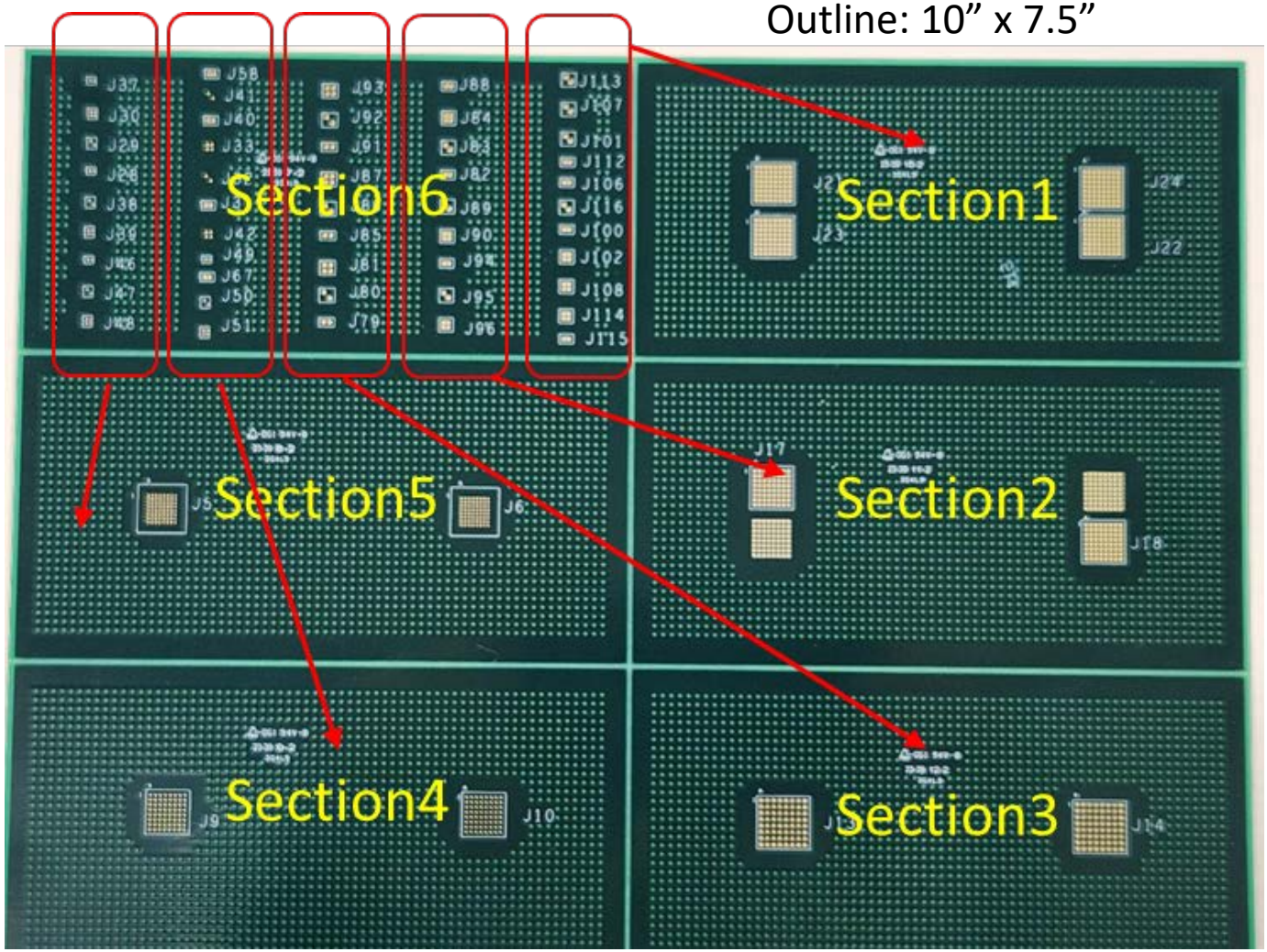
Background and Motivation

- When questions arise about accuracy of models, simulation or measurement results, resolution among DUT designers, instrument vendors and CAD companies is hard.
- The lack of a readily available reference platform, confidentiality concerns about Intellectual Property (IP) included in the Device Under Test (DUT) or details of the measurement instrumentation or details of simulation software hinder the dialog among the parties involved.
- ***To enable better dialog, the goal of this challenge problem is to offer a simple and easy-to-reproduce reference platform that anyone can make, measure and simulate.***

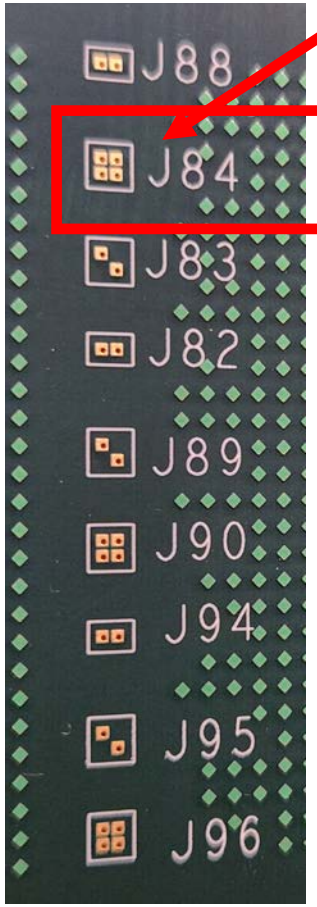


Description of (Full) Board

Outline: 10” x 7.5”



The benchmark structure



J88: both vias (straight) land on L3

J84: all four vias land on L2

J83: both vias (diagonal) land on L2

J82: both vias (straight) land on L2

J89: both vias (diagonal) land on L3

J90: all four vias land on L3

J94: straight pair landing on L2 and L3

J95: diagonal pair landing on L2 and L3

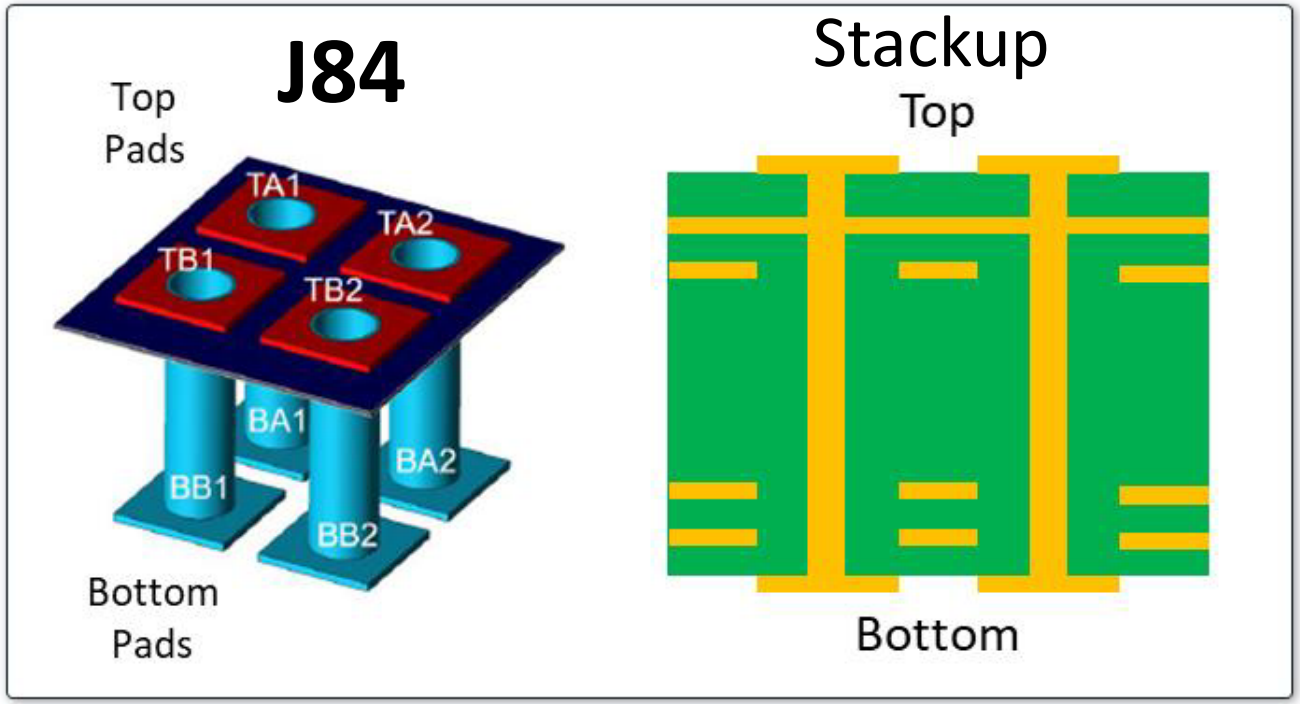
J96: checker-board quad landing on L2 and L3

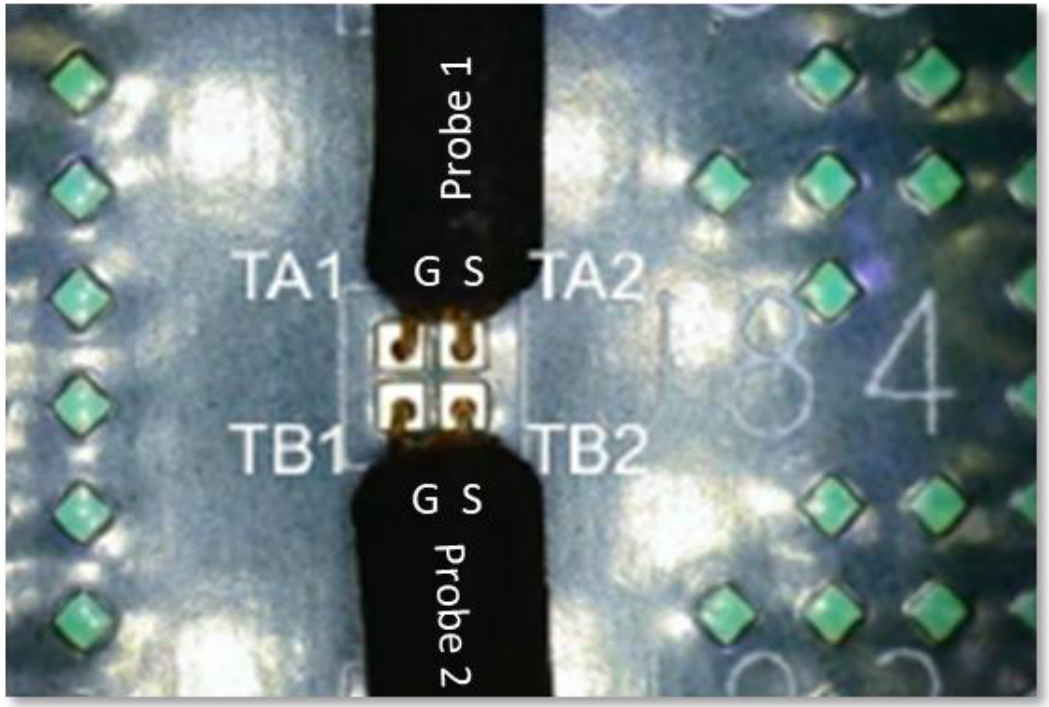
"Introducing an Upcoming IEEE Packaging Benchmark," Signal Integrity Journal, 2024

The Benchmark Piece

Four 15-mil vias on 40-mil square grid
All vias are shorted on L2 plane

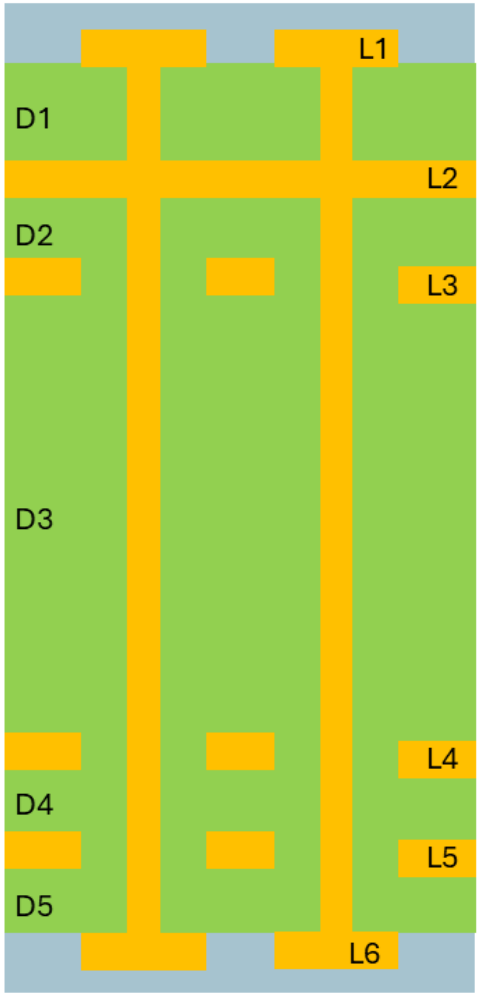
Photo of J84 with two probes
Straight and flipped options





Stackup

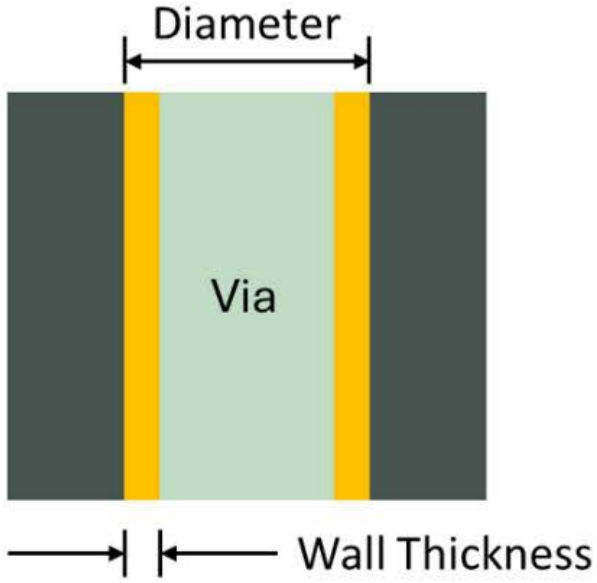
Layer	Material	Nominal Thickness		Cross Section Data	
		mils	µm	mils	µm
	Solder Mask	0.700	18		
L1	Copper	2.000	51	1.75	44
D1	Dielectric	3.064	78	3.07	78
L2	Copper	1.200	30	1.36	35
D2	Dielectric	3.000	76	2.80	71
L3	Copper	1.200	30	1.35	34
D3	Dielectric	40.328	1024	42.10	1069
L4	Copper	1.200	30	1.36	35
D4	Dielectric	3.000	76	3.08	78
L5	Copper	1.200	30	1.36	35
D5	Dielectric	3.064	78	2.98	76
L6	Copper	2.000	51	1.71	43
	Solder Mask	0.700	18		

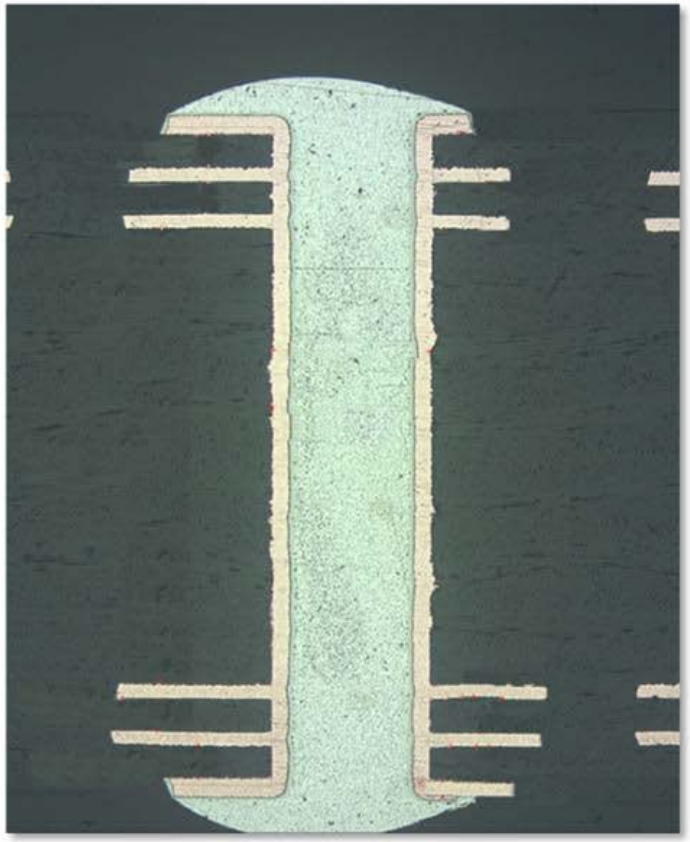


- Nominal stackup dimensions
- Measured cross section dimensions

Via Cross Section Photo

Via Feature	Nominal		Cross Section Data	
	mils	µm	mils	µm
Diameter	15	381	14.6	371
Wall Thickness			1.66	42



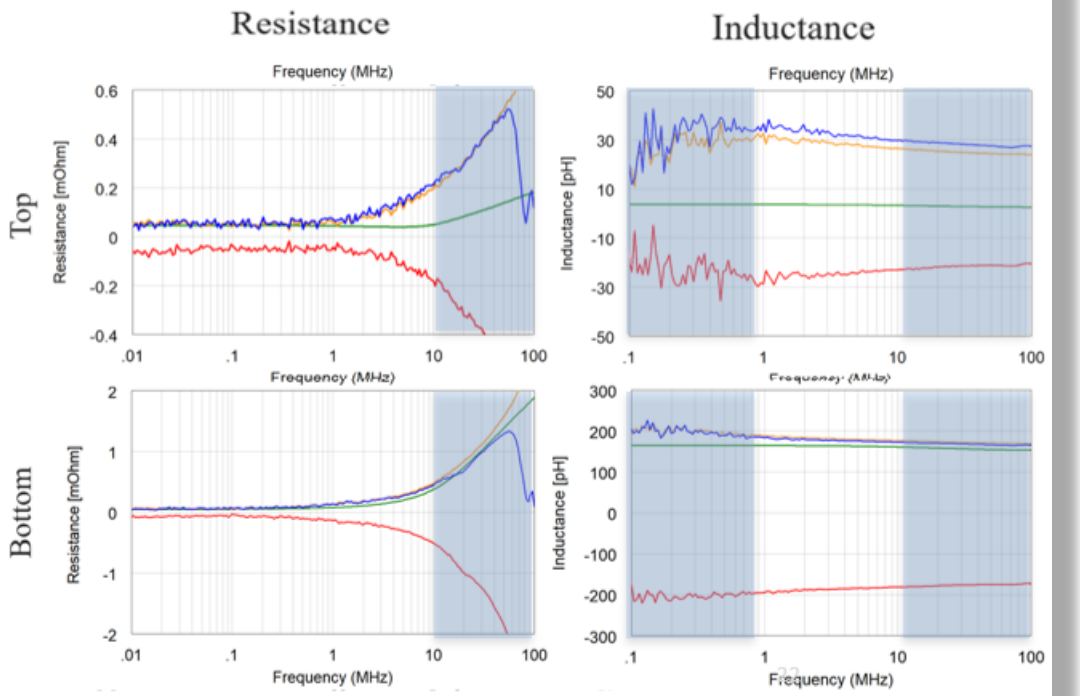


Cross section

- Note the large middle fill in the stackup
- Can accommodate various dielectrics and copper thickness

Early Correlations

- **Measurement depends on orientation of probe**
  - Average of straight and flipped configuration should cancel out probe-to-probe coupling
- **Simulation to measurement**
  - Trends generally similar when comparing to average of straight and flipped orientation
  - Top side probing (short via)
    - Resistance in good agreement to 3 MHz – short via section is masked by probe coupling
    - Measurement series inductance and coupling > inductance being measured . Indications that probe contributes around 30-35pH
  - Bottom side probing (long via)
    - *Good agreement between simulation and measurement but ΔL 35pH – probe coupling may add or subtract from measured DUT impedance*
- **In an actual board you may not have a choice whether probe configuration will be flipped or straight – the uncertainty in L can be a real problem**

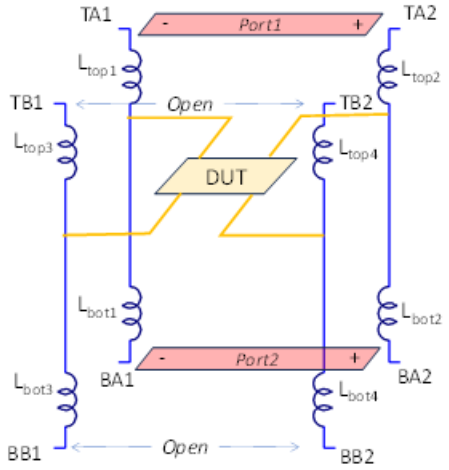


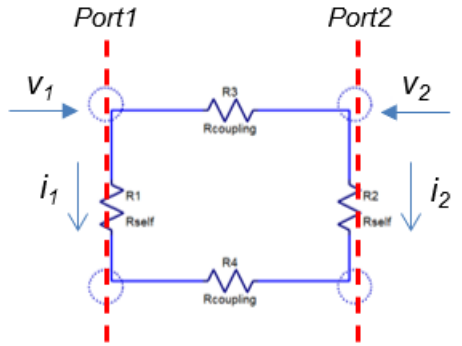
"Impact of Finite Interconnect Impedance Including Spatial and Domain Comparison of PDN Characterization," DesignCon 2024

Impedance Definitions

- The normalized impedance matrix can be calculated from the S parameters
- With two power-ground via pairs, there are multiple options to approximate impedance
  - TOP-DOWN data along one via captures the DUT impedance most closely
    - No loop coupling, no spatial attenuation
  - DUT impedance can be approximated from S21
- The transformation uses all four S parameters
  - Reflection terms are very inaccurate for large reflections
  - For many PDN impedances $|S_{ii}| \sim 1$

$$\begin{bmatrix} Z_{11n} & Z_{12n} \\ Z_{21n} & Z_{22n} \end{bmatrix} = \begin{bmatrix} \frac{2\Delta_1 S_{11} + S_{12}S_{21}}{4} & \frac{S_{12}}{2} \\ \frac{S_{21}}{2} & \frac{2\Delta_2 S_{22} + S_{12}S_{21}}{4} \end{bmatrix}$$

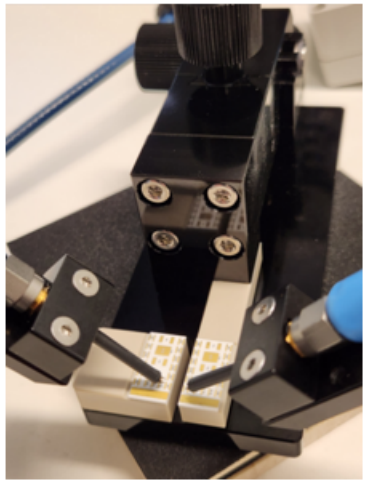




"Impact of Finite Interconnect Impedance Including Spatial and Domain Comparison of PDN Characterization," DesignCon 2024

Measurement Setup, Calibration

- Keysight E5061B-3L5 5Hz-3GHz 2-port VNA
- Keysight N7550A DC-4GHz Ecal unit
- Keysight N85561A mechanical calibration kit
- Custom common-mode choke
- Various sweeps used for the different tests
  - 100Hz-10MHz log (regular impedance measurements)
  - 10Hz-3GHz log (full-band noise floor test)
  - 10kHz-100MHz log (quick checks)
  - 2MHz-3GHz lin (probe characterization)
- PacketMicro RP-GR-121510 1mm probes
- PacketMicro TCS50-V2 calibration substrate
- PacketMicro custom substrate positioner



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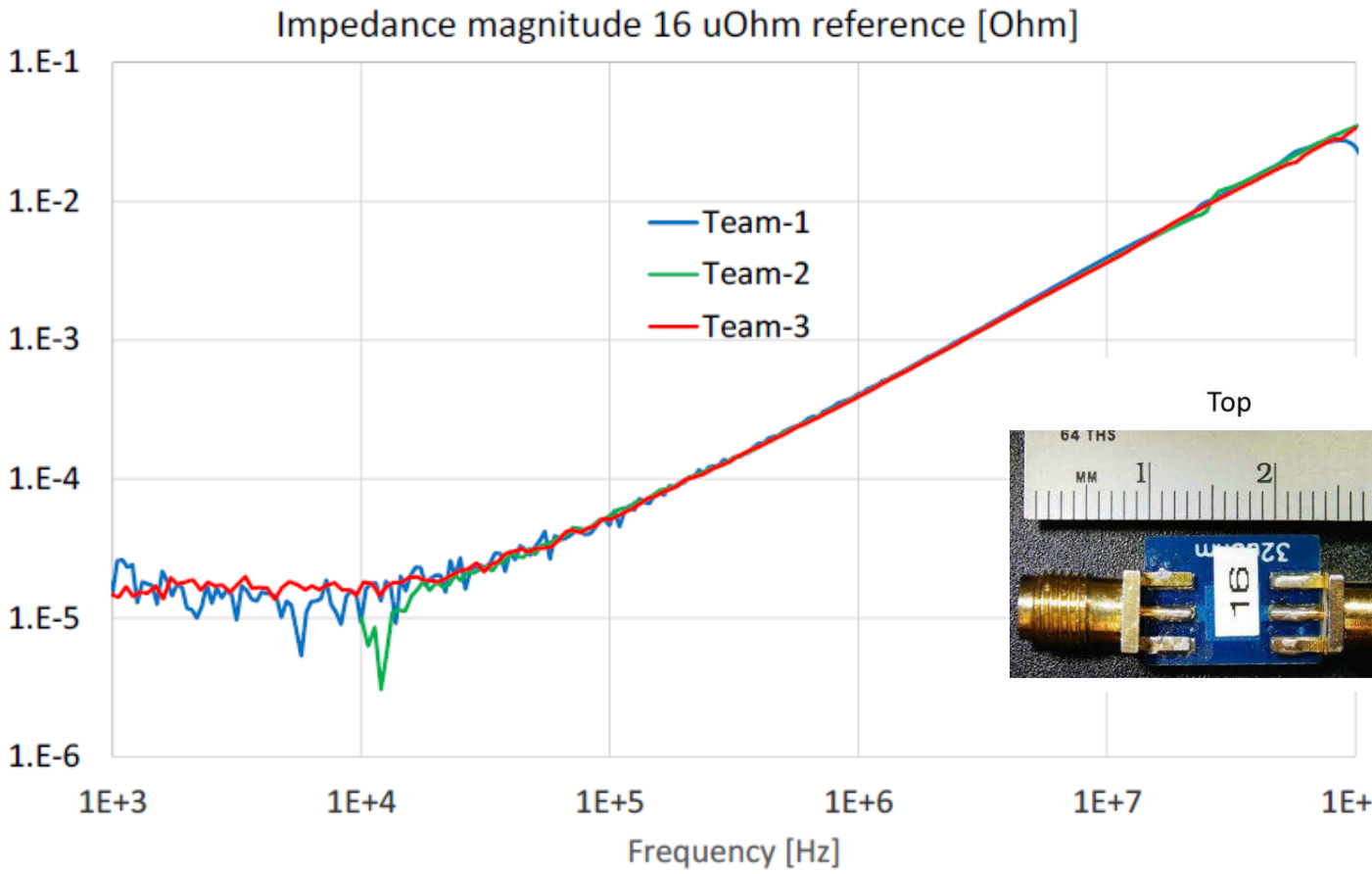
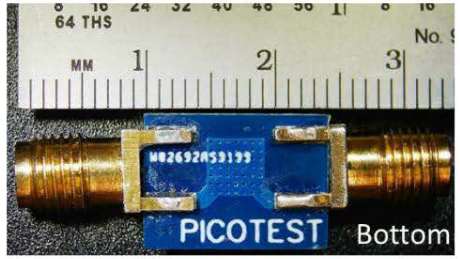
Three-Lab Comparison



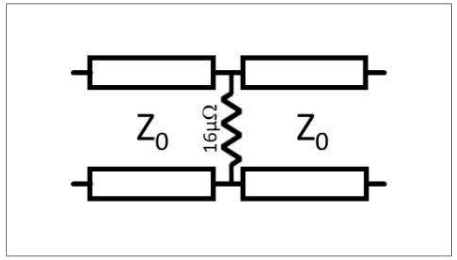
Picotest 16 uOhm shunt element

Top

Bottom

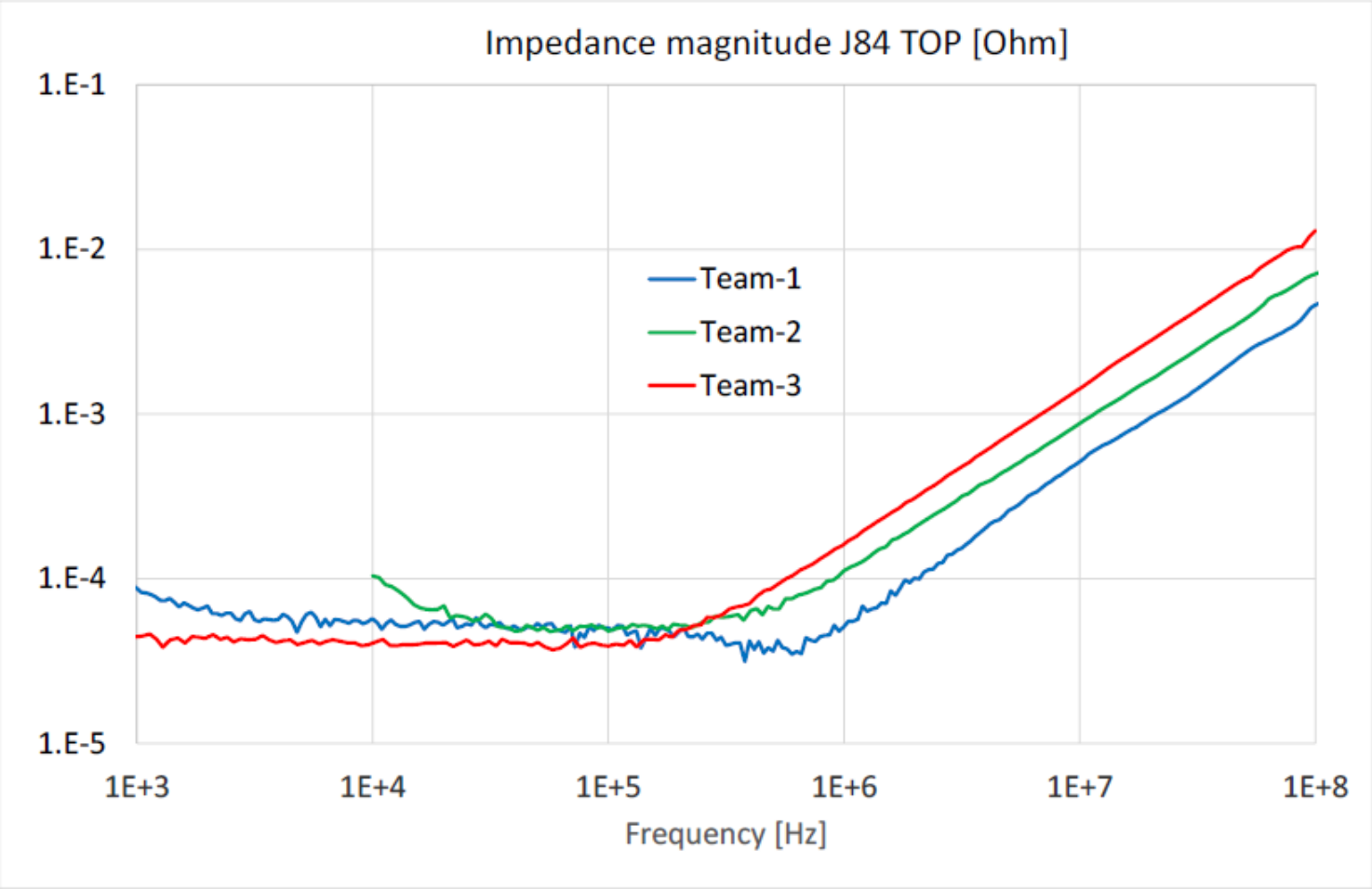


Circuit



"Power Integrity Via Field Impedance Challenge Problem V," online https://packaging-benchmarks.org/repository/available

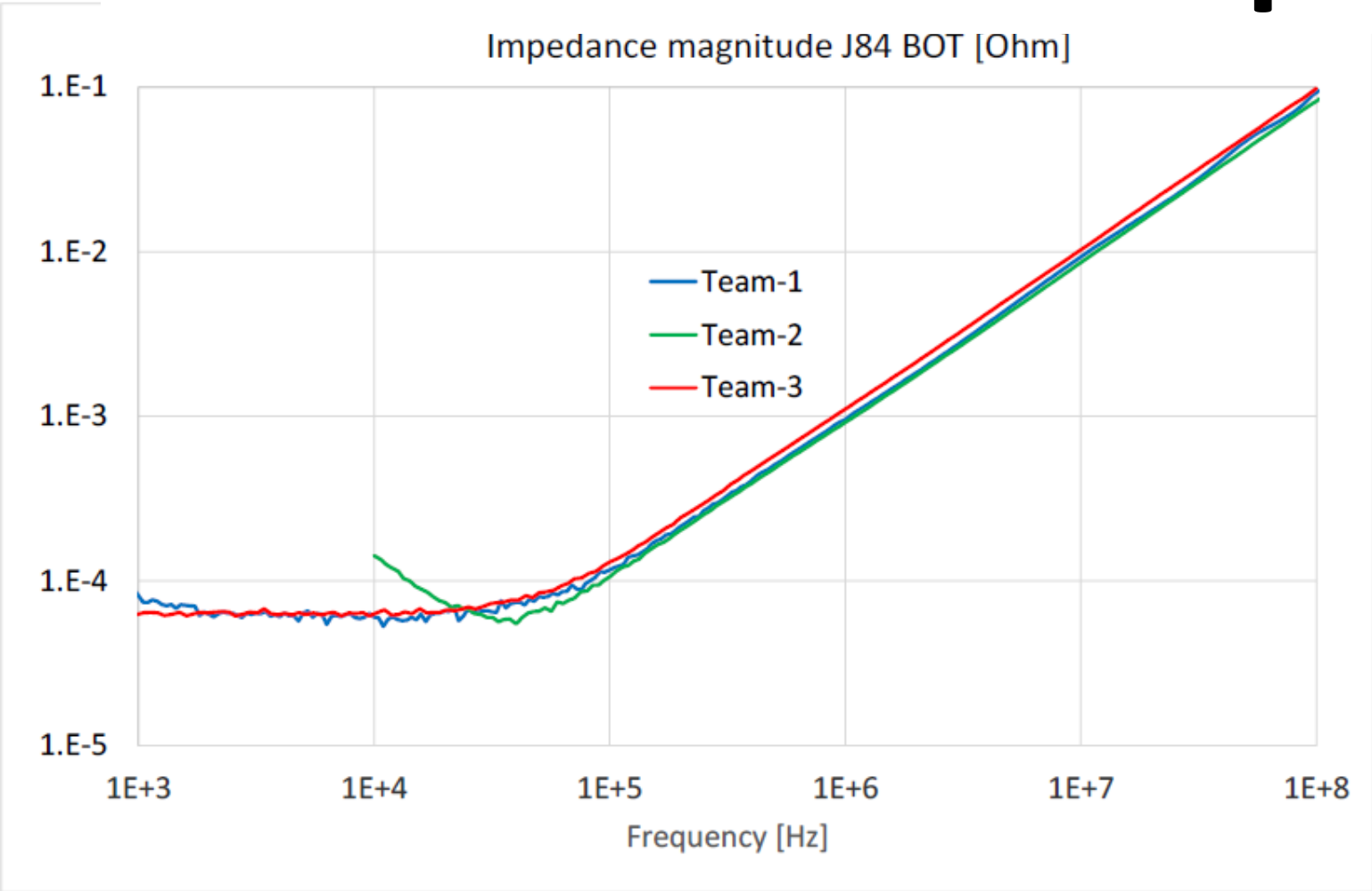
Three-Lab Comparison



- J84 **Top side**
- Short via
- Large probe-tip coupling influence
- Calibration type matters

"Power Integrity Via Field Impedance Challenge Problem V," online https://packaging-benchmarks.org/repository/available

Three-Lab Comparison



- J84 **Bottom side**
- Long via
- Probe-tip coupling influence is less
- Calibration type still matters

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Three-Lab Result Discussion

- The largest differences are on the top side.
  - Vertical via portion is much shorter than the exposed open pins of the probes
  - The collected data varies more with different calibration techniques and probe pitch differences between the labs.
  - No way to determine which of the measurement results, if any, represent the ‘true’ result.
- Smallest differences are when coax connection is used on reference piece

“Power Integrity Via Field Impedance Challenge Problem V,” online https://packaging-benchmarks.org/repository/available

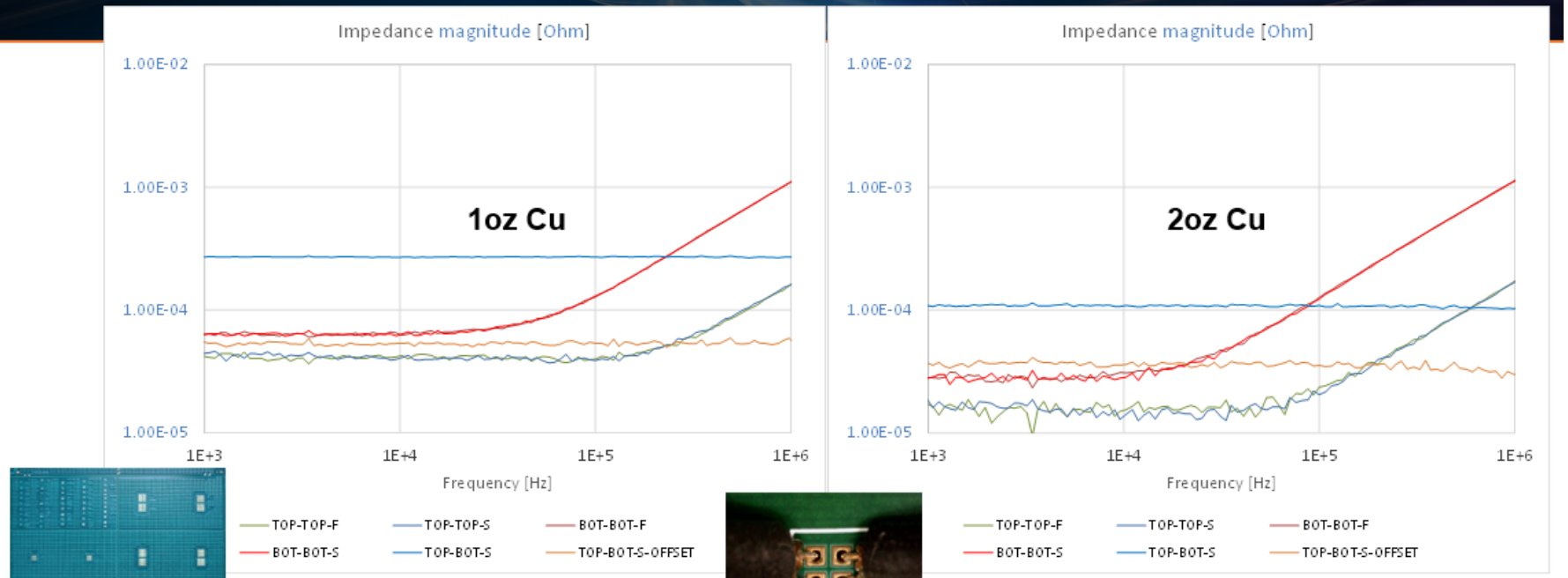
Three-Lab Result Discussion

- The three teams used the same base model of VNA, but the settings, accessories and calibrations were different.
  - At low frequencies, data from Team 2 started at 10 kHz. The slight downslope of the impedance magnitude from Team 2 and Team 3 is due to the insufficient common-mode inductance.
  - At high frequencies the upslope of impedance represents inductance. Teams 1 and 2 used wafer-probe calibrations, which removes the artifacts of the probes, but does not completely remove the impact of probe tip coupling. Team 3 used mechanical calibration kit and the probes were not deembedded.

"Power Integrity Via Field Impedance Challenge Problem V," online https://packaging-benchmarks.org/repository/available

Comparing Different Builds

1oz vs. 2oz Copper



Board with 1oz 3-mil FR4 laminate
Boards courtesy of PacketMicro

Board with 2oz 8um HK04 laminate
Boards courtesy of DuPont

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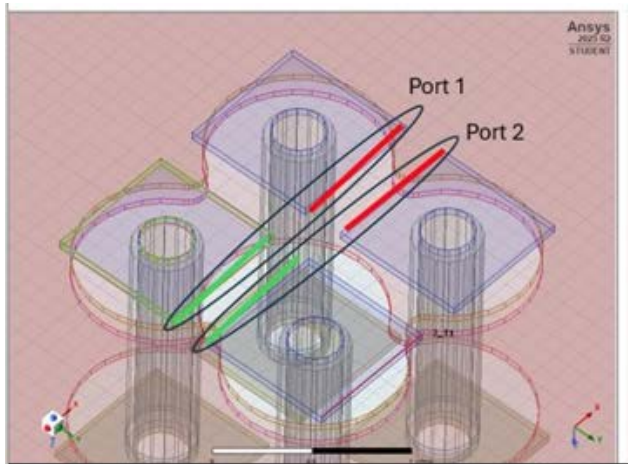
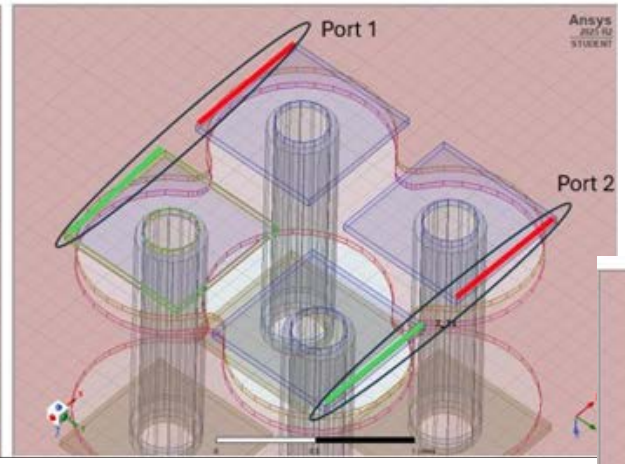
Full-Wave Solver Simulations

Close

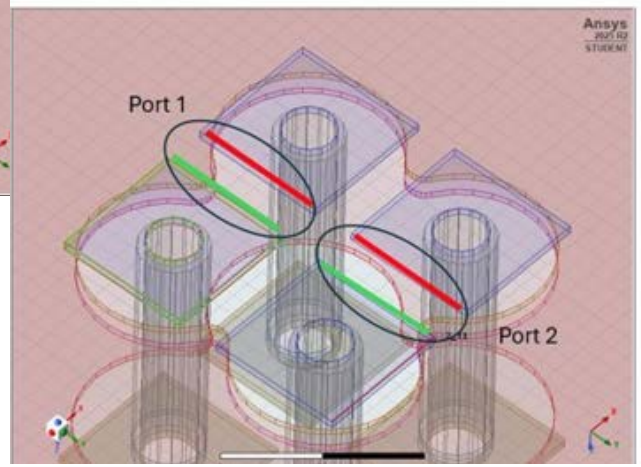


Far

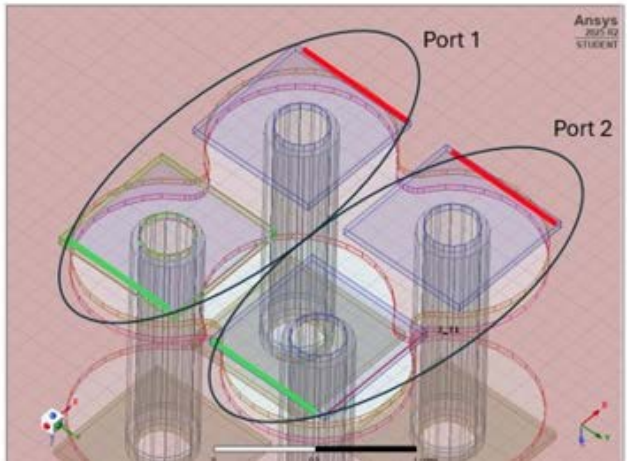


Large number of permutations for port placement

Inner

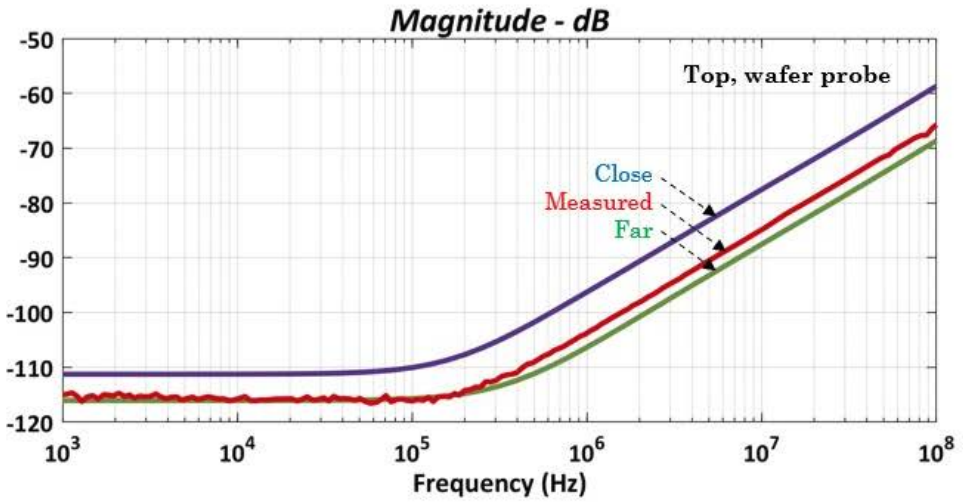


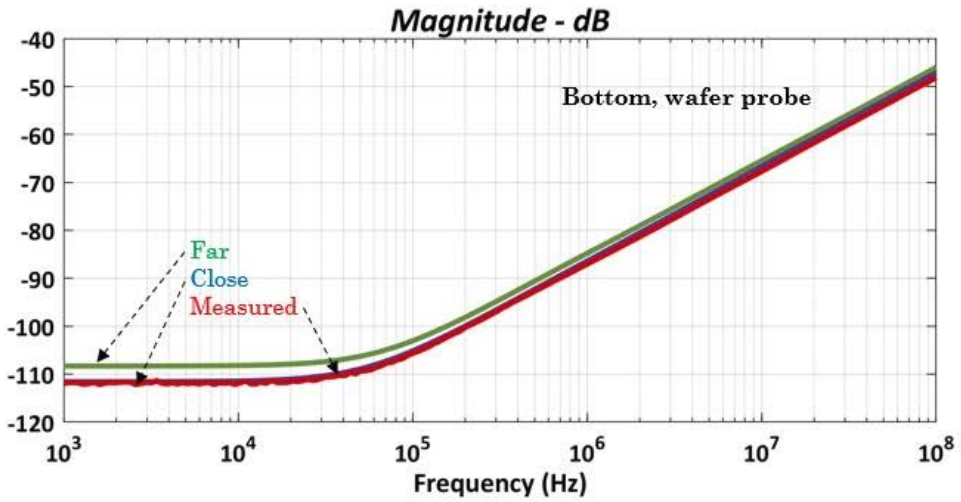
Outer



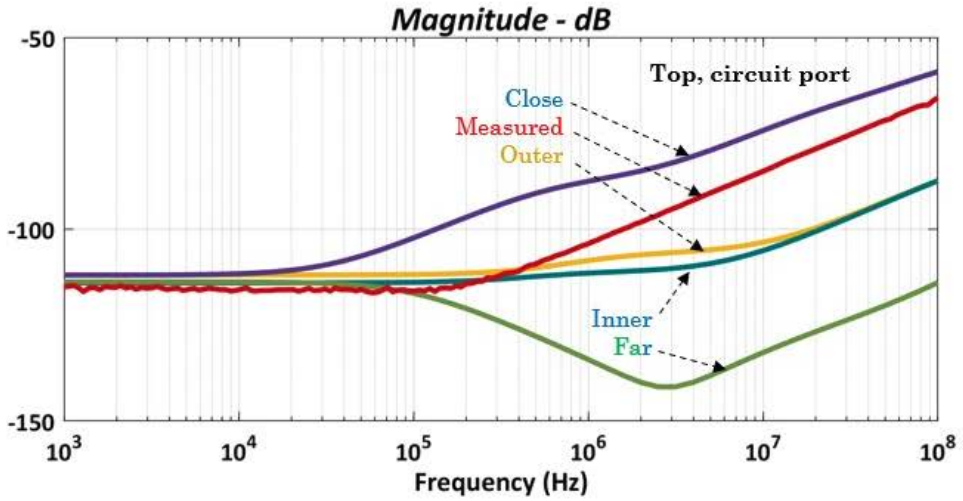
Ajay Thumma, “Power Integrity Correlation Results for IEEE TC-EDMS Benchmark Problem 5,” submitted to Signal Integrity Journal online

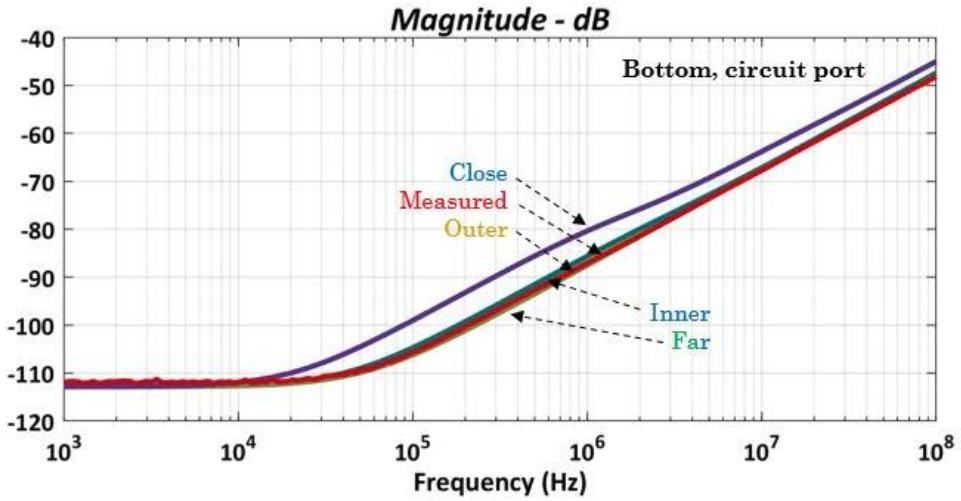
Full-Wave Solver Simulations





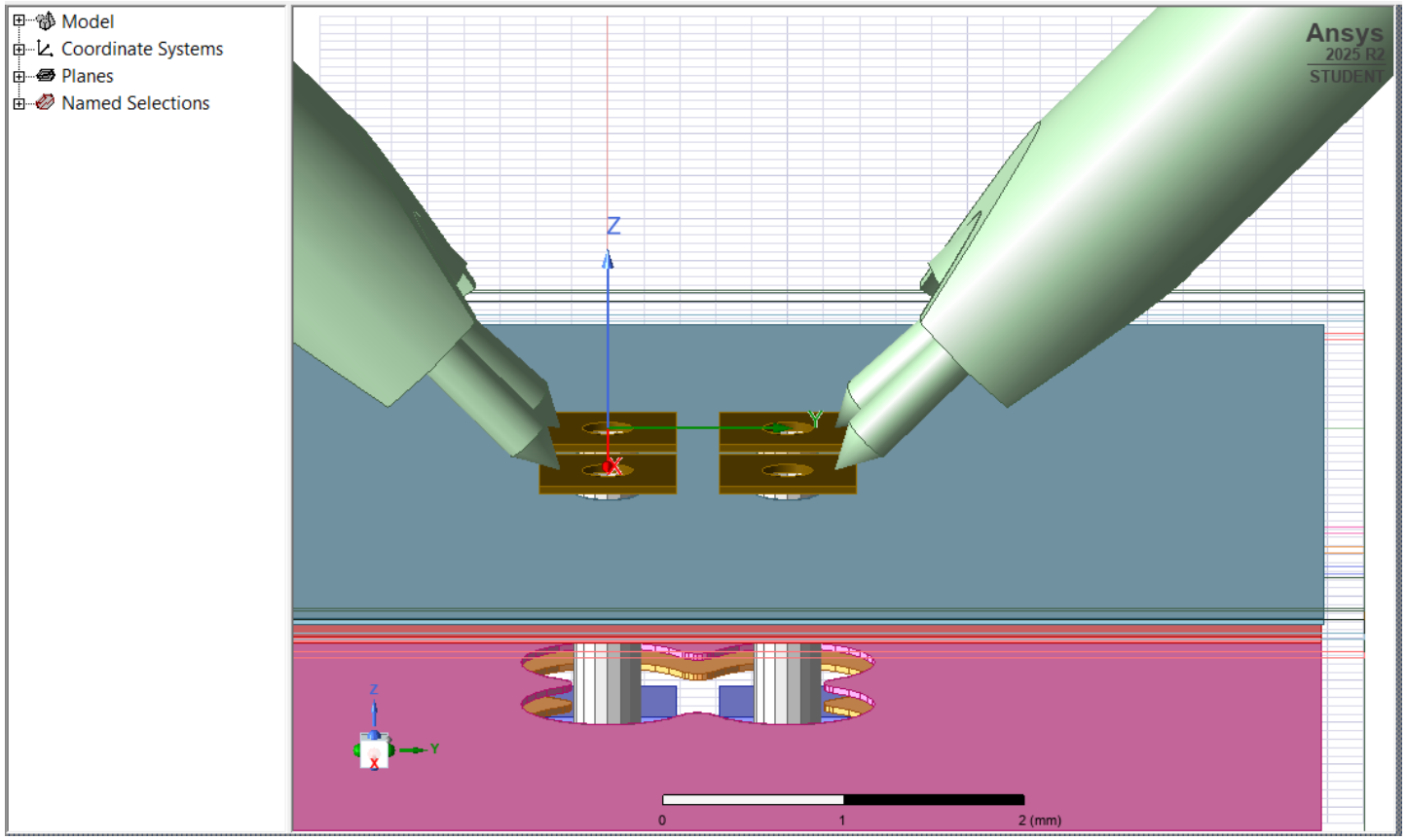
Best match with probe model included. Positioning still matters





Circuit port does not capture probe tip coupling

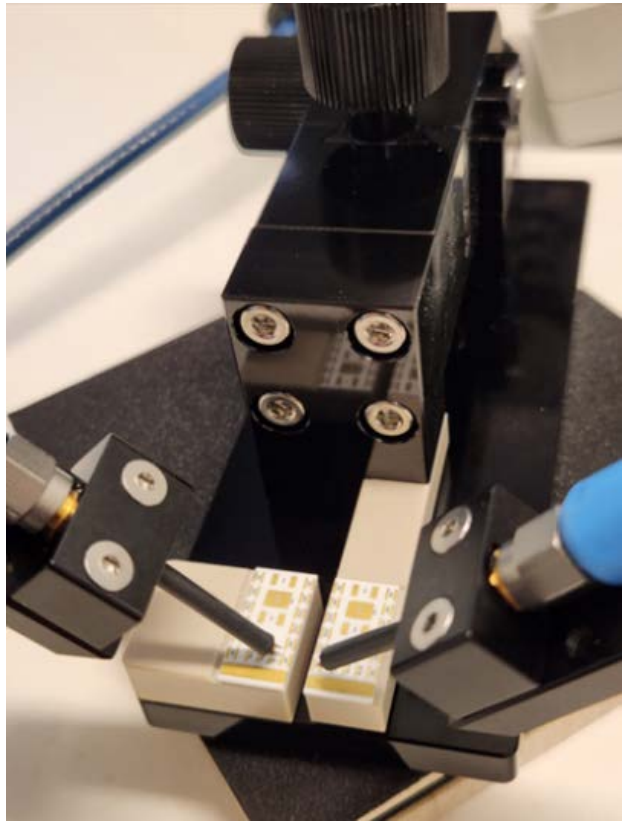
Full-Wave Solver Simulations

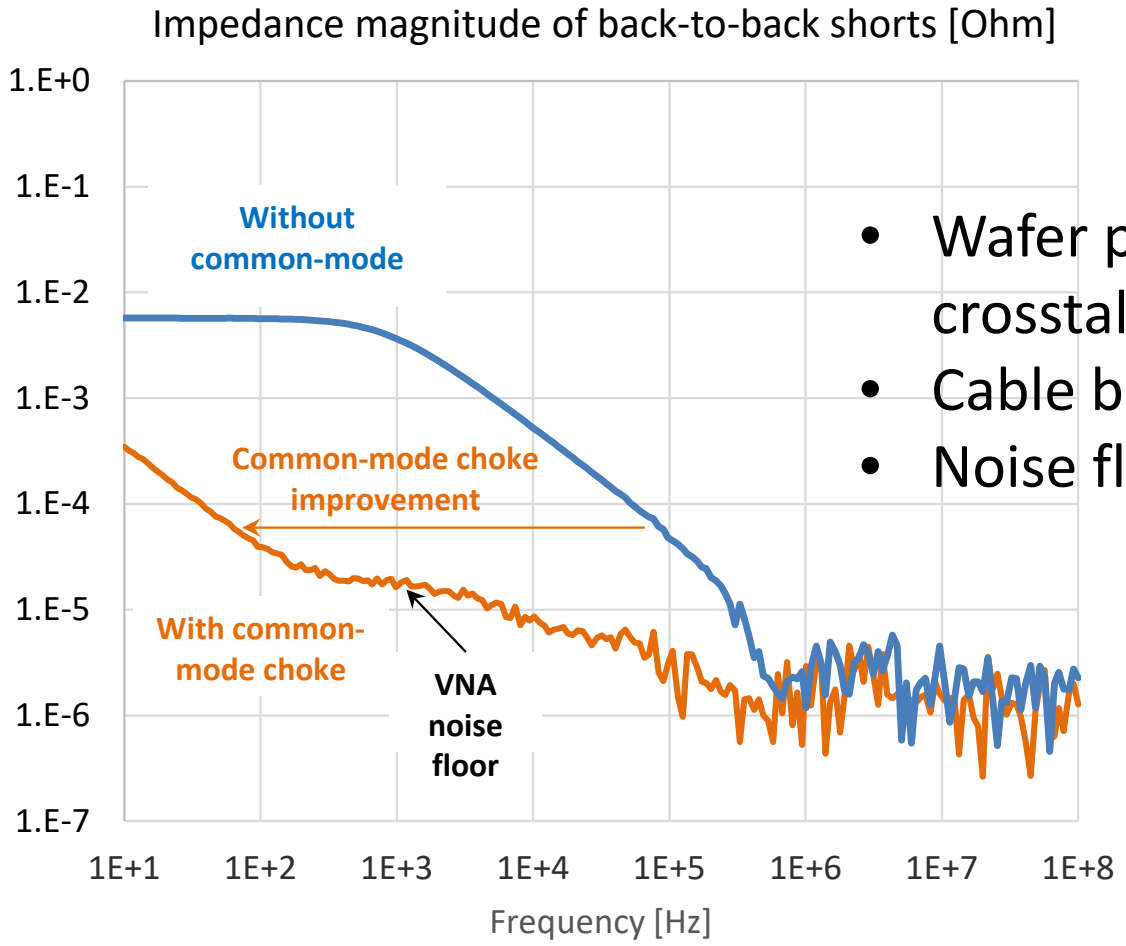


- Capturing probe tip coupling requires 3D model of probe
- Large number of permutations for probe landing coordinates and contact area

Ajay Thumma, “Power Integrity Correlation Results for IEEE TC-EDMS Benchmark Problem 5,” submitted to Signal Integrity Journal online

Measurement Challenges

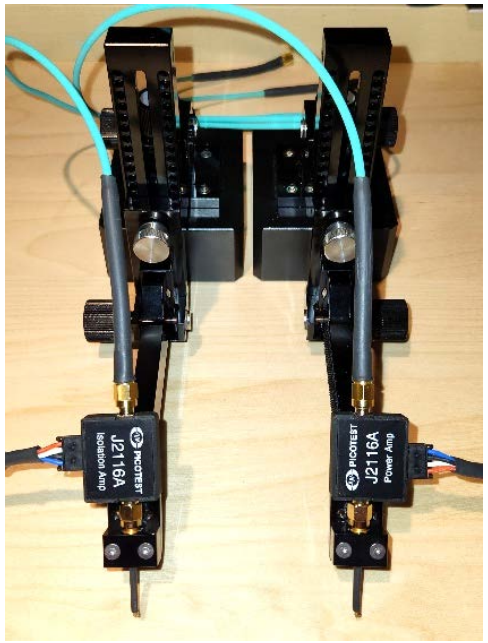


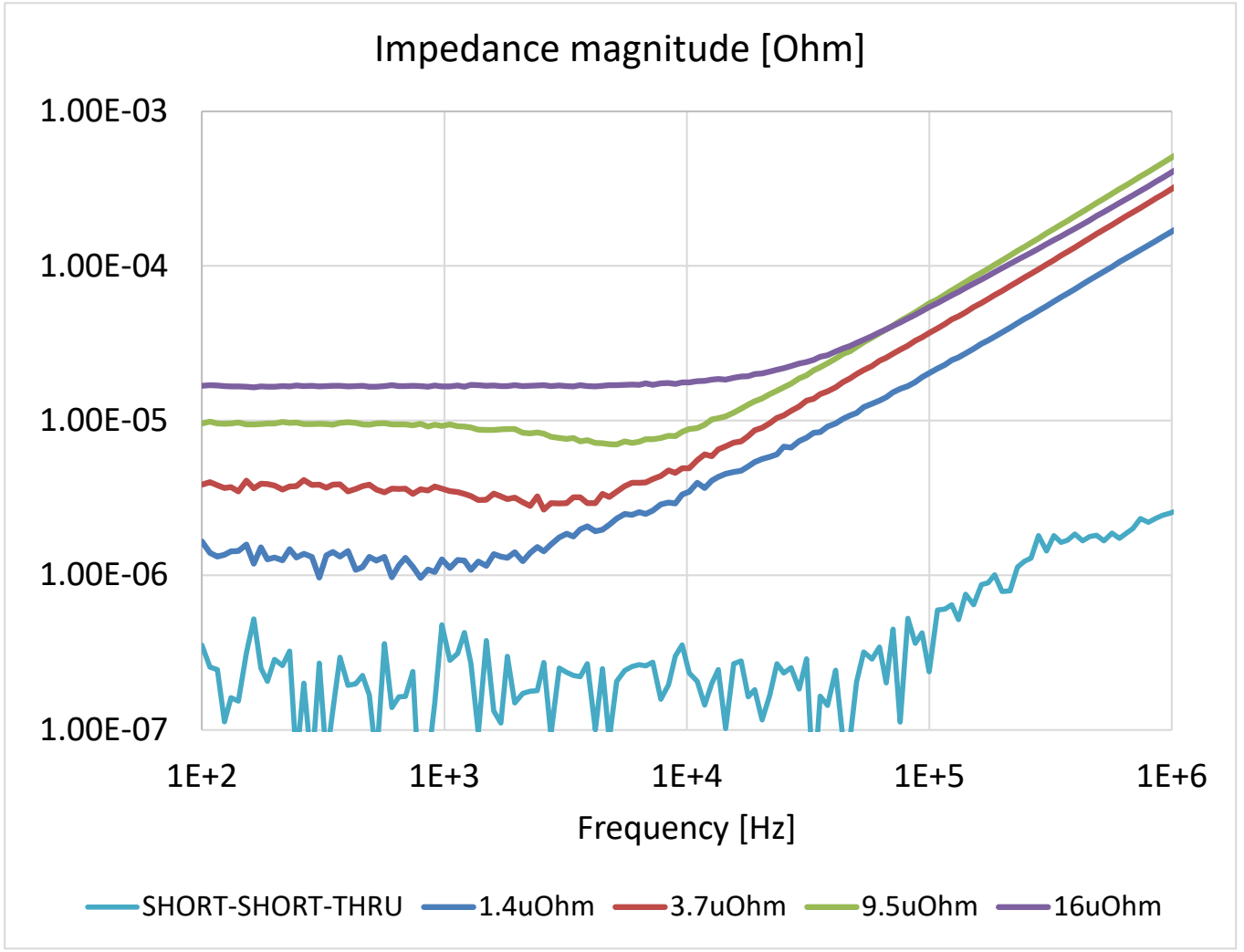


- Wafer probe calibration crosstalk
- Cable braid loop error
- Noise floor

Noise Floor

- 1Hz IFBW
- 0dBm source power
- No averaging
- SOLT calibration (including Isolation)
- 20dB 20dBm power booster on Port1
- 20dB low-noise pre-amplifier on Port2





Summary, Conclusions

- We have shown a versatile open-source PI reference board
- Simple, easy to reproduce
- Offers multiple PI connectivity options
- Challenges to study both in simulation and measurement
  - Impact of solver choice on accuracy
  - Port definitions
  - Calibrations
  - Probe coupling (size, position, orientation of probe loops)
  - Probe de-embedding, including probe-to-probe crosstalk
  - Impact of PCB manufacturing tolerances
- The author invites fellow practitioners from the industry to look at this benchmark challenge and share their results

Acknowledgements

Special thanks go to

- The team members (Shirin Farrahi, Kristoffer Skytte, John Phillips, Gustavo Blando, Mario Rotigni) for their contribution to the board design, layout, and early publications
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- Heidi Barnes of Keysight and Michael Hill of Intel for their measurement support in the three-lab comparison
- Michael Hill of Intel for his editorial support of the IEEE benchmark challenge document
- The IEEE TC-EDMS for their review and comments on the document

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THANK YOU!