Wideband RF launches:
Much more than footprints on PCBs

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As the demand for higher frequencies and wider bandwidths continue their relentless march upward, RF connectors need to keep up with, or even exceed device bandwidth demands. Mating the RF connector to a PCB or substrate requires careful consideration of several factors to get the full performance out of the connector. This white paper provides an understanding of what makes successful launches work. It covers design guidelines and an understanding of what knobs to turn to make connector launches perform well as the industry moves toward 100 GHz bandwidths.

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Introduction

There are many types of RF connectors that are used in different applications. The subject is too vast to cover in a single document. For the purposes of this white paper, the focus is on compression mount PCB connectors. A compression mount connector is one which is compressed onto a PCB, using mounting hardware, to make a connection. They can connect to either microstrip or stripline traces in a PCB. With the number of high-speed connections in PCBs increasing continually, compression mount connectors provide a number of advantages to meet this demand:

- They are relatively compact, which means a number of them can be placed on a PCB.
- They can be placed anywhere on a PCB. This allows them to be placed close to the device the signal needs to reach.
- They can be reused.

Instantiating them on a PCB and getting the full bandwidth out of them does require careful design. Just like a race car needs the optimal tires that allow it to obtain sufficient traction to the track, while going as fast as possible, RF PCB connectors need a good launch structure in order to get the widest bandwidth signal transfer into and out of the PCB.

Defining an RF launch

The launch includes the connector, signal via and the via to the trace transition inside the PCB. To accurately gauge the performance of this combination, the tip of the connector and break out region – including a short section of trace (about 2 mm) – all need to be modeled together. An example of this is shown in Figure 1.

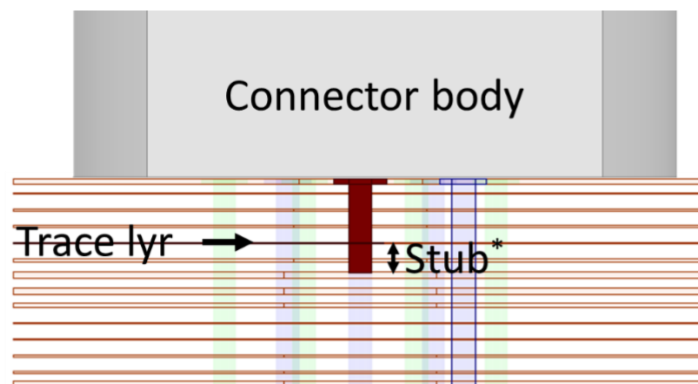

Figure 1: Modeling of the launch with connector tip

RF launch designs are complex structures with no closed form solutions. They consist of many elements that need tuning in an EM solver to deliver maximum performance. The following section identifies some of these key features.

Each of the sub-components shown in Figure 2 represents a degree of freedom in the design of the launch. All these launch elements must be optimized together to get bandwidths of 100 GHz.

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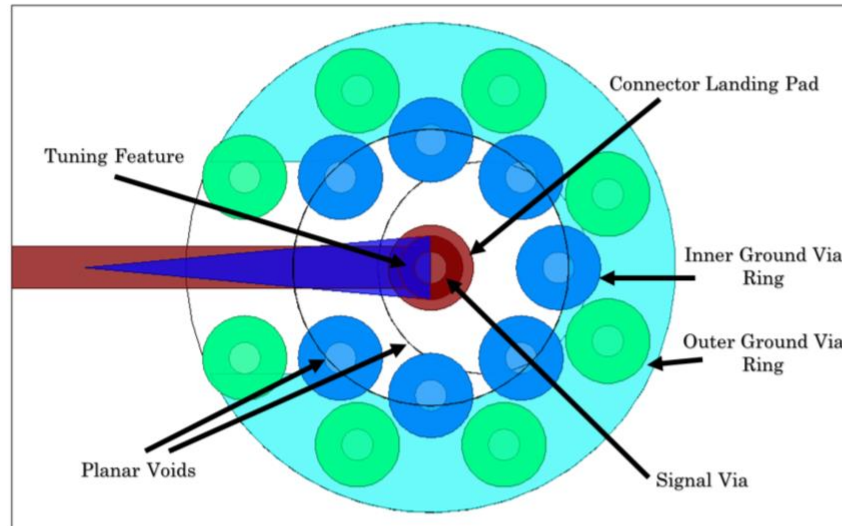

Figure 2: Sub-components of an RF launch

A brief description of the launch sub-components follows.

Connector: As stated previously, the connector impacts launch performance and needs to be included when modeling the structure. The transition between PCB and connector tip has complex interactions requiring tuning, including contributions from both sides to achieve highest performance.

Connector Landing Pad: The landing pad size is dictated by the mechanical constraints of the connector. It needs to be large enough to provide a reliable connection by accounting for manufacturing variations of connector and PCB fabrication, but small enough to allow for designs using the connector to achieve the desired performance level.

Signal Via: Electrically speaking, for a via, the drill hole size is the dimension that matters, not the finished hole size. Having a list of common drill sizes used by the PCB vendor is very useful while trying to tune via launches.

The drill size determines the minimum pad size of the via on the inner layers. The smaller the minimum pad size is, the better the performance of the via. Laser drilled microvias, due to improved registration, can accommodate very small pad sizes with an annular ring as little as 2 mils with a L1:L2 transition (pad diameter = drill diameter + 2x annular ring). For deeper microvias, the drill size and annular ring needs to increase in size.

Tuning Feature: Used to equalize the impedance from via pad/void region to the trace.

Planes, Voids and Ground Collar: The ground planes under the launch tie the ground rings together. Voids in the planes allow the tuning of the impedance seen by the signal as it travels down the via. When possible, it is best to create a "ground feature" on power planes and

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signal layers. This ensures adequate metal coverage along the via, improving the quasi-coaxial structure of the launch and performance.

Ground Rings Inner/Outer: There are 2 rings of ground vias. The inner ring has a strong impact on the impedance of the transition and cutoff frequency. The second ground ring helps seal the gaps between the vias of the inner ground ring which limits crosstalk to adjacent transitions. The performance of the launch is heavily dependent on the ground rings.

Tuning the different sub-components to obtain a wide bandwidth launch requires balancing several competing constraints. In the following sections, 4 key area of focus are detailed. They are:

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Section 1: Impact of via stubs

Key section takeaways

- >8 mil via stub will hinder getting > ~ 60 GHz launch bandwidth
- Fab limits on stub length AND length tolerance will determine launch limits
- Designing in compensation for longest stub will make things bad for shortest stub length. Tight tolerance is key for wide bandwidth!

When using a through via to transition to an internal layer, there is a stub created by the part of the via that extends below the transition layer. The higher the bandwidth goal, the more this stub impacts the performance. The impact of the stub is the worst at a frequency where the stub length equals ¼ of the wavelength [1]

$$f_0 \approx \frac{c}{4\,(Stub\ length)\sqrt{\varepsilon_R}} \quad \text{Equation 1}$$

Where,

f_0 = Frequency where the stub = ¼ wavelength [Hz]

c = Speed of light in vacuum [in/s]

Stub length = Length of stub [in]

ε_R = Dielectric constant seen by the via

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While f_0 is the frequency at which the impact is most prominent, well before this frequency the via stub starts to degrade the performance of the via transition because it adds additional capacitance to the launch.

A common strategy used to minimize the impact of the via stub is to backdrill most of the stub away. In the backdrilling process, the PCB fabricator drills out the via stub from the side opposite the connector launch. No manufacturing process is perfect, however. The backdrill cannot get close to the signal launch layer for fear of damaging the contact between the via and trace. Therefore, there is always a residual stub left behind after the backdrilling process. There is also a tolerance associated with the leftover stub length. For example, a PCB fabricator might say the leftover stub length can be 8mil ± 4mil. A backdrilled via in this case can be left with a stub that is anywhere between 4 and 12 mils long! That is quite a large range! To be fair, this is a conservative example of stub length variation. It is possible to get smaller stubs in many cases.

To illustrate the need to push for the smallest stub length, look at the curves shown in Figure 3. There are 16 curves in the graph, one each corresponding to a stub length between 0 and 15 mils. The smaller the stub length, the better the return loss is across the frequency band. To visualize the bandwidth impact better, the frequency at which the return loss crosses the 15 dB level (VSWR = 1.4) is plotted in Figure 4. There are 2 main points to notice about the shape of the curve: (i) the curve is not linear, with longer stub lengths causing a rapid drop off in the bandwidth of the via transition and (ii) for small stub lengths the reduction in bandwidth is not significant. Hence, pushing for a small residual stub and a tight tolerance provides significant benefit not only from the point of view of increasing the operating bandwidth of the launch but also from the point of view of all launches on the board behaving similarly to one another.

So far, we have only been looking at the impact of a single stub. Every internal trace has at least 2 stubs – one at the launch and the other at the device side. So, any performance degradation introduced by the stub is going to be magnified by the reflections that will setup between the stubs at either end of the trace. This is depicted in Figure 5. For each of the three stub lengths depicted in the figure, the return loss impact of reflections bouncing between two via launches at either end of the 3 inch long, low loss trace are shown in solid lines. The comparative performance of a single launch is shown by the dashed line, and in every case is significantly better than the double via case.

Ideally, the best mitigation strategy against via stubs is to go with laser vias that have no stub at all. If however, backdrilled vias must be used, it is possible to compensate for the capacitance introduced by the stub to a limited extent in the design of the launch. In designing the compensation structure, it might be tempting to compensate for the worst-case stub length. This, however, can still result in poor performance, if the stub tolerance is large. To clarify this, look at Figure 6. Here a tolerance of 4 mils on the 6 mil nominal stub is assumed. The launch compensation is designed to provide the best impedance match for the worst-case stub length of 10 mils. Thus, for a 10 mil stub, the impedance of the launch is within 1 Ohm of nominal. The problem arises for vias with the stub length at the other end of the tolerance (2 mils). For this stub length, the launch looks quite inductive. Keep in mind that every stub in the board need not

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have the same length. The ±4mil tolerance can result in some vias looking inductive and others not, perhaps even when they are adjacent launches.

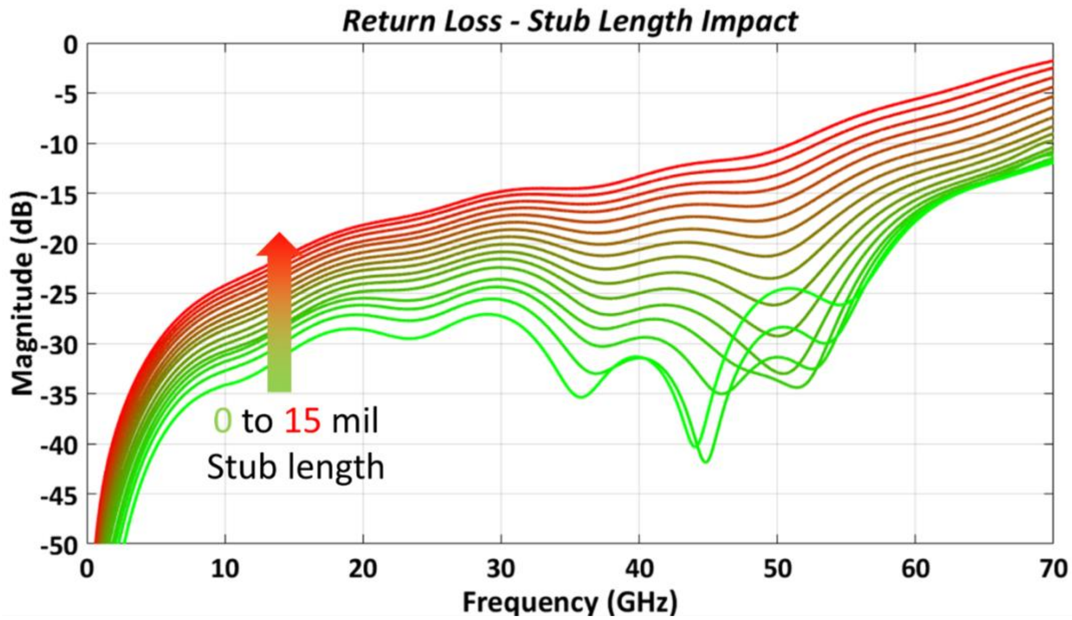

Figure 3: Via stub length impact on return loss

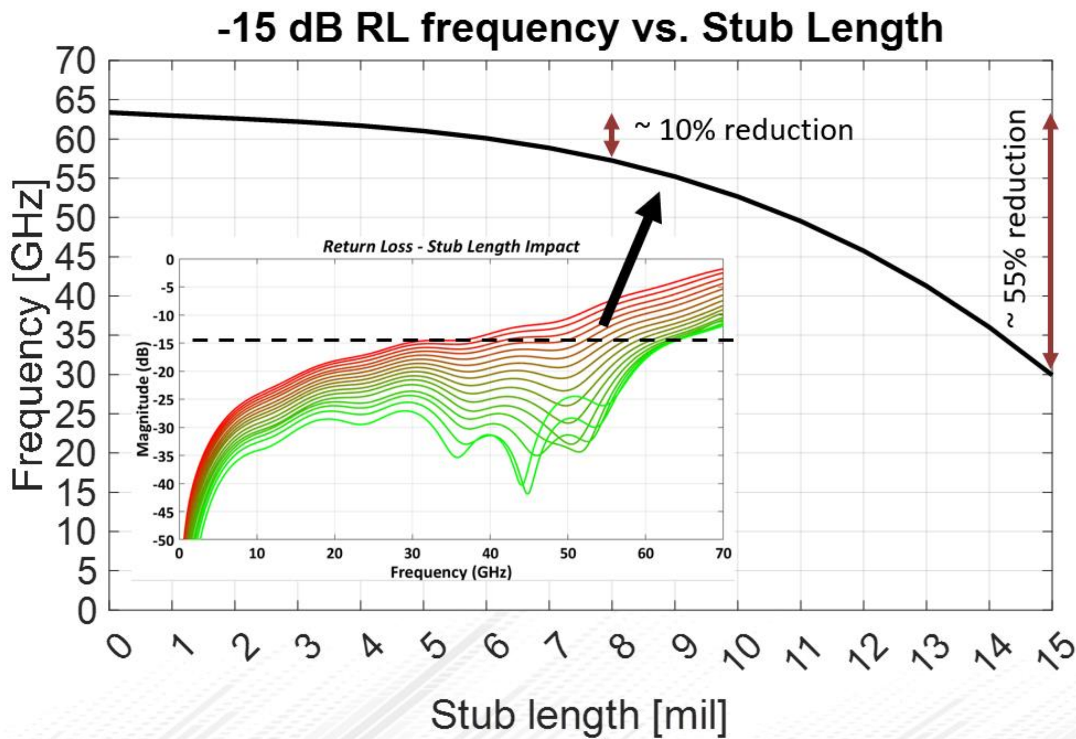

Figure 4: Bandwidth impact of via stubs of different lengths

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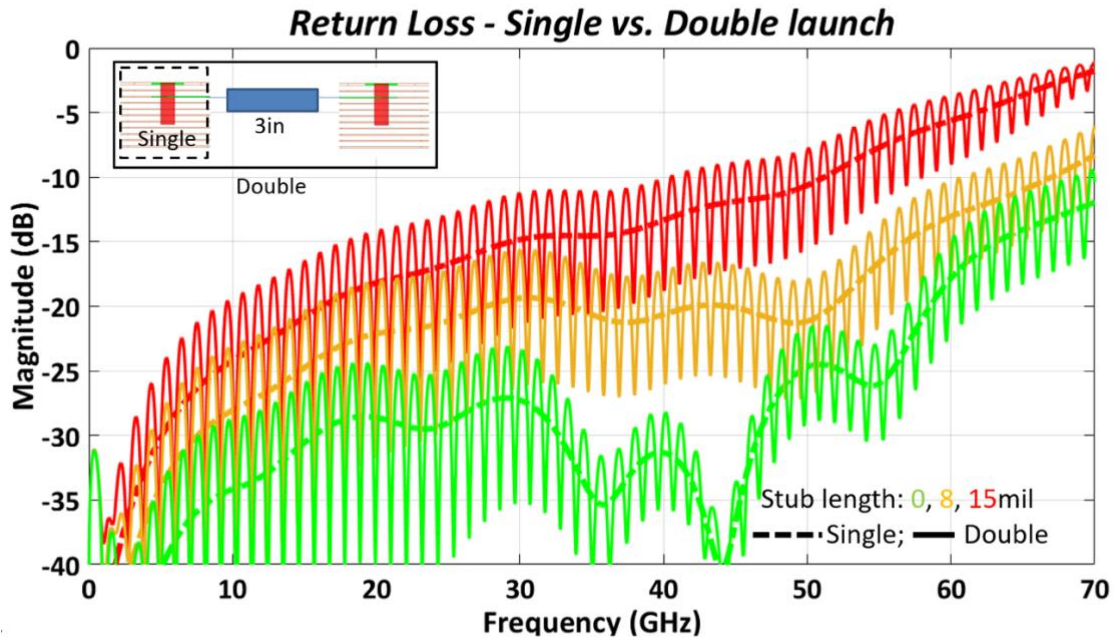

Figure 5: Multiple reflections between via stubs at either end of a trace magnify any performance limitations introduced by the via stub

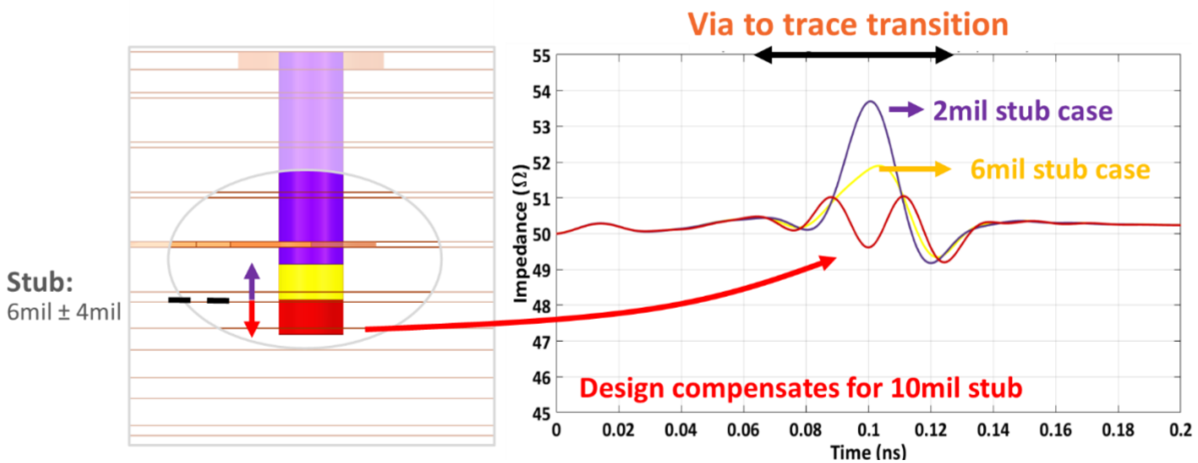

Figure 6: Impact of stub tolerance on compensation design

Section 2: Correct ground ring sizing

Key section takeaways

- When designing RF launches with bandwidths >70 GHz, choosing dielectrics with ε_R<3 and drill diameter ≤ 5 mil is likely necessary for good performance.
- Loss factor is a good metric to see when a launch is no longer behaving as designed.

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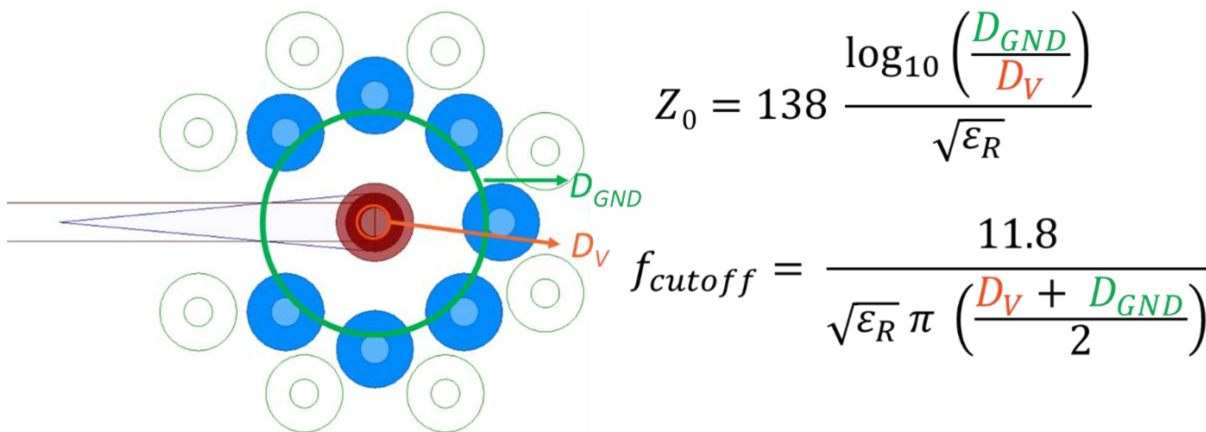
The inner ground ring has a strong influence on the performance of the launch. There are 2 main factors that determine the diameter of the inner GND via ring [2]:

(i) The impedance of the launch area.
Figure 7 shows that the impedance of the launch area can be determined, to the first order, by treating the signal drill size as the center conductor diameter of a coax and the inner GND ring diameter as the shield diameter of a coax. For long vias, the nominal system impedance (e.g.: 50 Ohms) can be used as the target impedance. Short vias however, are strongly impacted by the capacitive loading caused by the interaction between the launch and the end of the connector body. For this reason, a higher target Z_0, like 70 Ohms, is better. That way the average effect of the connector + launch via is closer to 50 Ohms.

(ii) The cutoff frequency of the higher order modes supported by the launch.
Normally, in a launch for a coaxial RF connector, we want only the fundamental mode to propagate. This is the transverse electromagnetic mode (TEM). Above a certain frequency, called the cutoff frequency, the launch can support higher order modes. When this happens, energy is spread among the different modes and since the different modes propagate differently, the signal gets distorted quickly. To prevent this, the launch needs to be designed so the cutoff frequency lies outside the bandwidth of interest. Figure 7 shows that the cutoff frequency is inversely proportional to both the size of the GND ring and the dielectric constant seen when traveling down the via. The higher these numbers are, the lower the cutoff frequency and the lower the operating bandwidth of the launch. The formula for f_{cutoff} in Figure *7* provides the cutoff frequency in GHz when the diameters (D_v, D_{GND}) are given in inches.



$$Z_0 = 138 \frac{\log_{10}\left(\frac{D_{GND}}{D_V}\right)}{\sqrt{\varepsilon_R}}$$

$$f_{cutoff} = \frac{11.8}{\sqrt{\varepsilon_R}\,\pi\left(\frac{D_V + D_{GND}}{2}\right)}$$

Figure 7: Equations to help with sizing the inner GND ring

Both the impedance and the cutoff frequency are also inversely proportional to the dielectric constant (ε_R) seen by the signal as it travels down the via. It is important to note that this ε_R need not match the value seen by the trace. The reason is PCBs comprise of laminates bonded together. The laminates are composites and consist of glass fiber and resin. Take a look at Figure 8. It shows a cross-sectional

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picture of a PCB. There are both core layers and pre-preg layers, each consisting of layers of glass cloth and resin. Since each of these layers has different dielectric properties, the effective dielectric constant seen by the signal depends on the direction in which it is traveling. PCBs in other words are anisotropic as far as dielectric constant is concerned [3]. The higher the anisotropy, the greater the difference in dielectric constant seen by the via as compared to the trace.

To achieve high bandwidth launches, the dielectric constant of both the resin and the glass should be low and equal. This ensures the lowest possible dielectric constant around the via and therefore, the highest cutoff frequency. The table in Figure 9 [2] shows that to reach cutoff frequencies of >90 GHz, signal drill diameters of <5mils and dielectric constants of <3.1 are needed. The values in Figure 9 can serve as a useful starting point in guiding the design of an RF launch.

From Figure 9 it is possible to understand mathematically why the performance of the launch quickly degrades around the cutoff frequency, as seen in

Figure *10*. To get a physical explanation of what is happening, refer to Figure 11. Here the physical structure of the launch via and the surrounding GND vias is shown on the left side of the figure. The portion of the vias colored in green represents the portion that we want the signal energy to travel in. Since the GND vias are through vias however, they continue below the reference layer of the trace to form waveguide structures below the signal reference layers. To visualize this better, a conceptual schematic is shown on the right half of Figure 11.

The right half of Figure 11 shows that the connector launches the energy into the coaxial portion of the launch and then the signal energy propagates down a stripline. However, below the trace reference layer, the GND vias form a circular waveguide under the signal via. There are also several rectangular vias formed by the plane layers and stitching GND vias under the trace reference layer. The circular waveguide and rectangular waveguides under the trace are non-TEM structures. That means they cannot propagate energy below f_{cutoff}.

With this understanding, let us look at how energy flows in the launch at different frequencies. Shown in Figure 12 are the electric field patterns in the launch below f_{cutoff} (on the left half) and above f_{cutoff} (on the right half). Below f_{cutoff}, the energy stays contained withing the stripline layers and the circular waveguide below the signal via cannot propagate energy. This is exactly what we want to happen. Above f_{cutoff} though, the circular waveguide can now propagate energy and remove energy from the TEM mode traveling down the stripline and sends a portion of it through the rectangular cavities below the trace reference layer. This is an undesirable situation because the energy can spread through the plane cavities to other parts of the board and cause crosstalk, radiation, and other undesirable effects. Staying below f_{cutoff} therefore, has utmost importance in obtaining a high performance, wide bandwidth launch. An animation of the field plots is available at https://blog.samtec.com/wideband-rf-launches/#verify

While the field plots shown in Figure 12 aid greatly in understanding the physical effects causing poor performance, computing the field plots is computationally quite intensive and takes significant time. There is a faster way to see if the launch performance is being adversely impacted by allowing the propagation of higher order modes. Figure 13 shows a metric called the loss factor. Loss factor is a measure of the amount of energy not reaching any of the ports of the structure. For a 2 port structure, for example, $|S_{11}|^2 + |S_{21}|^2$ is the total energy flowing through port 1. This energy gets either transmitted to port 2 ($|S_{21}|^2$), or reflected to port 1 ($|S_{11}|^2$). Loss factor, in this case, is then $1 – (|S_{11}|^2 + |S_{21}|^2)$. Figure 13 shows that below f_{cutoff} the energy loss increases gradually and corresponds to the energy lost in copper

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and dielectric losses. Above f_{cutoff} however, the loss factor increases rapidly. This is an indicator that higher order modes are carrying energy to other parts of the structure and the launch is no longer performing as desired.

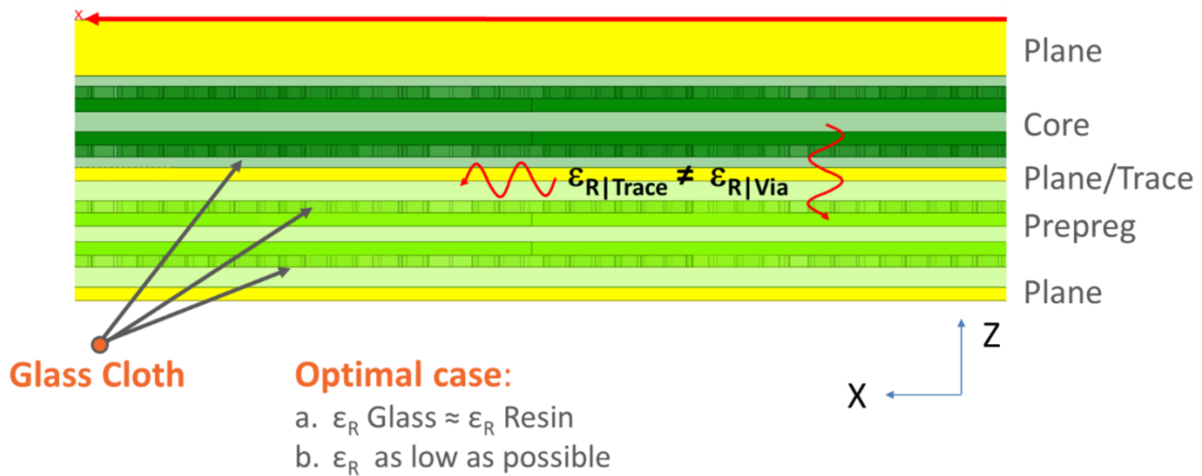

Figure 8: Dielectric constant in PCBs is direction dependent

Drill diameter [mil]	Er						
	2.50	2.75	3.00	3.25	3.50	3.75	4.00
3	201	176	156	138	124	111	100
4	151	132	117	104	93	83	75
5	120	106	93	83	74	67	60
6	100	88	78	69	62	56	50
7	86	76	67	59	53	48	43
8	75	66	58	52	46	42	38

f_{cutoff} in GHz

Figure 9: Higher order modes cutoff frequency as a function of drill diameter and ε_R

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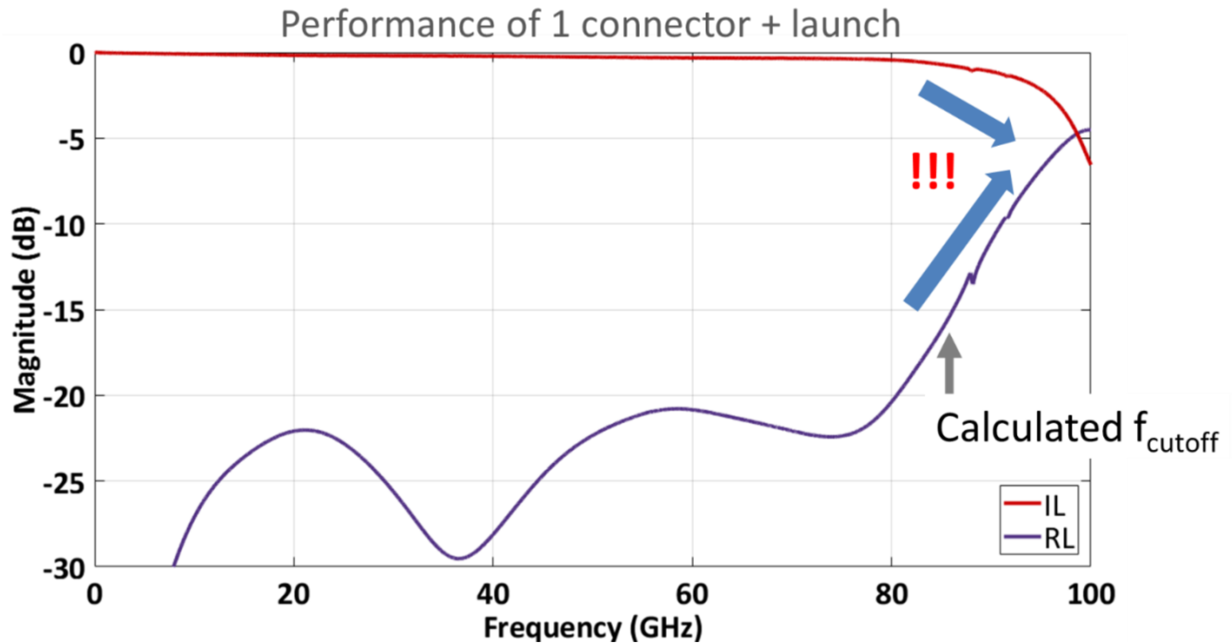

Figure 10: Rapid degradation in performance near and past cutoff frequency of a launch

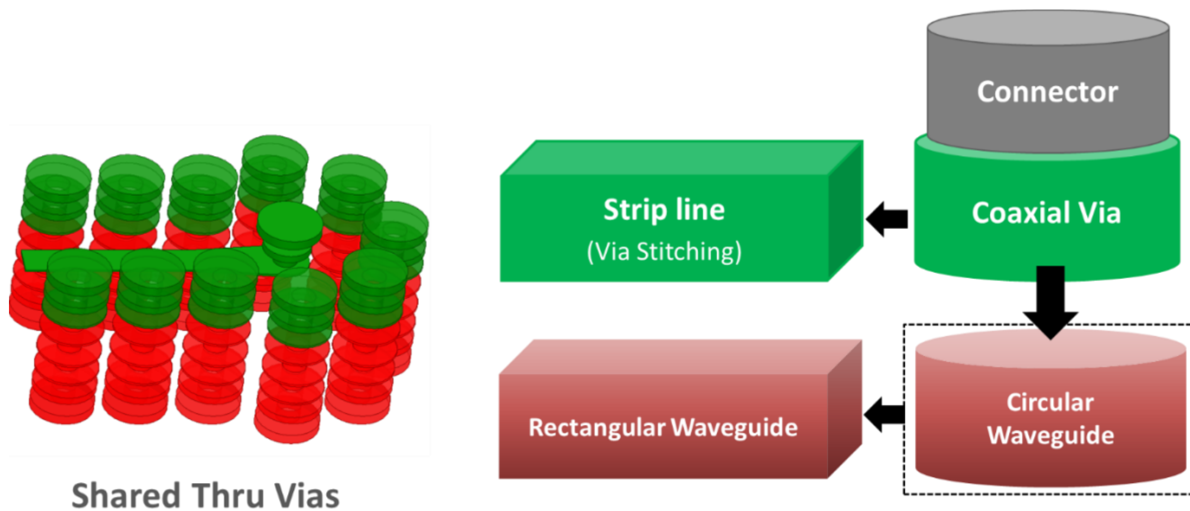

Figure 11: Physical structure of signal and GND vias of a launch (left) and conceptual drawing of the different physical parts of the launch structure (right)

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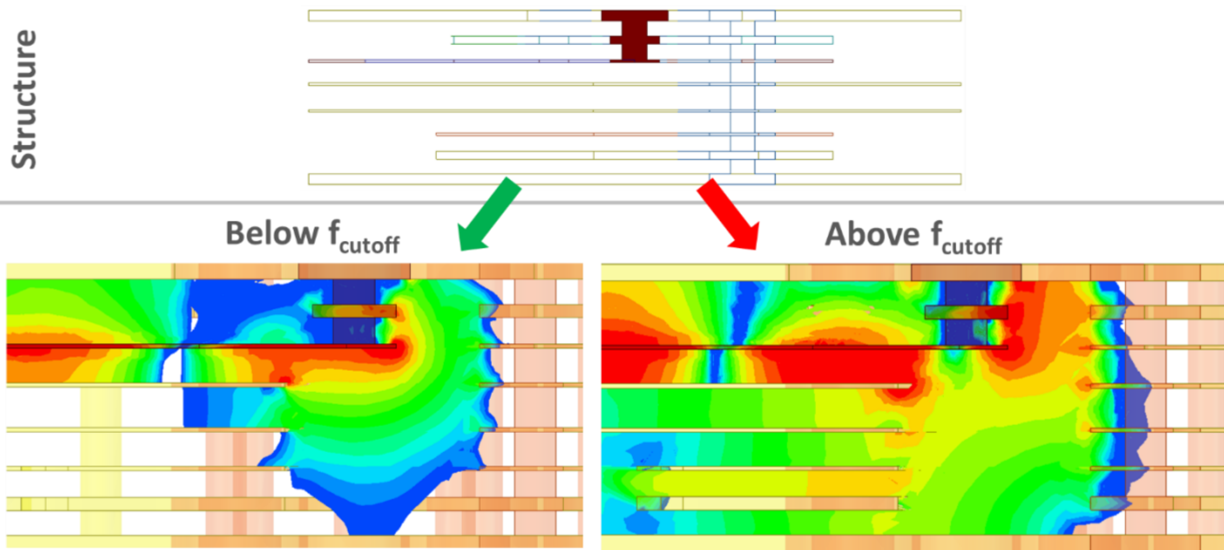

Figure 12: Electric field patterns in launch area below and above cutoff frequency

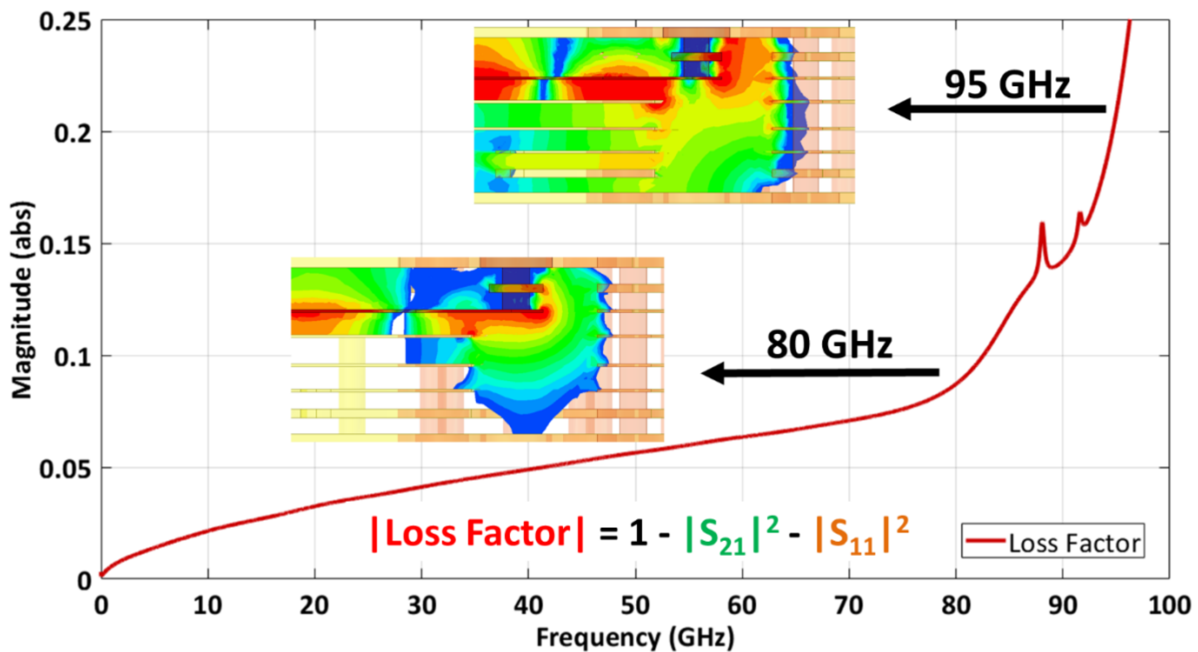

Figure 13: Plot of loss factor allows determination of whether launch performance is being impacted by higher order modes

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Section 3: Misregistration compensation

Key section takeaways

- A tapered transformation from via to trace lowers impact of via to etch misregistration
- Minimize launch asymmetry between channels to minimize differences in performance

Misregistration refers to the fact that all the internal layers and the outer layers of the PCB are not perfectly aligned with each other. Figure 14 [4] shows an example of this. Here the inner layer is offset by 3.5 mils from where we would expect. When designing launches for wide bandwidth, shifts of this order can result in the structure behaving quite differently than what it was designed to do.

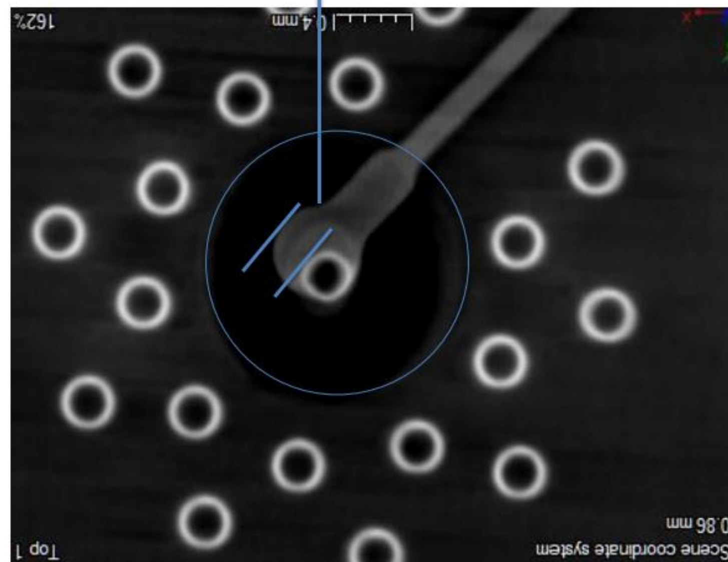

Figure 14: CT image showing misregistration of the inner layer with respect to the top layer

There are a couple of aspects to consider here. The first is that the exact amount of misregistration is hard to quantify ahead of time. The second aspect is that the misregistration can have a directional impact on measured results. Figure 15a, for example, shows a TDR of the two legs of a diff pair. The leg shown in blue clearly has an inductive spike that is caused by the clearances on the reference planes of the trace being shifted with respect to the via-to-trace tuning feature.

To better understand this let us look at parts b and c of Figure 15. Figure 15b shows a photograph of the PCB, while Figure 15c shows a CT image of the same board. At each of the connector locations in Figure 15a, there are two arrows shown. One is in red, the other in blue. The red arrow indicates the direction in which the misregistration happened. The blue arrow

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shows the direction in which the differential trace launches under the connector. In this particular example, the trace launch direction in some cases is parallel to the direction of misregistration, while in other cases it is perpendicular to the direction of misregistration. The CT image in Figure 15c shows the direction of misregistration in red and four traces that launch from under the connector in comparison to the misregistration direction. Comparing the TDR in Figure 15 with both the photograph and the CT images, what becomes clear is that when the misregistration is parallel to the direction of the trace exit, the impact on the TDR is much more than when it is perpendicular to it. The underlying reason is that the size of the antipad and the shape of the via to trace transition are tuned relative to each other. When the antipad on the reference plane moves, the impedance seen by the signal in the via-to-trace transition is impacted much stronger than when the misregistration is perpendicular to the direction of the trace launch. Figure *15* quantifies this effect.

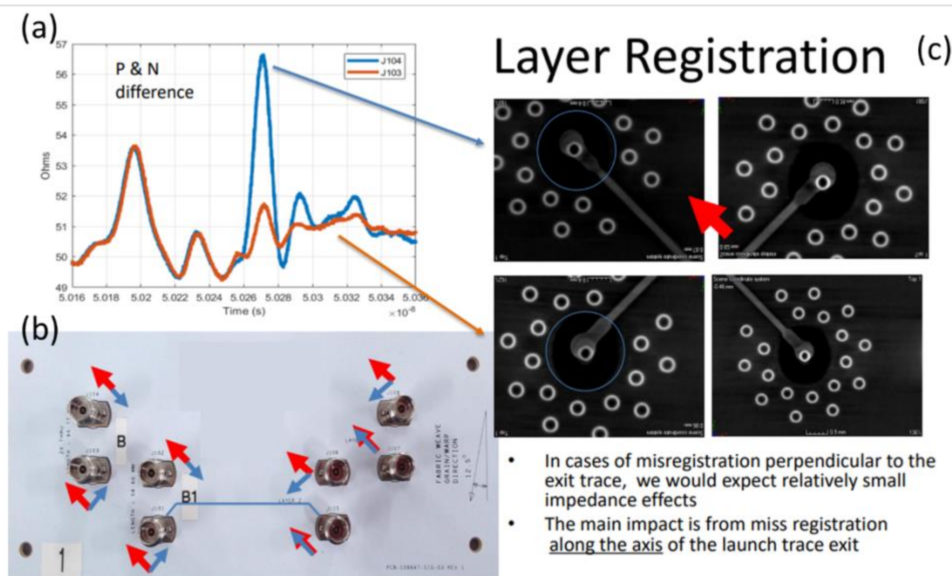

Figure 15: Impact of layer misregistration on connector launches

In Figure 16a, the TDR for a number of traces which launch parallel to the direction of misregistration is plotted. Figure 16b on the other hand, shows the TDR of traces that launch perpendicular to the direction of misregistration. Clearly, the variation in the impedance profile of traces launching parallel to the direction of misregistration is significantly greater than the variation seen for trace launches perpendicular to the direction of misregistration. Not only is the difference in impedance between the legs of the diff pair problematic, but the fact that it is inconsistent from one pair to the next or even one side of the diff pair to the other, makes it next to impossible to remove this effect when measuring a device.

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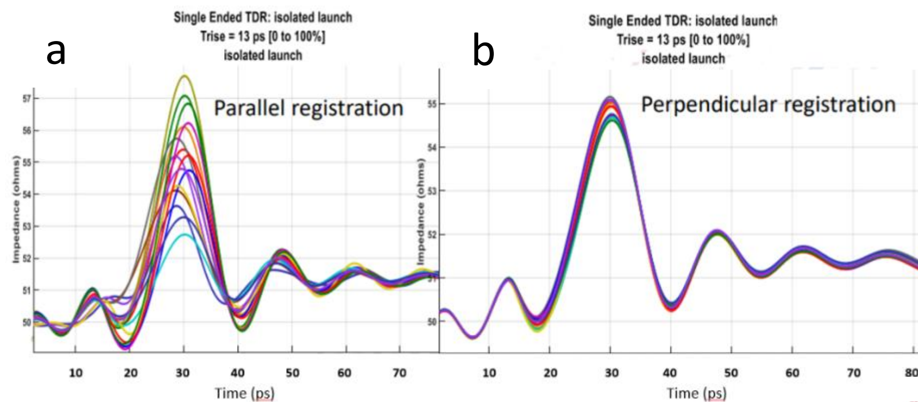

Figure 16: Impact of misregistration is dependent on orientation of trace launch

Having understood the root cause of how misregistration can impact electrical performance, let us look at a couple of mitigation strategies. This is by no means a complete list, other parameters can also be tweaked to reduce manufacturing sensitivity and talking to your PCB fabricator is the best way to understand what all options are on the table.

1. Instead of using a shape that is a rounded rectangle to do the transition from the via to the trace (Figure 17, left), use a tapered transition shape (Figure 17, right). This way, even if there is misregistration of the antipad in the reference layer, the impedance impact will be minimized.

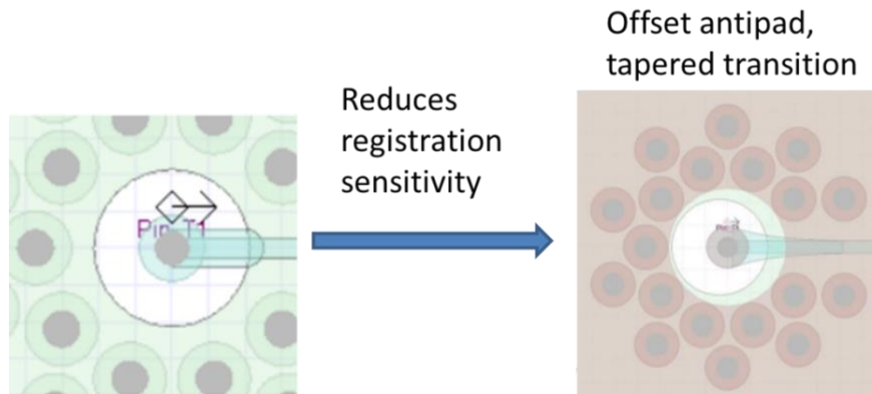

Figure 17: Use a tapered via-to-trace transition to minimize misregistration impact

2. When routing legs of a diff pair or multiple channels of a bus, where we want all the lanes to look as identical to each other as possible, launch all the channels the same way. Figure 18 shows an example of this for a differential pair. Instead of launching the traces at 45° and bringing them together to form a diff pair (Figure 18, left), launch all the lanes parallel to each other (Figure 18, right). Once they have left the connector launch area the traces are brought together to the differential pair spacing.

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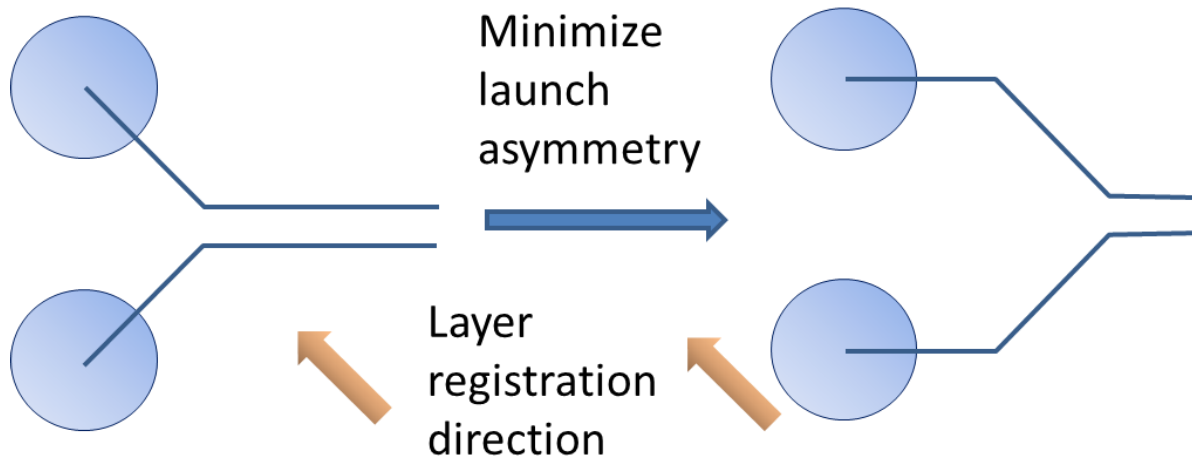

Figure 18: Route channels the same way to minimize difference between them

Section 4: Launch performance issues introduced during connector assembly

Key section takeaways

- Use tight hole size and positional tolerance to ease assembly
- Align to copper features to minimize assembly variations

So far in this white paper issues related to the design and fabrication of the launch have been addressed. Once the PCB has been fabricated, the connectors need to be installed on the PCB. Two main assembly processes used for connectors are solder reflow and compression mount to the PCB, either directly or through some sort of interposer. For this paper, only issues with compression mounting are addressed.

To assemble a compression mount connector, the connector is placed on the PCB without pressing down on the surface. Screws are then fed from the opposite side of the PCB and threaded within screw holes in the foot of the connector. There is usually a torque specification in the connector datasheet for how tight the screws need to be torqued down to ensure good and reliable contact. Care must be taken while tightening the screws to make sure the connector does not move around during the process. If the connector is moved around, it is possible to destroy the landing pad of the connector launch.

Even when care is taken during the assembly of the connector, as the screws are tightened to their final positions, the forces on the connector can cause them to rotate. Figure 19 shows an example of misalignment that can occur due to this rotation.

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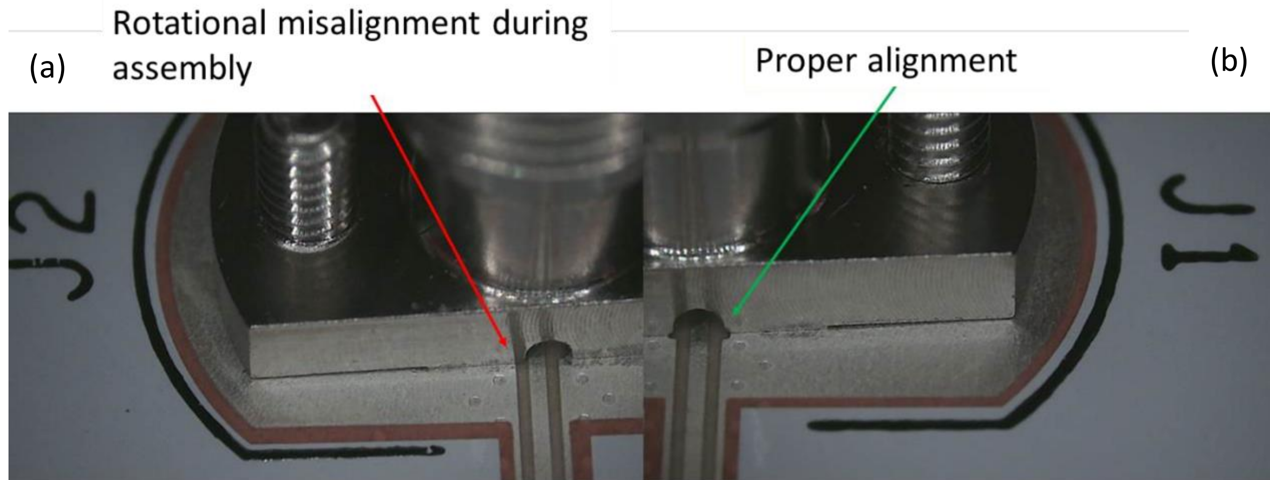

Figure 19: Connector misalignment introduced during assembly

Figure 19a shows that as a result of the connector rotation that occurred during assembly, the connector's ground body is now very close to the surface trace. Figure 19b shows what the properly mounted connector position should look like.

Misalignment of the order shown in Figure 19a will cause a capacitive loading at the launch. Figure 20 shows a 90 GHz bandwidth TDR of the two connector positions shown in Figure 19. It shows an approximately 8 Ohm capacitive dip introduced by the misalignment. Clearly, when working with very wide bandwidths, even small misalignments can have a significant impact on the resulting performance.

One method that can be used to mitigate the risk of tearing off the pad while tightening the connector as well as misalignment during assembly, is to reduce the size of the screw holes used to mount the connector. There is a manufacturing tolerance in the positioning of the screw holes. By keeping this positional tolerance to a minimum and ensuring a tight tolerance for the size of the hole, the ease of assembly of the connectors is greatly simplified. There will be minimal need to move the connector around to get to the proper position. Getting this accuracy, though, involves a couple of additional steps.

As shown in Figure 21 the positional tolerance of the connector mounting holes is specified to be tight. To get a tighter tolerance, the hole drilling is done using an optical inspection step that locates the landing pad of the connector. The drilling positions are then picked based upon this position. That way each connector's mounting holes are drilled with respect to the copper features of that particular location. It is important to constrain the position of the holes in both the X and Y axes. Constraining the position along just the axis joining the mounting hole locations to the center pin location is not sufficient.

A tight tolerance for the size of the screw hole is also specified. This reduces the play in the screw hole, limiting the amount of room available for the screw to move, thus minimizing the chances of connector rotation during the process of tightening the mounting screws.

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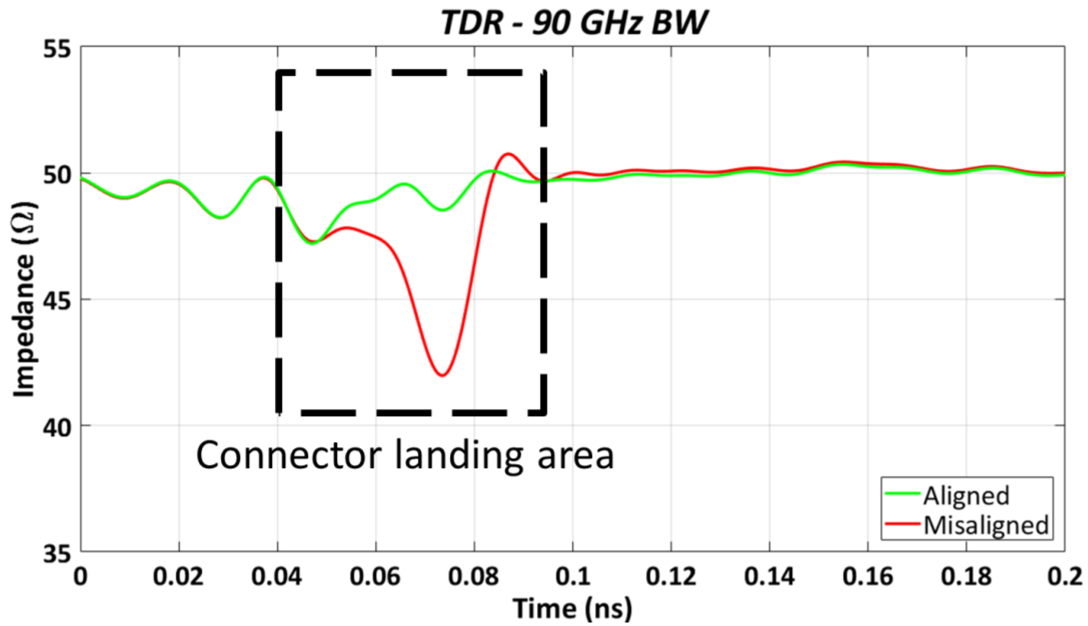

Figure 20: TDR of the connectors shown in Figure 19A, B

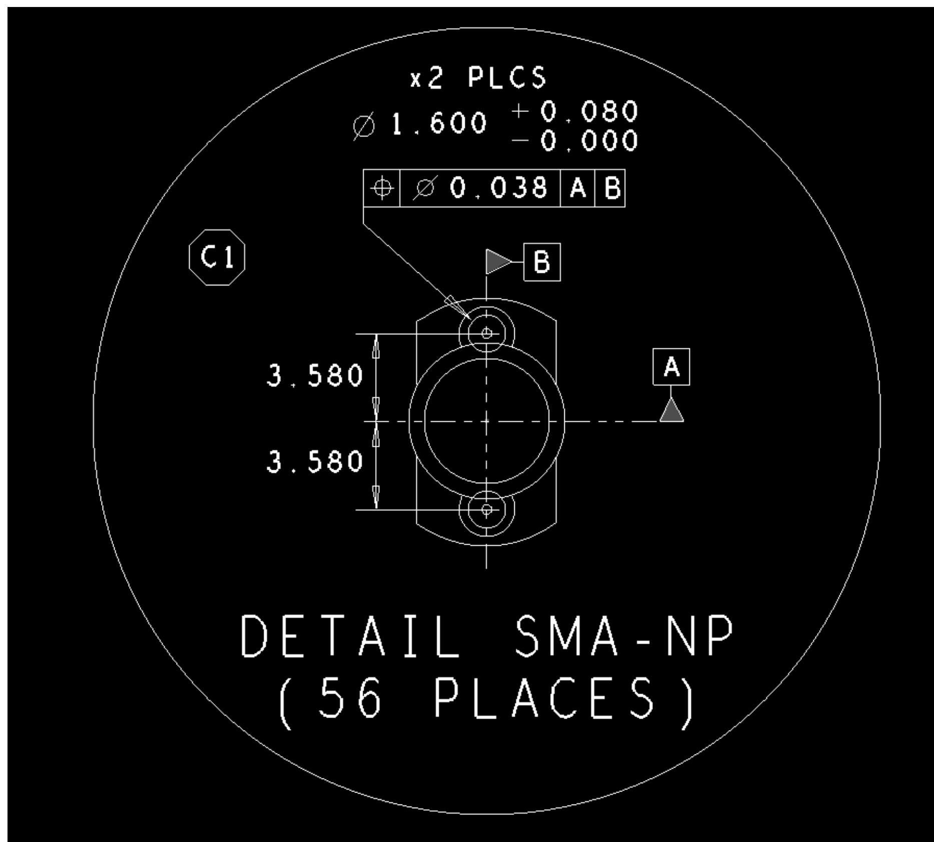

Figure 21: PCB fab drawing callout for connector mounting holes positioning tolerance

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An additional feature of Samtec connectors, that is very useful during the assembly process, are notches that are milled into the foot of compression mount connectors. An example is shown in Figure 22.

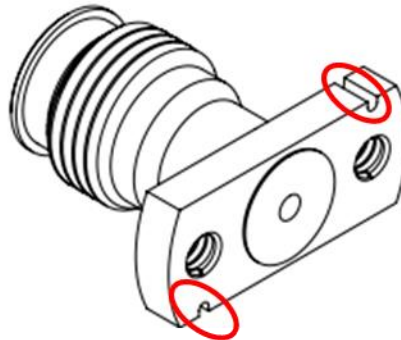

Figure 22: Notches milled in the foot of Samtec's compression mount connector to aid in connector assembly.

If copper features are defined to match the location of these notches, it becomes very easy during assembly to check the positional accuracy of the assembled connectors and make fine adjustments, if needed. This is especially helpful when assembling compression mount connectors that connect only to striplines. In this case there are no doghouse openings in the foot of the connector to verify the positional accuracy of the connector, making the notches invaluable. An additional benefit is that since the notches align to copper features in the PCB, any offset between the mounting hole location and landing pad location is easily noticed. This removes any doubt on whether assembly effects are detrimentally impacting subsequent measurements. An example of a PCB with the footprint having copper defined features is shown in Figure 23a. Figure 23b shows the final result of the assembled connector, whose notches are aligned with the copper features, thus ensuring that the connector center pin is centered on the PCB landing pad.

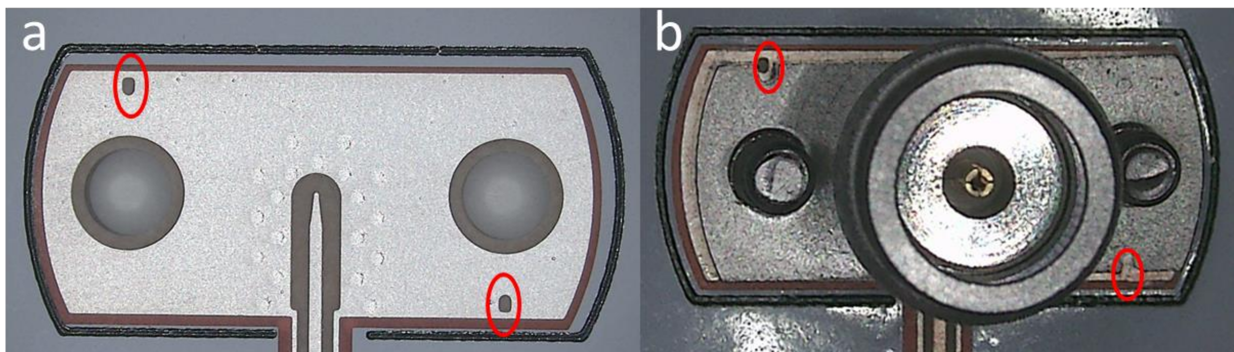

Figure 23: A) PCB with copper defined features for alignment. B) Connector with notches aligned to PCB alignment features

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Conclusion

The purpose of this document is to show that very wide bandwidth RF launches are possible to implement, even with vias included, in PCBs. That does not mean it is trivial. A lot of competing requirements, be they electrical, mechanical, manufacturing or cost, must be considered and balanced simultaneously.

In this white paper, some of the most important design considerations have been elaborated on. Optimizing these factors requires working with your PCB house to understand what the manufacturing limits are. Ultimately, getting to 90-100 GHz bandwidths, is going to, in many cases, require pushing the edge of today's fabrication limits. Understanding the limits at the start of the design process goes a long way toward reaching a high performance launch, which ultimately means high fidelity connections to your device.

To discuss RF Launch and System Optimization contact
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