



SIGNAL INTEGRITY HANDBOOK

Reference for the Selection of High-Performance Interconnects
for Signal Integrity Optimized System Design

SIGNAL INTEGRITY

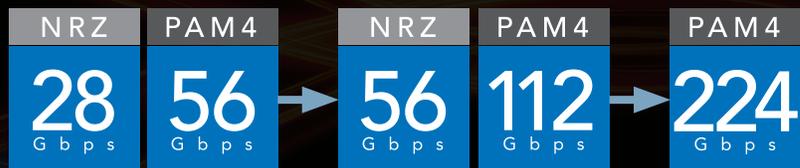
FOR HIGH-PERFORMANCE SYSTEM DESIGN

The 5G/6G Network, High-Performance Computing, Artificial Intelligence and Auto "2.0" industries are driving new architectures that demand previously unimaginable transmission speeds, bandwidths, frequencies and densities - all while balancing scalability, power and thermal management concerns, and of course, cost.



NEXT GENERATION SYSTEM SI CHALLENGES

Interconnect solutions that support bleeding edge speeds are a necessary component of next generation high-performance systems. Those capabilities, however, can be rendered ineffective unless they are part of a well-designed and optimized system. A holistic approach to system design - particularly as speeds, bandwidths and densities increase - is a necessity.



FULL SYSTEM OPTIMIZATION... FROM SILICON-TO-SILICON™

The purpose of this handbook is to provide a reference for those with little or no signal integrity (SI) experience who are tasked with selecting a high-speed interconnect. The information included has been carefully developed by Samtec's industry-leading Signal Integrity Engineers to help facilitate informed decisions when specifying components that will affect a system's signal integrity.

For additional assistance with complex system design challenges, Samtec provides high-level design and engineering support both at the component level and system level - from bare die, to IC package, to PCB, to connectors and cables, and back again. To discuss your specific application, please contact sig@samtec.com or learn more about Samtec's signal integrity capabilities at samtec.com/s2s.

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Signal Integrity Fundamentals

Anytime an electrical signal is transmitted, signal integrity (SI) is a concern. Water circuits are subject to limited flow along the water path. In an analogous manner, electrical circuits are subject to attenuation along the signal path (see **Figure 1**). At its most basic level, SI ensures that a signal is transmitted from "Point A" to "Point B" with sufficient quality (or integrity) to allow effective communication. As a term, SI typically applies to baseband signals that are transmitted using an interconnect, such as a cable, printed circuit board (PCB) trace, or transmission line, and it also applies to broadband applications, such as those operating at RF or microwave and millimeter wave frequencies (see "**Signal Integrity in RF Systems**" p. 21).

i. What is Signal Integrity?

SI needs to be considered throughout the entire system and component design process. Unlike in the past, interconnects can no longer be treated as an afterthought. As rise times get shorter and clock frequencies increase, connectors and cables once considered electrically transparent can have a significant effect on the quality of a system's transmitted signal. Factors such as crosstalk, return loss, insertion loss, and electromagnetic interference (EMI) can all play significant roles in determining what interconnect solution is optimal for a given application. Digital interfaces use one of two types of signaling: single-ended or differential signaling, and each has its own effects on SI.

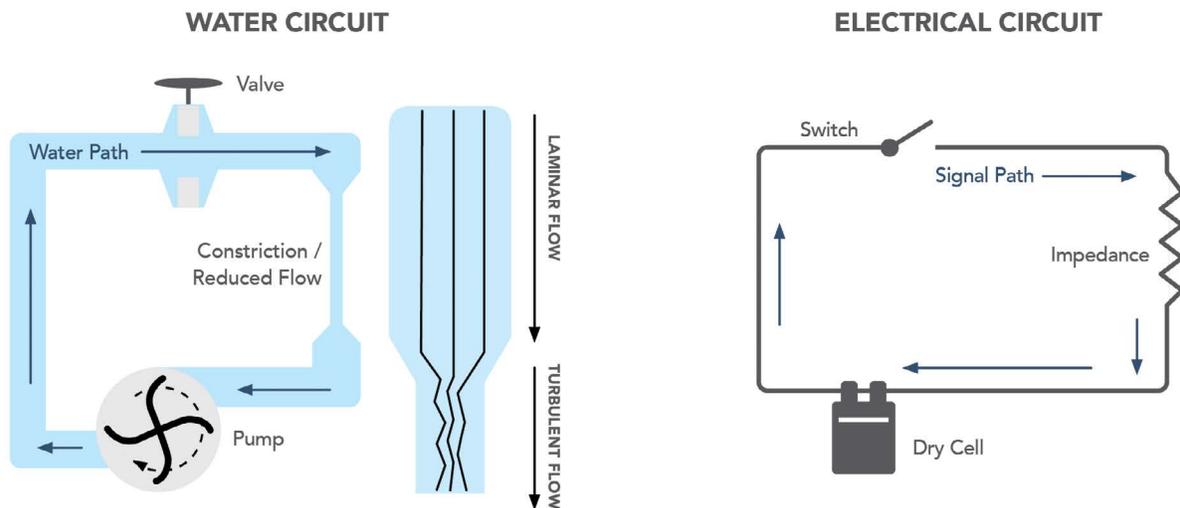


Figure 1. As water circuits are subject to reduced flow along the water path, electrical circuits are subject to attenuation along the signal path.

ii. Single-Ended Signals

Typically used in low-speed protocol designs, a single-ended signal is transmitted down a transmission line as a pulse referenced between a signal conductor and a return path. The return path is often referred to as “ground,” but at higher frequencies, the return path should be considered a critical part of the transmission line. The return path in a single-ended system might be a ground plane under a microstrip trace, an adjacent signal pin in a connector, or the outer tape shield of a cable. It is very challenging to achieve high data rates using single-ended signaling. Typically, data rates for single-ended signals range from approximately DC (e.g., reset signals, LED lights) up to 8.4 Gbps (e.g., DDR memory, UClc™).

iii. Differential Signals

A differential signal consists of two wires, each carrying two separate pulses that switch in opposite directions. For example, one pulse is switching from logic level 1 to 0 while the other pulse is switching from logic level 0 to 1. If a differential signal is perfectly symmetrical or balanced, it will propagate effectively on two identical conductors, 180 degrees out of phase and canceling the effects of symmetrically applied noise (see Figure 2).

In order to reduce interference and extend the capabilities of high-speed circuits, many interfaces have adopted a differential signaling architecture rather than single-ended signaling. Differential signals in PCB designs are more resilient against coupling with nearby magnetic fields (crosstalk), allowing for longer lengths and higher speeds in dense designs.

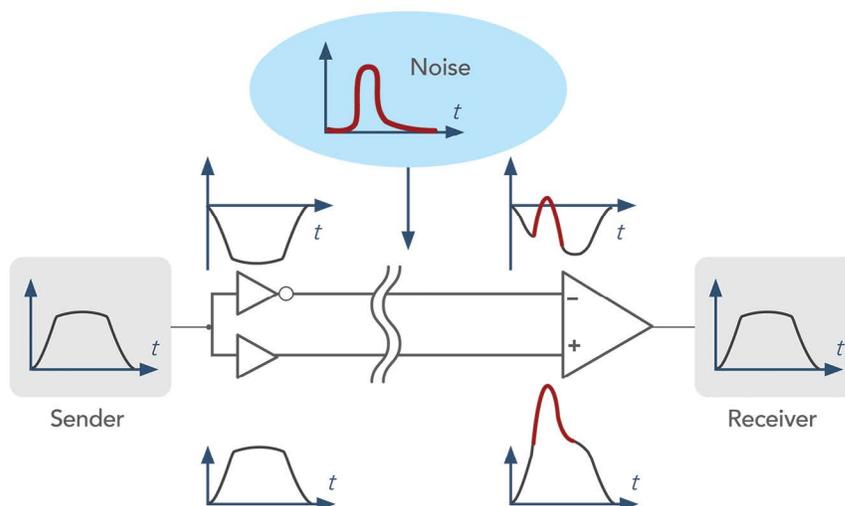


Figure 2. In differential signaling, because the two signals propagate 180 degrees out of phase, they are resistant to the influence of noise, and the signal at the receiver matches the one from the sender.

All interconnect products and signaling standards are defined by data rate or bandwidth capabilities, communicating the number of bits transferred. The definitions related to these specifications are:

Bandwidth and Data Rate

Data rate references the number of bits transferred per second. Bandwidth refers to the frequency spectrum required to transmit those bits.

Baud Rate

Number of signal units per second or data rate divided by number of bits per baud (e.g. 56 Gbps PAM4 signaling has a baud rate of 28 Gbps i.e. $56 \text{ Gbps} / \log_2(4) = 28 \text{ GBaud}$).

Nyquist Frequency

Fastest switching speed of an interface or baud rate, divided by 2:

- Nyquist Frequency for 28 Gbps NRZ is 14 GHz
- Nyquist Frequency for 56 PAM4 is 14 GHz

Aggregate Data Rate

Describes the summation of the data rates of all the individual lanes

within an interconnect and not just the capability of a single lane. For example, 800 Gb Ethernet may describe eight lanes operating at 100 Gbps. Use caution and context to verify data rate statements.

Unit Interval

The length of a single bit transition.

$$\text{Unit Interval} = \frac{1}{\text{Nyquist}} * \frac{1}{2}$$

**Computed the same way for NRZ or PAM4.*

Bit Error Ratio (BER)

A measure of errors occurring on a complete link. It may be a measured or simulated value. $\text{BER} = \frac{\# \text{ errors}}{\# \text{ of bits transmitted}}$. Signaling standards provide minimum limits most often $1e-12$ or $1e-15$. However, in some cases, detector error ratio (DER) is specified, which details the error tolerance prior to error correction encoding. Examples of DER targets are $1e-4$ and $1e-6$.

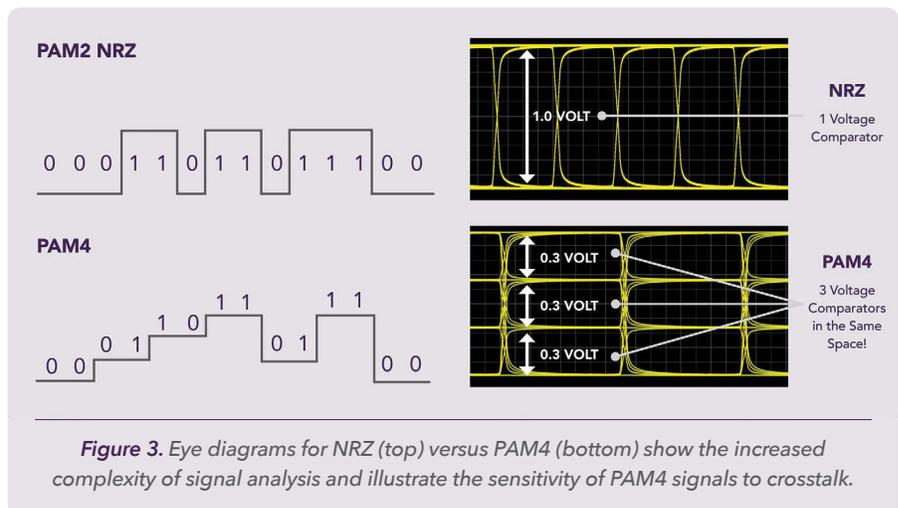
i. NRZ & PAM4

For the last few decades, high-speed links in the data center and compute environment have used two voltage levels in signaling, with low voltage representing binary 0, and high voltage representing binary 1. This scheme is also known as non-return to zero (NRZ) or pulse amplitude modulation 2-level (PAM2).

As Nyquist frequency increases to a higher data rate, loss and reflection become a challenge. A shift to four-level signaling (pulse amplitude modulation 4-level; PAM4) encodes data in the amplitude and doubles the data rate for signals operating at the same Nyquist frequency as PAM2.

Each of the four voltage levels corresponds to one of four bit-sequences (00, 01, 10, 11), providing two bits on the space previously occupied by one, yet not increasing operating frequency.

Unfortunately, PAM4 signaling is more sensitive to noise sources such as reflection and crosstalk (see Figure 3). This is due to the reduced signal amplitude (1/3 of NRZ), effectively reducing the signal-to-noise ratio. The highest speed standards operating at NRZ/PAM2 are 28 and 32 Gbps. Above this data rate, PAM4 is typically used, beginning at 56 and 64 Gbps and beyond.



S-parameters, also known as scattering parameters, are a unified set of frequency-domain performance characteristics that can be used to completely define the properties of an electrical device.

S-parameters can be generated from a simulation, or they can be measured with a vector network analyzer (VNA). S-parameters are treated like a black box between input and outputs: the performance through is described; however, the contents are hidden. This makes S-parameters an ideal way to share characteristics while protecting intellectual property.

The total number of available S-parameters for characterizing a specific electrical device is determined by its number of ports.

S-parameter models may be used to make performance charts or can be used directly in full channel simulations. From S-parameters, numerous SI characteristics can be extracted including insertion loss, return loss, and crosstalk (see Figure 4).

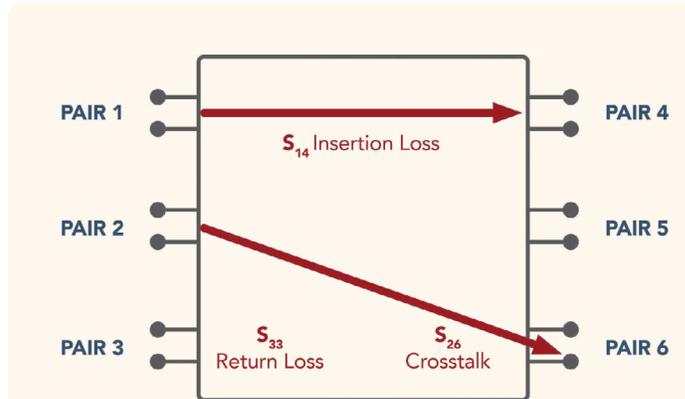


Figure 4: S-parameter measurements give an indication of the electrical device's performance, in terms of insertion loss, return loss, and crosstalk. This figure identifies three relationships of interest in a six-port device under test.

Characterizations in the frequency domain are not specific to a particular data rate. Interpretation depending on frequencies of interest is left to the reader. The following sections provide a guide.

i. Insertion Loss

In the frequency domain, the transferred signal through a medium is characterized as insertion loss (IL). In a two-port device under test (DUT), insertion loss is the magnitude of S_{21} in an S-parameter matrix and expressed in dB, where the nomenclature "21" (expressed as "two-one") refers to the signal observed at port 2 when stimulated at port 1.

Insertion loss is expressed as a negative number for attenuation and as a positive number for gain. It is expressed in dB as the ratio of output to input.

In some cases, industry specifications for insertion loss must be satisfied for components or complete channels.

Often component bandwidth is defined as the point where insertion loss crosses -3 dB. However, for high-speed applications, this rule is less applicable. It is not uncommon to require -1 to -2 dB insertion loss from a small component (like a connector) at Nyquist frequency (see Figure 5).

For larger components, like cables or even packages, insertion loss is significant and a holistic assessment, channel insertion loss must be evaluated against interface requirements.

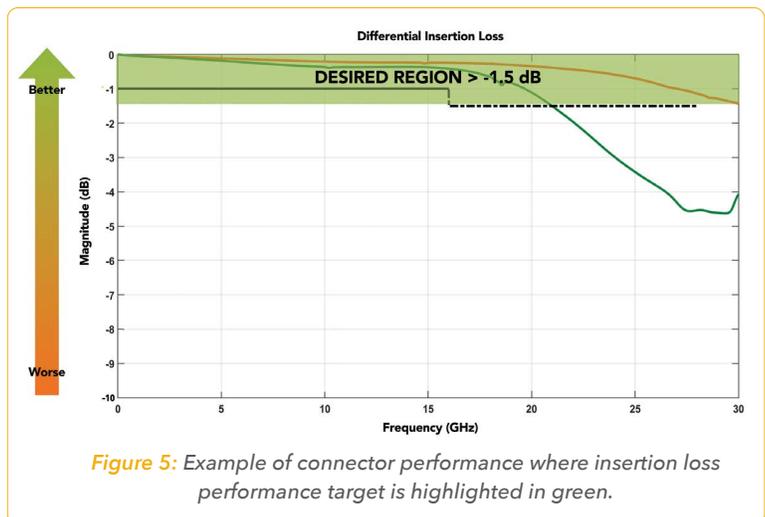


Figure 5: Example of connector performance where insertion loss performance target is highlighted in green.



Frequency Domain & S-Parameters (continued)

ii. Return Loss

Return loss (RL) is a measurement of reflected noise in a single port due to impedance mismatch against a reference value (see Figure 6). As device impedance becomes further mismatched to the reference impedance, return loss increases in the positive direction. Reference impedances are most often 50 Ω , 46.25 Ω or 42.5 Ω , depending on the application.

iii. Crosstalk

Crosstalk is unwanted coupled noise that a signal lane experiences from other nearby lanes or sources. Every part of the interconnect, from chip to chip, is a potential source of crosstalk. Most applications desire crosstalk levels of -40 dB through Nyquist frequency (see Figure 7).

There are two types of crosstalk of concern in high-speed systems, near-end crosstalk (NEXT) and far-end crosstalk (FEXT) (see Figure 8). NEXT is the measure of crosstalk coupling from transmitting (Tx) lanes onto nearby receiving (Rx) lanes. NEXT is most critical when coupling sources (vias, connectors, etc.) occur near the transmitting source (where Tx signal levels are the highest and the Rx signal levels are the smallest).

FEXT relates to signals traveling in the same direction. For example, FEXT is the noise that a transmitting lane experiences from other transmitting lanes. It is generally viewed in the context of the length and loss of the channel. With FEXT, both the crosstalk levels and signal levels are attenuating together before reaching the receiver.

Crosstalk power sum is the combination of multiple crosstalk responses in an effort to describe the total crosstalk noise in a system (see Figure 9). It may be separated as NEXT and FEXT power sums.

iv. Mode Conversion

Mixed modes are undesirable energy lost from or added to the differential signal. They can be measured at the system or component level. SDC, or differential-to-common mode conversion, is the amount of transmitted differential signal that remains when the positive and negative signals of the pair are subtracted. Similarly, SCD is common-to-differential mode and represents noise sources added to the differential signal that remain after subtraction.

For a perfectly balanced differential pair, SCD & SDC are zero. Imbalances and skew within the pair lead to mixed modes that can be observed as through, reflected, or coupled noise. Sometimes specifications provide limits for mixed modes.

v. Electromagnetic Interference

Electromagnetic interference (EMI) refers to the electrical noise that is emitted to other electrical devices that are operating nearby.

Because of the serious nature of electromagnetic compatibility (EMC) issues, many governments require EMI compliance testing of active electronic systems. In the US, regulations are administered by the Federal Communications

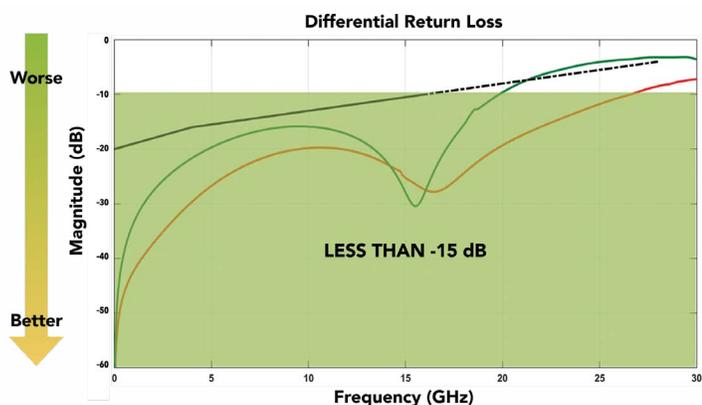


Figure 6: As a rule of thumb, RL values of less than -15 dB in the frequency band of interest are desirable, and a value of -15 dB is typically sufficient.

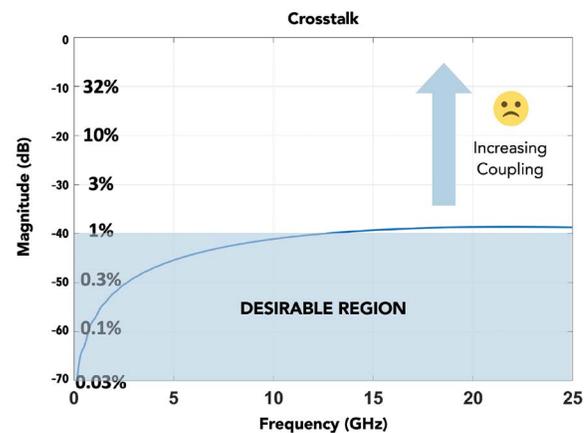


Figure 7: Crosstalk is measured in dB as the ratio of sent to received noise; smaller (negative) numbers represent less crosstalk (which is desirable).

Commission (FCC). Military applications may require more stringent testing.

Techniques to mitigate EMI include routing PCBs internally as stripline and grounded caging/shielding around external connectors.

vi. Voltage Standing Wave Ratio

Another way of characterizing the effects of impedance mismatch in the frequency domain is voltage standing wave ratio (VSWR; pronounced “viz-wer”). Impedance discontinuities within a terminated cable connector and/or terminated PCB connector (terminated connector system) will cause partial reflections of a traveling wave. These reflections will either interfere constructively (add to the magnitude when in phase) or interfere negatively (out of phase) with the original traveling wave. The resultant wave is called a standing wave as it does not actually travel along the transmission line. VSWR describes the ratio between these maximum and minimum voltages measured at a given point before the terminated connector system within the transmission line.

VSWR is a term commonly used in RF and microwave environments. It is often specified as a “one number rating,” especially for coaxial connectors. In such cases, the impedance mismatches within the terminated connector system will be the dominant electrical characteristic limiting its performance in a high-frequency system. Performance data for a coaxial connector might simply be provided as “VSWR 1.20.” This is shorthand for an implied maximum VSWR of 1:1.20 of the connector when used in a system with an appropriate impedance, and across the frequency band of interest.

Since VSWR and return loss are both related to impedance, VSWR can provide quick insight into the amount of voltage that is reflected into a transmitter from a terminated interconnect system. Return loss (measured in dB) provides similar insight into the ratio of the transmitted power to the reflected power and thus the eventual level of a signal that is transmitted through the same interconnect system.

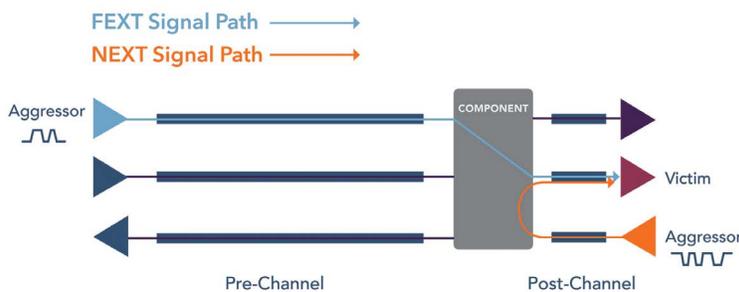


Figure 8: FEXT and NEXT result from different signal paths. In applications, designers seek to isolate transmit and receive lanes from each other to minimize NEXT and FEXT.

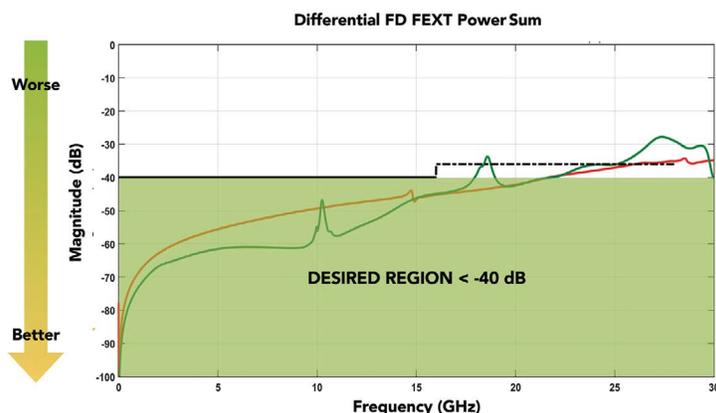


Figure 9: Power sums are often used for industry specifications to restrict the total allowable noise. In this case, the desired total FEXT is below -40 dB.

IV

Time Domain

Analysis in the time domain reveals the pertinent behavior of an interconnect and is specific to a given data rate. The advantage of time domain analysis is that it provides spatial resolution and can inform us about behavior at every location throughout the topology.

i. Impedance

Impedance (Ω) is a measure of the behavior of the interconnect. It is influenced by signal conductor and reference conductor surface area, the gap between them, and the dielectric property of whatever is between them (air, plastic, etc). Impedance is a function of inductance and capacitance, and is highly influenced by conductor surface area. The impedance value affects return loss.

For high-speed interfaces, impedance is measured as an instantaneous (2D) value, called characteristic impedance. Systems are generally designed to meet an impedance target. Often these system impedance targets apply to the individual components or the PCB traces in an attempt to better match the system impedance.

In practice, the difficult to control pieces of the interconnect, such as vias, surface mount (SMT) pads, and ball grid array balls, are lower in impedance. This can require a lower impedance design of components and routing in order to yield better signal integrity in the system. Some typical system impedances are shown in [Table 1](#).

Impedance Requirements for Common High-Speed Signals		
Interface	Impedance (Ω)	Mode
PCI Express [®]	85	Differential
SATA	85	Differential
Clocks	85, 100	Differential
Ethernet	100	Differential
DDR, DQ, DQS	40, 50	Single-Ended
Miscellaneous Signals	50, 55	Single-Ended
USB	85	Differential

Table 1

While PCB routing is generally uniform, vertical components (such as connectors, vias, and sockets) have a variable impedance because of their complex geometry. Mismatches in impedance throughout an interconnect create reflections and degrade performance. This discontinuity occurs at every

point in the transmission path where there is a change in impedance the signal “sees.” These types of reflections are also called inter-symbol interference (ISI).

Time domain reflectometry (TDR) is a common diagnostic used to review impedance throughout a structure; it can be measured or simulated. A step response is provided at an input, reflected voltage is observed, and the ratio of reflected voltage to input voltage (reflection coefficient) is converted to characteristic impedance. In fact, the TDR plot identifies the physical location of impedance discontinuities known by their delay. A desirable TDR plot is smooth and depicts a gradual change in impedance (see [Figure 10](#)). Note: TDR results are subject to the rise time used. The rise time used should be appropriate for the signaling standard.

Connectors are generally not characterized at a specific impedance; in fact, it is expected that impedance could vary as much as 20%, depending on the data rate and application. For connectors, then, overall impedance is characterized by return loss performance. Since return loss is referenced to a specific value (100 Ω , 92.5 Ω , or 85 Ω), it captures the overall severity of the discontinuities in the component.

It is common practice to renormalize a measurement or simulation from 100 to 92.5/85 ohms, thereby better representing the performance for the intended application. Give care to reading TDR and return loss plots by verifying the reference impedance that was used.

All measurements for products such as RF connectors, adaptors, and cables are precision tuned to 50 ohms and interoperate with little impedance discontinuity. For this reason, measurements and models are most often referenced to 50 ohms, 75 ohms single-ended, or 100 ohms differentially. Components that are not designed for 100 ohms may then appear poor, showing a mismatch against the equipment output or reference.

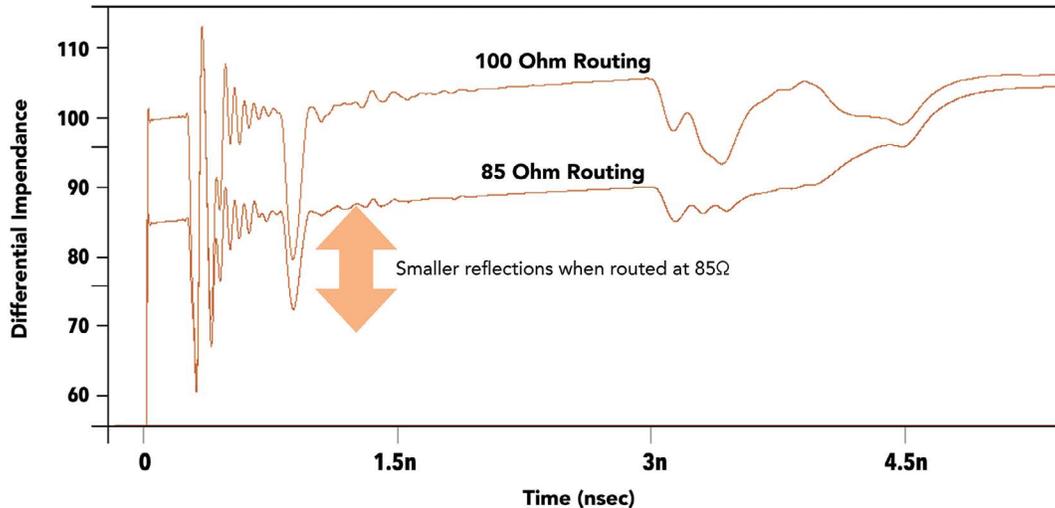


Figure 10: This figure shows an example of two TDR responses from a PCIe® system: one model with the PCB trace at 85 Ω and the other at 100 Ω. Note the physical locations on the bottom of the graph and their subsequent effect on the system’s characteristic impedance. This graph shows larger discontinuities at 100 Ω.

ii. Propagation Delay & Skew

Propagation delay is defined as the amount of time it takes for a signal to propagate through an interconnect path. Knowing the propagation delay of the various signal paths can be critical for system timing analysis for some interfaces.

Skew is defined as the difference in propagation delay between multiple wires. For a single-ended bus, skew between data and a clock may be important. In a differential pair, skew between the two wires composing the pair is critical. Between differential pairs, skew may be less stringent, and requirements vary by interface.

Within a differential pair, skew leads to increased insertion loss, impedance mismatch, crosstalk, and EMI. Sources of skew may include bends in PCB routing, PCB routing parallel to glass bundles called “fiber weave skew,” right-angle connectors, and cable assemblies physical length mismatch.

iii. Rise Time & Dispersion

Rise time is the rate at which a signal changes from low to high. It is usually defined between 10 and 90% (or 20 and 80%) of the total voltage range. For high-speed interfaces, rise time is related to data rate.

As a rule of thumb, rise time is 25% of the unit interval. So, a 10 Gbps signal contains the same signal content as a 25 ps rise time: $0.25 * (1 / 10E9)$. The rise time is the same for 28 Gbps NRZ and 56 Gbps PAM4 signals as they share the same Nyquist frequency and unit intervals (~36 ps). For this case, rise time = 9 ps, unit interval = 36 ps, and Nyquist frequency is 14 GHz.

Time domain characterizations require a rise time input, most commonly TDR. Rise time used for TDR should be related to the data rate of interest. It is important to note that rise time degrades as a signal passes through the interconnect due to dispersion. Dispersion is the spread of signal due to changes in propagation delay across frequencies in PCB dielectrics. Receiver equalization is designed to compensate for dispersion.

IV

Time Domain (continued)

iv. Apparent Impedance

Apparent impedance is the effective impedance of a component when measured or used at a specific signal rise time or frequency, in a specific impedance environment. As rise times get slower and the frequency bandwidth goes lower, the effective, or apparent, impedance of a component moves closer to the impedance level of the circuit in which the component is being used.

At slow rise times, the device will appear to have an impedance value close to the reference or system impedance. But as rise times decrease (in other words, as edge rates get faster), the measured impedance values begin to move toward the true characteristic impedance of the component. At an infinitely short rise time, we would measure the true characteristic impedance of a device.

This effect is important when seeking an interconnect solution for a system with an impedance other than the reference impedance used in the characterization process. In those instances, the impedance values at the fastest rise times on the TDR impedance profile should be used as an approximation of the interconnect's "true" characteristic impedance (see Figure 11).

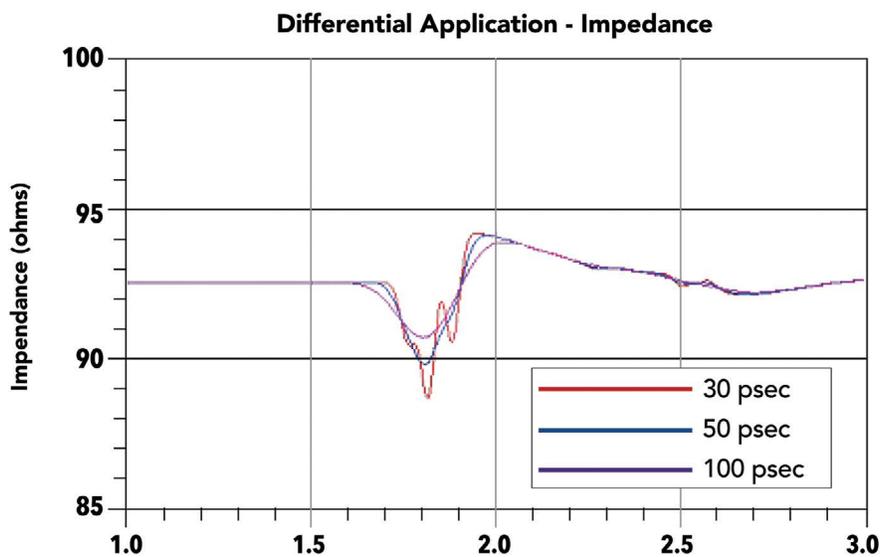


Figure 11: Measured TDR Differential Impedance for a Samtec NovaRay® 7 mm stack height from high-speed characterization reports with three apparent impedances at 30, 50 and 100 ps rise times.

V

Single Value Metrics

i. Effective Return Loss (ERL)

Effective return loss (ERL) is a figure of merit representing measured RL and is a single value. ERL is the amount of digital signal returned which is statistically reduced to an effective value at the test point. It may address both compensable and un-compensable ISI and is computed from RL (see description of return loss, page 8).

The concept of ERL was introduced during the specification development of the IEEE 802.3 50 Gbps Ethernet Standard. The intent of this metric is to control variations in system performance due to excessive reflections that occur when pieces of the system are designed and budgeted separately but later expected to work together in high volume.

As the name implies, ERL is related to the return loss of a device, channel, or component in that energy is injected into a port and the return signal is analyzed; this is like echo pinging into the scattering parameter. The injected signal is a unit pulse that represents a single symbol. The histogram of this return signature is then combined with a histogram of a collection of random symbols to create a single value property. Often this combination is done with the cumulative distribution of the stochastic nature of symbol reflections. The value is reported in dB and as a necessity requires a data rate and symbol error rate.

ii. Integrated Crosstalk Noise & Integrated Return Loss (ICN & IRL)

Integrated crosstalk noise (ICN) and integrated return loss (IRL) are single numbers used to characterize the total noise in a system or component. To achieve this, a weighting filter is configured to the data rate of interest, focusing only on applicable frequencies. Once filtered, the response is integrated into a single number expressed in mV. Many standards use ICN calculated from the crosstalk power sum for compliance, including IEEE, OIF, PCIe®, and USB. For reflections, IRL is used for USB cable compliance.

ADDITIONAL RESOURCES



gEEK® spEEk Webinar:
"What is ERL & How is it Computed?"



Samtec White Paper:
"Characterizing High-Speed Digital Interfaces: Reflecting on Reflections"

VI

Samtec Channel Performance Metric

Recognizing that it is important to consider an interconnect as part of the system, Samtec offers a Channel Performance Metric (CPM) for its products that provides a recommended maximum data rate based on system complexity. This chart is displayed in the catalog and product's web page.

Samtec CPM is calculated using full end-to-end channel simulation including PCB, packages, reflections, and crosstalk. Maximum data rate is determined when a minimum BER threshold is reached.

ADDITIONAL RESOURCES



Samtec Blog Article:
"High-Speed Connector Rating Accounts for Entire System"



Samtec Blog Article:
"New Protocol Capabilities for High-Performance Interconnects"

VII

Model Considerations

i. Simulation Tools

There are many modeling tools to enable electrical behavior characterization. These include 2D, 2.5D, 3D, and hybrid field-solving tools that focus on the multiphysics of larger structures broken down to simpler nodal coarse static or dynamic mesh solutions.

There are also system-level characterization analysis tools based on building schematics and libraries, including scripted programmed functionalities that allow engineers to bring models from concept to realization (see Figure 12).

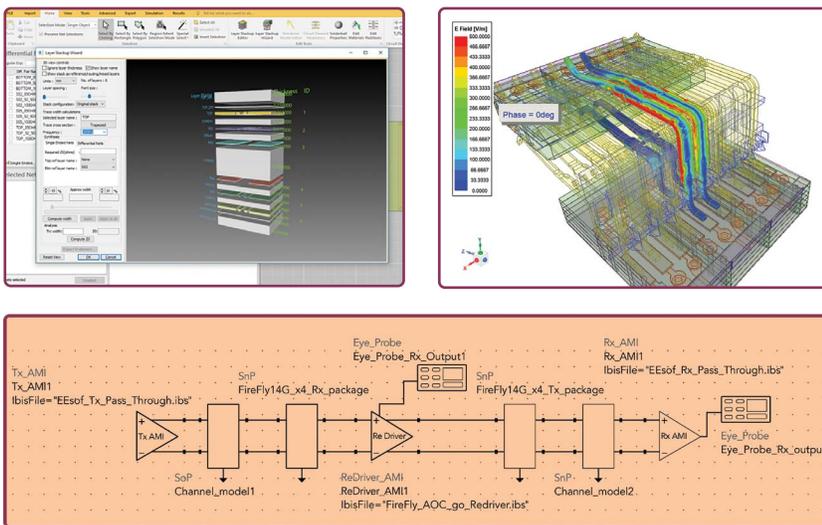


Figure 12: Various simulation tools enable electrical model characterization, including 2.5D wave EM solvers (top left), 3D field solvers (top right), and system analysis tools (bottom).

ii. Boundaries

Understanding a model's boundary is important when interpreting frequency or time domain reports. Models can vary in terms of the impedance and duration of PCB routing that is included. For example, if the pads or vertical transitions of the PCB or breakout region (BOR) are not included, performance may further degrade when they are added. Comparing products with different extents of the interconnect included may lead to incorrect conclusions. Clear documentation should indicate the physical location of model ports.

In some instances, connector models do not include PCB breakout areas. This enables modeling of application specific stack-up and breakout needs separately. Simulation tools provide functions to cascade S-parameters, combining separate connector and PCB models (see Figure 13).

iii. Validation

Several criteria are often checked to determine model or measurement quality for use in system analysis, including passivity, causality, and reciprocity. Definitions of these terms are provided in the IEEE 370-2020 standard. Software to evaluate these limits is provided by IEEE 370-2020 and is also being implemented in several commercial tools.

Model bandwidth, or maximum frequency available for a given model, needs to meet or exceed the spectrum for which energy exists for a given data rate. Therefore, a minimum range of 1.5x to 3x Nyquist frequency is recommended to account for the higher frequency harmonics contained in the signal energy.

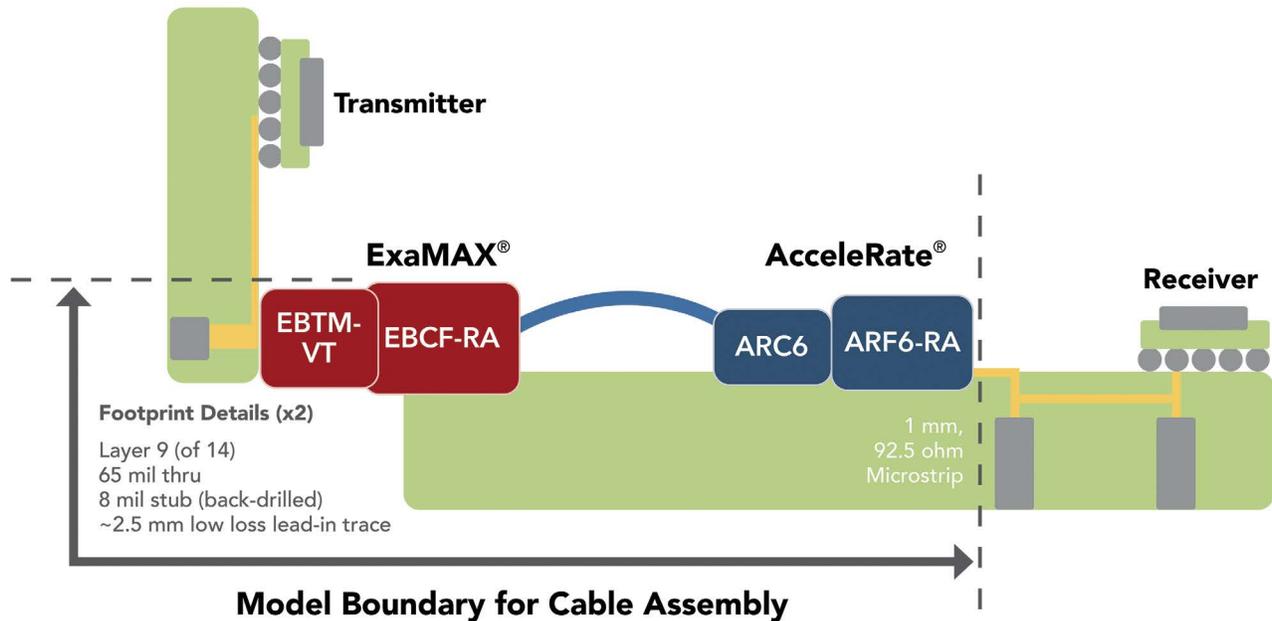


Figure 13: This diagram shows connector models (red and blue) that can be combined with PCB, Tx and Rx models (green) within a simulation tool to capture a unique stack up design. Samtec ExaMAX® (EBTM/EBCF Series) and AcceleRate® (ARC/ARF6 Series) are shown.

iv. Encrypted 3D Components

Encrypted 3D components within 3D field solver tools allow for a better collaboration space between component-level and assembly-level designs while protecting the intellectual property of the component manufacturer. As data rates increase, it becomes more important to have accurate system-level models of the entire signal channel from package die to package die with the precise plane of reference match.

Samtec’s encrypted 3D components, for instance, have all of the specifications with corresponding material properties, physical structure attributes, points of contact, wipe distance, and deflections incorporated in the model.

Designers can use encrypted models in their workspace, directly on their board designs, with their own parameters and launches.

ADDITIONAL RESOURCES



Video:
 How to Encrypt ANSYS®
 3D Components



Video:
 ANSYS® 3D SI Models for
 Samtec Interconnects

During a system's design phase, obtaining an assessment of SI performance of the complete channel design may be required before moving on to the development of a physical prototype. To support this system-level assessment, a design team needs electrical simulation models, usually in the form of S-parameters, and a particular physical protocol and topology expectation to execute channel simulation.

Simulation of an entire link can be done in a number of available tools. Many standards offer simulation tools preloaded with transmitter and receiver configurations. This includes the free, open-source tool Seasim for PCI Express® channels and the channel operating margin (COM) algorithm for IEEE and OIF. If specific silicon is known, IBIS-AMI models (which can be used in commercial tools such as ADS) may be obtained to represent the actual noise levels, which may be better than specification limits. Channel simulation can require product eye diagrams, COM results, or BER.

i. Eye Diagram

An eye diagram is a characterization of system level performance. Eye patterns are generated by sending continuous streams of data from a transmitter to a receiver and overlaying the received bits upon one another. Over time, the received data builds to resemble an eye.

Negative SI effects in the transmission path can cause the signal to distort, which over time, will cause the eye to "close." Specifications may define a minimum eye mask template, which can be placed on the amount of open area as an aid to determine compliance (see Figure 14). Eye diagram specifications are used for the entire interconnect path, or subsets of the path, but are not used for smaller components like connectors or cables.

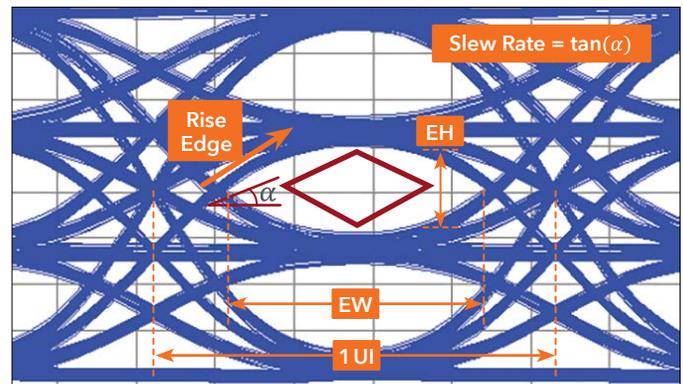


Figure 14: Sample eye diagram. The red diamond is the eye mask, and the blue lines show the received bits. (EH: Eye Height, EW: Eye Width, UI: Unit Interval)

ii. Channel Operating Margin (COM)

During the development of 25 Gbps Ethernet signaling in IEEE 802.3, a need arose to help unify the budgeting capability of transmitter, receiver, and channel specifications. The previously recommended frequency domain masks were abandoned in favor of time domain specification of the system. This time domain-based specification is known as COM.

COM is a figure of merit for a channel derived from a measurement of its scattering parameters. It is related to the ratio of a calculated signal amplitude to a calculated noise amplitude at a receiver input.

ADDITIONAL RESOURCES



Free Software:
Request a Copy of
Samtec's COM Code



gEEK® spEEK Webinar:
"IEEE COM for
Channel Analysis"



gEEK® spEEK Webinar:
"Mechanics of Running
COM"

Transmitters (represented by "n") are used to transfer data between physical layers (PHYs). There are "n" near-end crosstalk paths, and "n-1" far-end crosstalk paths going into a victim receiver, as illustrated in **Figure 15**. The specific number of paths depend on the number supported lanes.

COM is computed using defined path calculations and a specified procedure. In addition to S-parameters, COM accepts parameter values such as signaling rate, frequency (min, max and step), and the device package model to use in the computation (see **Figure 16**). For convenience, and to ensure consistency in computational results, the COM procedure has been implemented in a MATLAB® script. An accompanying spreadsheet referred to as "COM configuration file" is used to load the parameter values into the MATLAB procedure script.

As opposed to an eye diagram, COM operates as a budget for insertion loss, insertion loss deviation (ILD), crosstalk, and SerDes parameters.

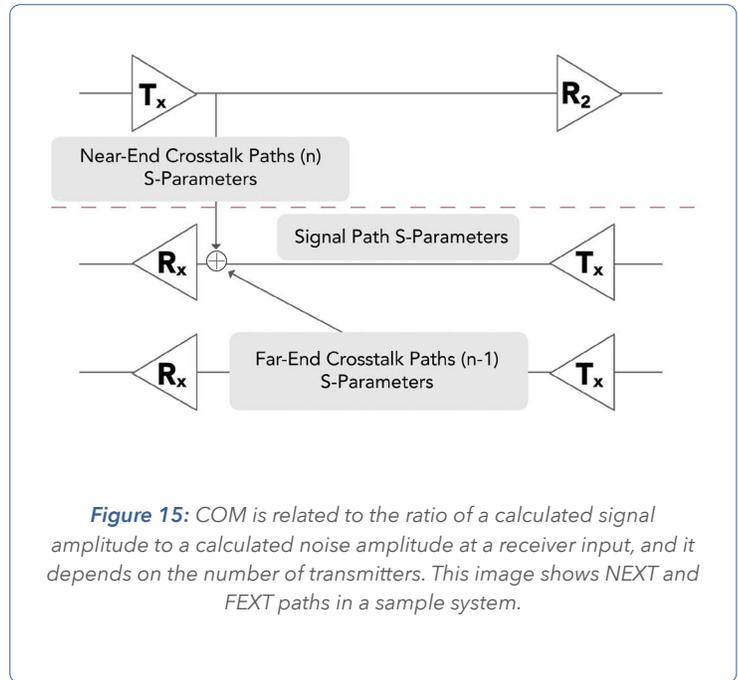


Figure 15: COM is related to the ratio of a calculated signal amplitude to a calculated noise amplitude at a receiver input, and it depends on the number of transmitters. This image shows NEXT and FEXT paths in a sample system.

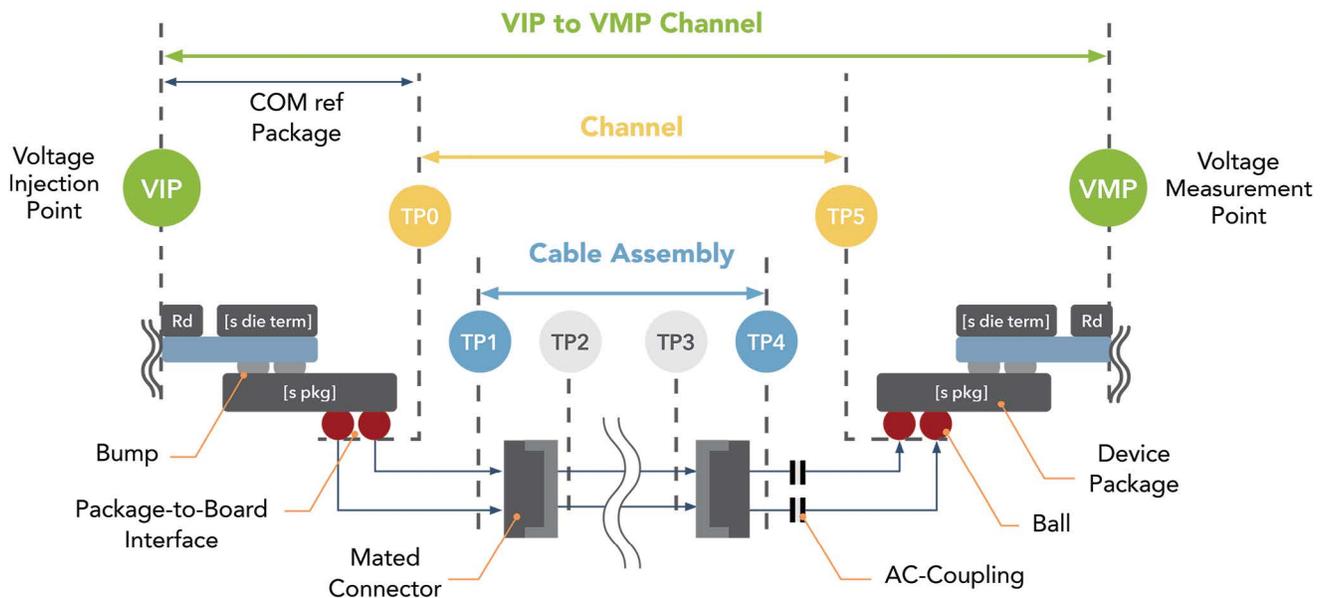


Figure 16: COM voltage injection and voltage measurement points. COM is computed from a voltage injection point (VIP) to voltage measurement point (VMP) from provided measured S-parameters TP0 to TP5.

IX

Selecting a Connector

Connector solutions generally fall into two categories: open-pin-field and assigned signals. Open-pin-field offers the best flexibility to place signals, grounds, or power in any location. Selections with assigned signals usually have superior SI performance due to specially designed ground structures. Cabled connectors may also have assigned positions to properly connect the twinax ground shield.

Many parameters critical to high-speed connector performance will vary significantly depending upon the pin assignment and form factor. An open-pin-field connector will have improved crosstalk performance when two grounds are placed between signals (SSGGSS) as compared to a single ground (SSGSS). A design with a smaller pitch may favor system placement because of its greater density; however, performance could be reduced as higher crosstalk is incurred due to proximity. This is not always true due to innovative designs, so it is critical to refer to SI characterization reports to make the best decisions.

i. Contact Spacing

As the distance between contacts increases, inductive and capacitive coupling decrease. This effect can be observed in an electromagnetic field plot by noting the reduced number and density of field lines connecting the two conductors. For example, a connector with terminals spaced on a 0.80 mm pitch will typically have better crosstalk performance than one with a 0.50 mm pitch. In differential pair systems, increasing the distance between adjacent pairs minimizes coupling and, in some cases, eliminates the need for interstitial grounds, so total signal density can be increased (see Figure 17).

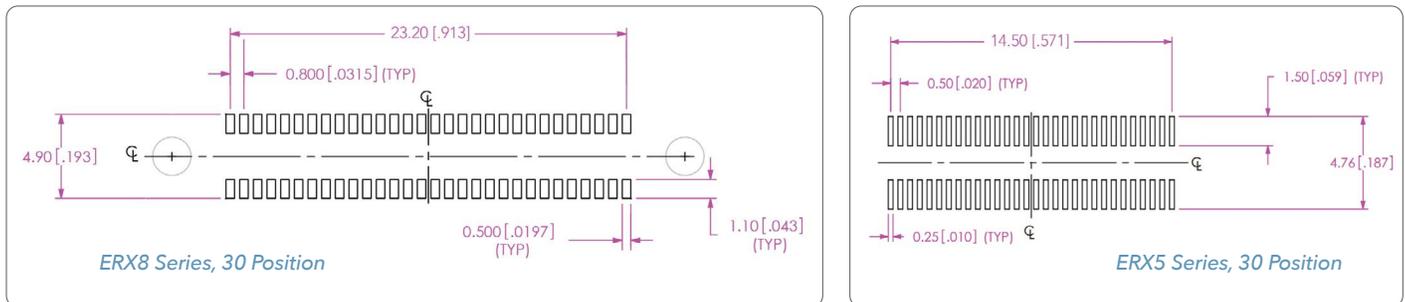


Figure 17: Recommended PCB Layout footprint for Samtec Edge Rate® (ERX8 and ERX5 Series) with 0.80 mm pitch and 0.50 mm pitch, greater pitch spacing, and interstitial spacing.

ii. Pin Mapping

By assigning pins between signals as return paths (grounds), unwanted coupling between signal pins can be minimized. A 1:1 signal-to-ground ratio is typically used in the industry. So, pin mapping for single-ended applications would then be SGSG, while differential pair applications would use DP-G-DP-G. These pin assignments generally provide a good performance vs. density trade-off.

To increase isolation, more return paths could be added between signals. For example, optimal solution mappings could have a 1:2 signal-to-ground ratio. Differential solutions would then use DP-G-G-DP while single-ended applications would use SGGS. These can be directed either vertically or horizontally depending on the connector solution. This approach, however, will reduce the signal density of the interconnect (see Figure 18).

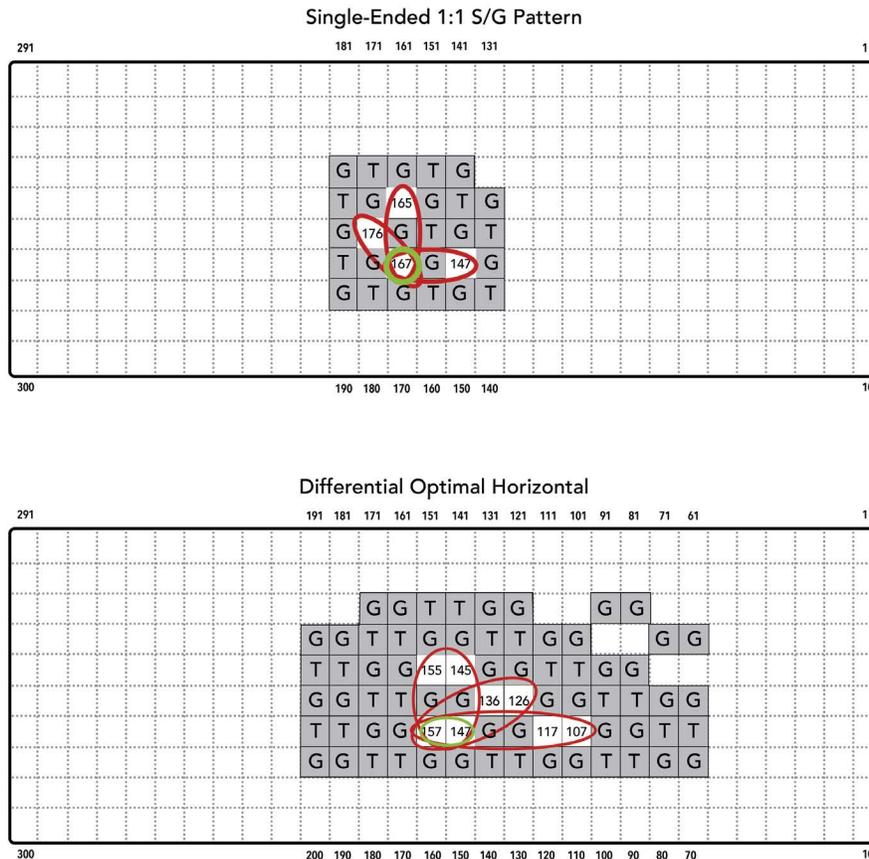


Figure 18: Single-ended 1:1 pattern (above) and differential pair 1:2 optimal horizontal pattern (below) from Samtec's SEARAY™ high-speed characterization report.

High-speed performance of PCB-mount connectors must be considered in the context of the application in a real-world environment. “Connector-only” data can be useful for comparing the relative performance between two similar connectors, but it may be very far removed from the performance practically obtainable in an actual application. This is mainly because of the PCB traces and ground planes in the vicinity of the connector. This region is often referred to as the breakout region (BOR), because, in this area, traces are “broken out” from an optimized, consistent transmission line environment and routed as required to attach to the connector terminals. If not done correctly, system performance can suffer. BOR/launch must be carefully designed to allow for the best possible high-frequency performance.

i. Constraints

When designing a BOR, it is important to first consider the limitations of the design and then improve the performance around these limitations:

- What is the intended routing direction? Right-angle connectors, for example, typically only allow routing in the direction opposite to the cable. What makes the most sense for the use case?
- Does this connector have a single ground (GND) or double GND positions between signals in a row? This will affect crosstalk performance and routing that must travel through rows of vias. If routing through a row of vias, it is critical to design around the routing path early.
- How much space do I have left to add GND vias for shielding, and where can I place them to shield crosstalk most effectively?
- Large open areas should be avoided in the BOR because they can resonate. GND vias can be placed to break up and limit the size of dielectric cavities. Larger cavities resonate at lower frequencies, so the importance of this is bandwidth dependent.
- After the overall layout of the vias and routing has been established, the signal vias can be impedance optimized by changing the distance between the edges of the GND planes and the sides of the signal vias. The cut outs in the GND planes that allow signal vias to transition through layers are known as anti-pads, and the anti-pad diameters are tuned to optimize via impedance.

ii. Outside the BOR

Once the BOR has been finalized, it is time to consider factors for routing across larger areas of the PCB:

- A number of techniques can help minimize skew within a differential pair due to differences in dielectric property of glass and resin in the PCB:
 - Board routing should have a trace pitch that is the same as the fiber weave in the board.
 - Routing at non-orthogonal angles can reduce fiber weave skew. The design should avoid using angles within +/- 10 degrees of the orthogonal directions on the panel because of manufacturing variations between the orthogonal directions of the fiberglass and those of the copper trace etch (see Figure 19).
- Length matching the traces within a signal pair is critical. It is best to do this by having an equal number of left and right turns as a trace routes across the board. Length matching structures like ‘serpentine’ traces are acceptable but should be avoided if the signal can be balanced by matching left and right turns.
- Thieving or copper balancing is placed throughout the board to keep the dielectric thickness consistent through a uniform copper density.
- Routing length across the board should be kept as short as possible within reason. Longer traces increase signal loss and reduce the signal bandwidth.

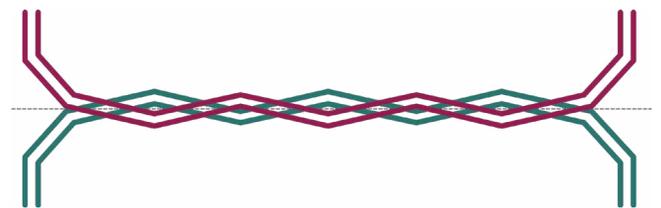


Figure 19: An example of routing style to avoid fiber weave effect.

XI

Signal Integrity in RF Systems

While digital and RF/microwave cables and connectors tend to be application specific, there are a number of similar concerns for designers of high-speed digital and high-frequency systems. High-speed digital designers, therefore, may find some value in the analysis of RF techniques.

Additionally, it is possible to use cables and connectors designed for RF/microwave applications for high-speed digital applications, so some comparison of similar terms might be useful. While a full discussion of RF is beyond the scope of this document, below is a brief listing of some RF terms and how they are analogous to SI ones.

As mentioned above, VSWR is one characteristic that is commonly used to specify RF cables and is related to return loss. Others include cable propagation velocity (which is related to time delay in a digital application), RF phase matching (which is analogous to skew), attenuation (which is analogous to insertion loss), and RF cable shielding (which is analogous to isolation and crosstalk).

There is much to consider when selecting a high-speed interconnect. For additional assistance, see the resources suggested and/or [contact sig@samtec.com](mailto:sig@samtec.com).

SIGNAL INTEGRITY TOOLS & SUPPORT

Samtec Signal Integrity Engineers address next generation system design challenges with industry-leading expertise in high-performance interconnect systems, along with testing and validation services, system optimization support, and easy-to-use design and development tools. Contact sig@samtec.com to discuss your specific application.

SIGNAL INTEGRITY SERVICES & SUPPORT

Frontline Engineering Services

- High Data Rate Simulations
- Channel Analysis
- Signal Integrity Models
- PCB & Breakout Region (BOR) Designs
- Connector Selection

Technical Application Support

- Signal/Power Integrity Expertise
- Testing, Validation & Analysis
- Full Channel SI Analysis/Optimization
- PCB Layout & Routing Assistance
- Full System Design Support

Industry Standards Support

- Member/Participant of 30+ Industry, Corporate & De Facto Standards
- Compatible/compliant products include: VITA, PICMG®, PCIe®, CXL, IEEE, OIF, SFF-SIG, PC/104™, PISMO™, SATA, USB and more
- Visit samtec.com/standards

ONLINE DESIGN & DEVELOPMENT TOOLS

- Innovative product search, connector builder and simulation tools that help streamline the design process
- Large Technical Library offers free 3D models, prints, footprints, test reports, white papers, application notes, etc.
- Semiconductor & T+M partnerships demonstrate next gen 112/224 Gbps PAM4 interconnect solutions

TESTING & VALIDATION CAPABILITIES

Design Qualification Testing (DQT)

Standard testing undergone by all Samtec products to verify the product design meets our intent.

Extended Life Product™ (E.L.P.™)

Rigorous testing that evaluates contact resistance including 10 year Mixed Flowing Gas (MFG) and High Mating Cycles (250 to 2,500). samtec.com/ELP

Severe Environment Testing (SET)

Additional testing evaluates whether select products are suitable for rugged and/or harsh environments and other extreme applications. samtec.com/SET

Leakage Testing

Platform developed for applications with higher voltage levels & extremely sensitive current leakage specifications.

Signal Integrity Screening

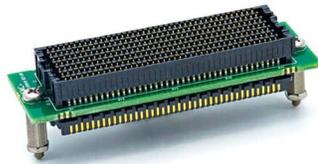
VNA-based test system screens for manufacturing process anomalies that could lead to SI degradation in higher data rate products.

Samtec-designed Evaluation & Development Kits simplify the design process and reduce time to market. Kits are available for many of our high-performance connector sets, high-speed cable assemblies and optical solutions. Custom kits are also available. Visit samtec.com/kits or contact kitsandboards@samtec.com for a full list of availability.

FPGA DEVELOPMENT BOARDS



VITA 57.4 FMC+
HSPC Loopback Card



VITA 57.4 FMC+ Extender Card

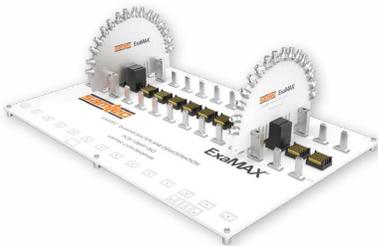


VITA 57.4 FMC+
25/28 Gbps FireFly™ Module



FMC+ HSPC Loopback Card
Supporting Xilinx® Virtex®
UltraScale™+ VCU118 Kit

SIGNAL INTEGRITY EVALUATION KITS



ExaMAX® High-Speed Backplane
System (EBTF/EBTM)



Generate™ High-Speed
Edge Card Socket (HSEC6-DV)



Generate™ Differential Pair
Edge Card Socket (HSEC8-DP)



AcceleRate® HD High-Density
Arrays (ADM6/ADF6)



ExaMAX® Backplane
Cable System
(EBCM/EBTF-RA)



AcceleRate® Flyover®
Slim Direct Attach Cable
System (ARC6/ARF6)



NovaRay® Flyover® Extreme
Density & Performance Cable
System (NVAC/NVAM-C)



Flyover® QSFP
Double Density Cable System
(FQSFP-DD to NVAC/ARC6)



Bulls Eye® 70 GHz
High-Performance
Test System (BE70A)

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ACRONYMS & ABBREVIATIONS

- B -

BER bit error ratio
BOR breakout region

- C -

COM channel operating margin

- D -

DDR double-data rate (refers to memory)
DUT device under test

- E -

EMC electromagnetic compatibility
EMI electromagnetic interference
ERL effective return loss

- F -

FCC Federal Communications Commission (USA)
FEXT far-end crosstalk

- G -

GND ground

- I -

ICN integrated crosstalk noise
IEEE Institute of Electrical and Electronics Engineers
IL insertion loss
ILD insertion loss deviation
IRL integrated return loss
ISI inter-symbol interference

- L -

LED light-emitting diode

- N -

NEXT near-end crosstalk
NRZ non-return to zero

- O -

OIF Optical Internetworking Forum

- P -

PAM2 pulse amplitude modulation 2-level
PAM4 pulse amplitude modulation 4-level
PCB printed circuit board
PHY physical layer

- R -

RL return loss
Rx receive

- S -

SI signal integrity
SMT surface mount

- T -

TDR time domain reflectometer/reflectometry
Tx transmit

- U -

UCIe™ Universal Chiplet Interconnect Express

- V -

VNA vector network analyzer
VSWR voltage standing wave ratio

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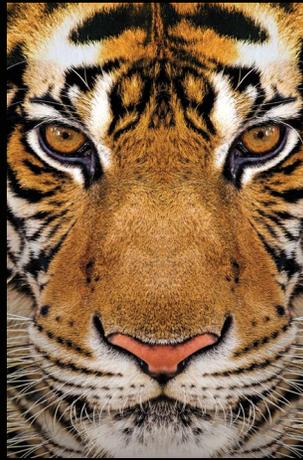
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