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# Current Distribution, Resistance, and Inductance in Power Connectors

Track 10. Power Integrity in Power Distribution Networks

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*Clement Luk, Samtec*
*Gary Biddle, Samtec*
*Istvan Novak, Samtec*
*Gustavo Blando, Samtec*

# Author Bio

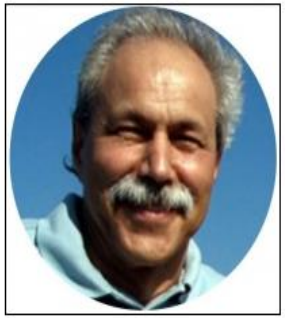
Adam Gregory is a Signal Integrity Engineer at Samtec. He is involved in modeling and analysis of high-speed differential signaling channels. He received a BSEE and MSEE at the University of South Carolina.

Clement Luk is a Signal Integrity Engineer in Samtec. He is involved in high-speed connector, PCIe application and channel simulation and measurement. He received his BSCS and MSEE from University of Wisconsin-Madison.

Gustavo Blando is a Senior Principal Engineer and leading Principal SI/PI Architect at Samtec Inc. In addition to his leadership roles, he's charged with the development of new SI/PI methodologies, high speed characterization, tools and modeling in general. Gustavo has twenty plus years of experience in Signal Integrity and high-speed circuits.

# Author Bio

Gary Biddle received his BS in Physics from University of Florida 1976 and MS in Physics from Penn State University 1991. His work experience includes high frequency VNA and EMI measurements, along with nearly 20 years of simulating PCB and interconnect structures. He has published several articles and holds several patents.



Istvan Novak is a Principal Signal and Power Integrity Engineer at Samtec, working on advanced signal and power integrity designs. Prior to 2018 he was a Distinguished Engineer at SUN Microsystems, later Oracle. He worked on new technology development, advanced power distribution and signal integrity design and validation methodologies for SUN's successful workgroup server families. He introduced the industry's first 25um power-ground laminates for large rigid computer boards and worked with component vendors to create a series of low-inductance and controlled-ESR bypass capacitors. He also served as SUN's representative on the Copper Cable and Connector Workgroup of InfiniBand, and was engaged in the methodologies, designs and characterization of power-distribution networks from silicon to DC-DC converters. He is a Life Fellow of the IEEE with twenty-five patents to his name, author of two books on power integrity, teaches signal and power integrity courses, and maintains a popular SI/PI website.

# Outline

- Introduction & Background
- Establishing Baseline
- Component Level:  DC to High Frequency Simulation to Measurement Correlation
- System Level: SI and PI Interaction
- Conclusions

# Introduction & Background

- This presentation analyzes the frequency dependent resistance and inductance of power connector pin patterns and connection geometries
- Goal is to establish:
  - 1) 3D simulator tools are capable of accurately profiling resistance and inductance at the low frequencies relevant for power integrity simulations
  - 2) The loss of existing 3D models of connectors correlates with measurement at low frequency
- If these goals are met, there is high confidence that simulation can predict impact to power integrity based on connection schemes in a full system

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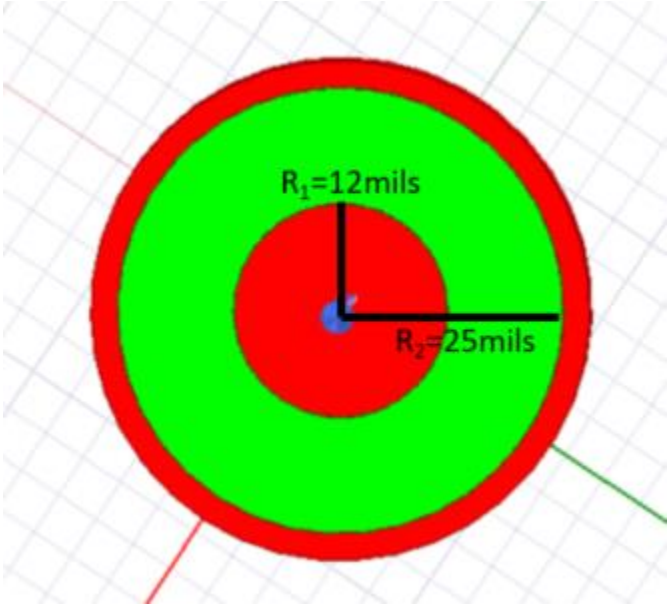
# Establish Baseline with Coaxial Cable

- Coaxial cables have analytical equations for frequency dependent resistance and inductance, so it is a good test case to establish simulator accuracy.
- Signal conductor radius ($r_1$) = 12 mils
- Dielectric radius ($r_2$) = 25 mils
- Conductor conductivity ($\sigma$) = 5.8e7 S/m

Coax Cable cross section



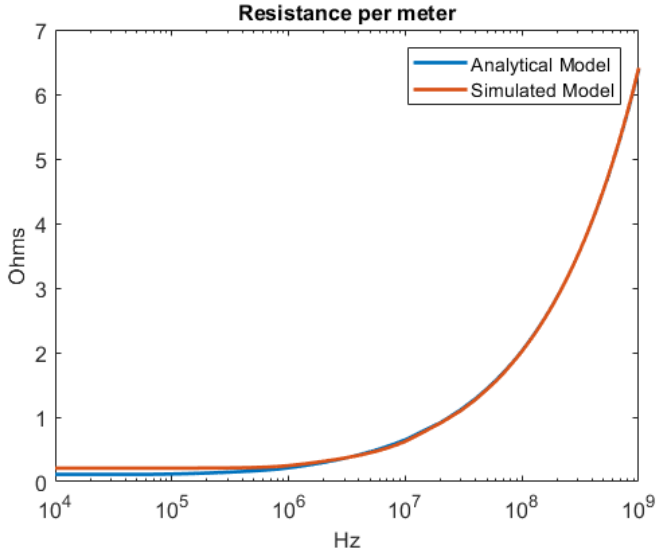

$$skin\ depth\ (\delta) = \sqrt{\frac{2}{\omega\sigma\mu}}$$

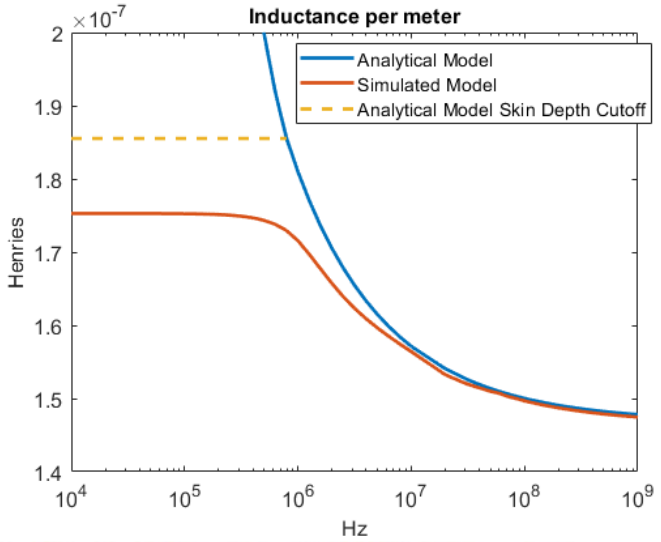
$$Resistance\ per\ meter:\ \ (\mathrm{R}) = \frac{1}{\sigma(2\pi r_1\delta - \pi\delta^2)} + \frac{1}{\sigma(2\pi r_2\delta + \pi\delta^2)}$$

$$Inductance\ per\ meter:\ \ (L) = \frac{\mu}{2\pi}\log\frac{r_2}{r_1} + \frac{R}{\omega}$$

# Coaxial Cable Resistance/Inductance

- Resistance is nearly identical but has some minor offset at low frequencies where the skin depth is larger than the conductor radius.
- Inductance diverges at low frequencies where the skin depth is larger than the conductor radius. The dashed yellow line shows an approximate location where inductance should become roughly constant since current density remains uniform.



# Convert S-parameter to Resistance & Inductance

- For medium and high impedances, short one side of 2-port S-parameter to Ground to create 1-port S-parameter
- For small impedances, shorted loops, use Two-port sunt-through scheme
- Solve input impedance ($Z_i$), Resistance, and Inductance using equations shown below

One-port reflection:

$$Z_i = Z_0 \frac{1 + S_{11}}{1 - S_{11}}$$

Two-port transmission:

$$Z_i = \frac{Z_0}{2} \frac{S_{21}}{1 - S_{21}}$$

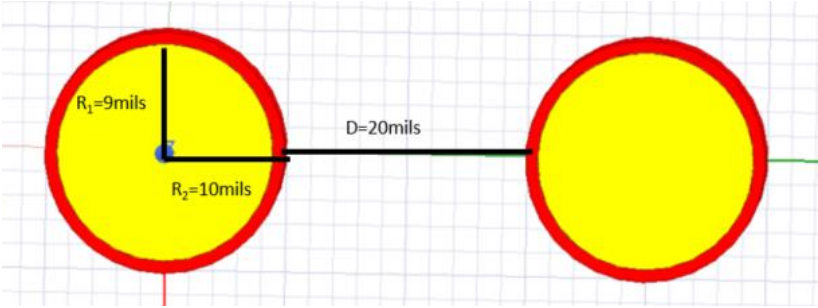
$$Resistance = real(Z_i)$$

$$Inductance = \frac{imag(Z_i)}{\omega}$$

# Approximate Connector w/ Layered Metal

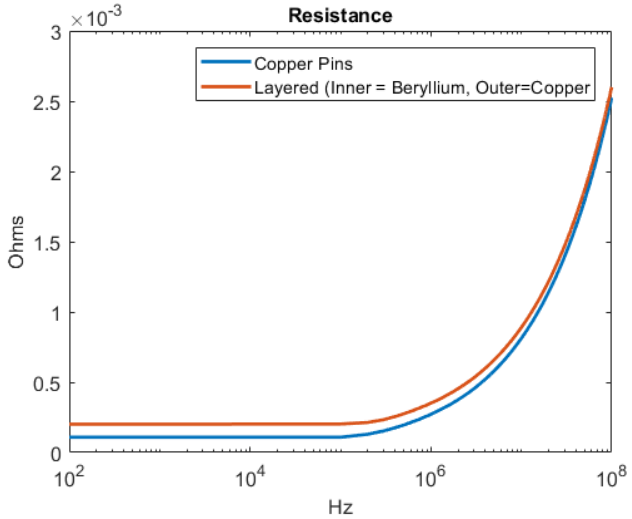
- Simple connector approximation:  2 cylindrical pins in a homogeneous dielectric material.
- Goal is to compare resistance/inductance results for single conductive material vs. a layered metal
- Radius of each pin  = 10 mils.
- Center-to-Center pitch = 40 mils
- Single material:
  - Conductivity = 5.8e7 S/m
- Layered material
  - 9 mil radius core with Conductivity = 2.5e7 S/m
  - 1 mil outer layer with Conductivity = 5.8e7 S/m

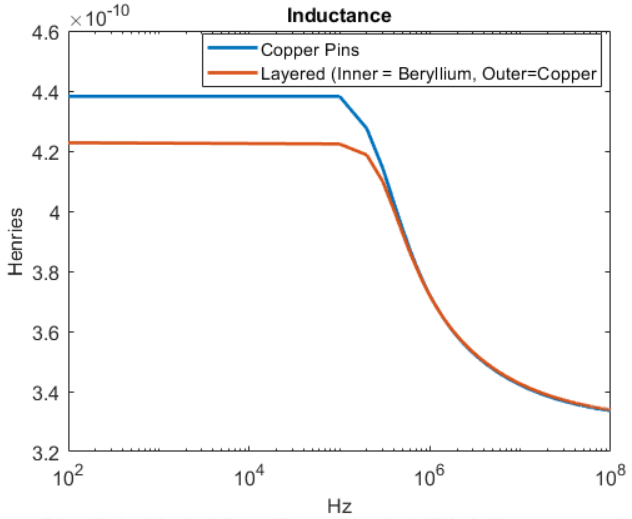
Cylindrical connector pins with layered metal



# Layered metal Resistance/Inductance

- Resistance shows the expected DC offset, and the resistance effectively converges around 100MHz.
- Inductance effectively converges around 1MHz. The skin depth becomes equivalent to 1mil copper around 5MHz. Below 200KHz, there is a 5% decrease in Inductance for the layered pins.
- For this simulation, the layered material accounted for 10% of the total cylinder radius. Actual products have a much smaller plating depth, so the effect of plating was ignored in the remainder of studies. The existing connector models use the material of the inner conductor.



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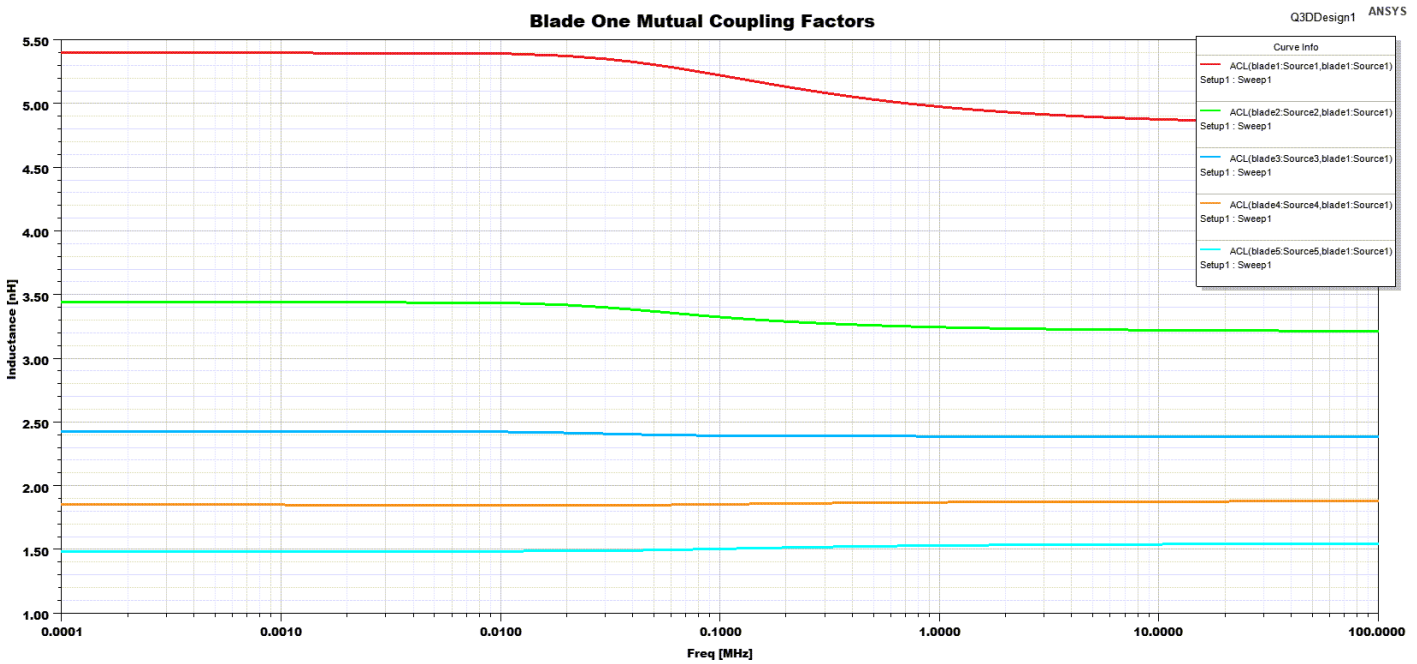
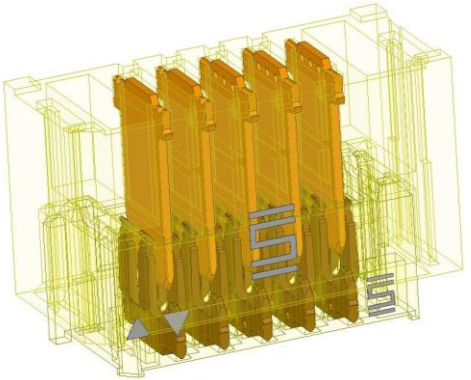
# Power Connector Example

Blade 1 Self Inductance & Mutual Inductances from Blade 1 to all other blades



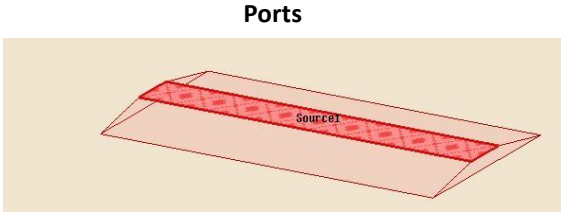

Blade Connector



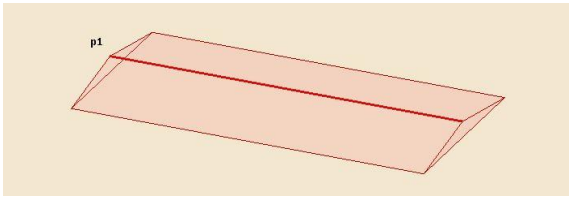
# Simulation Model Design

- Replicates Physical Test Sample [2 blade loop]
- CAD imports to HFSS & Q3D tools
- Multiple Excitation Points to check resolution
- Minimized port excitation effects between tools

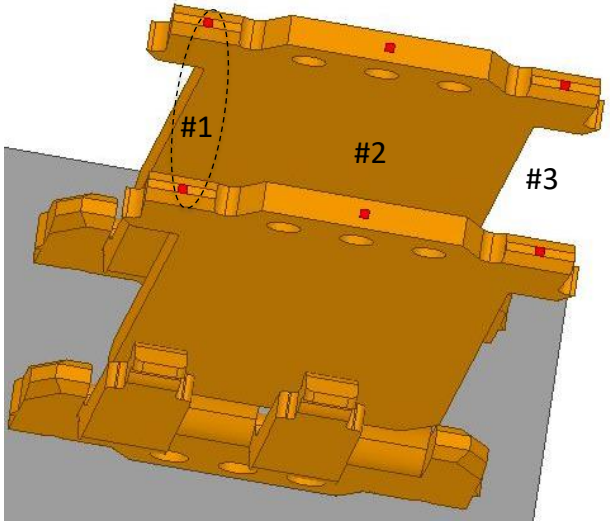
Q3D




HFSS



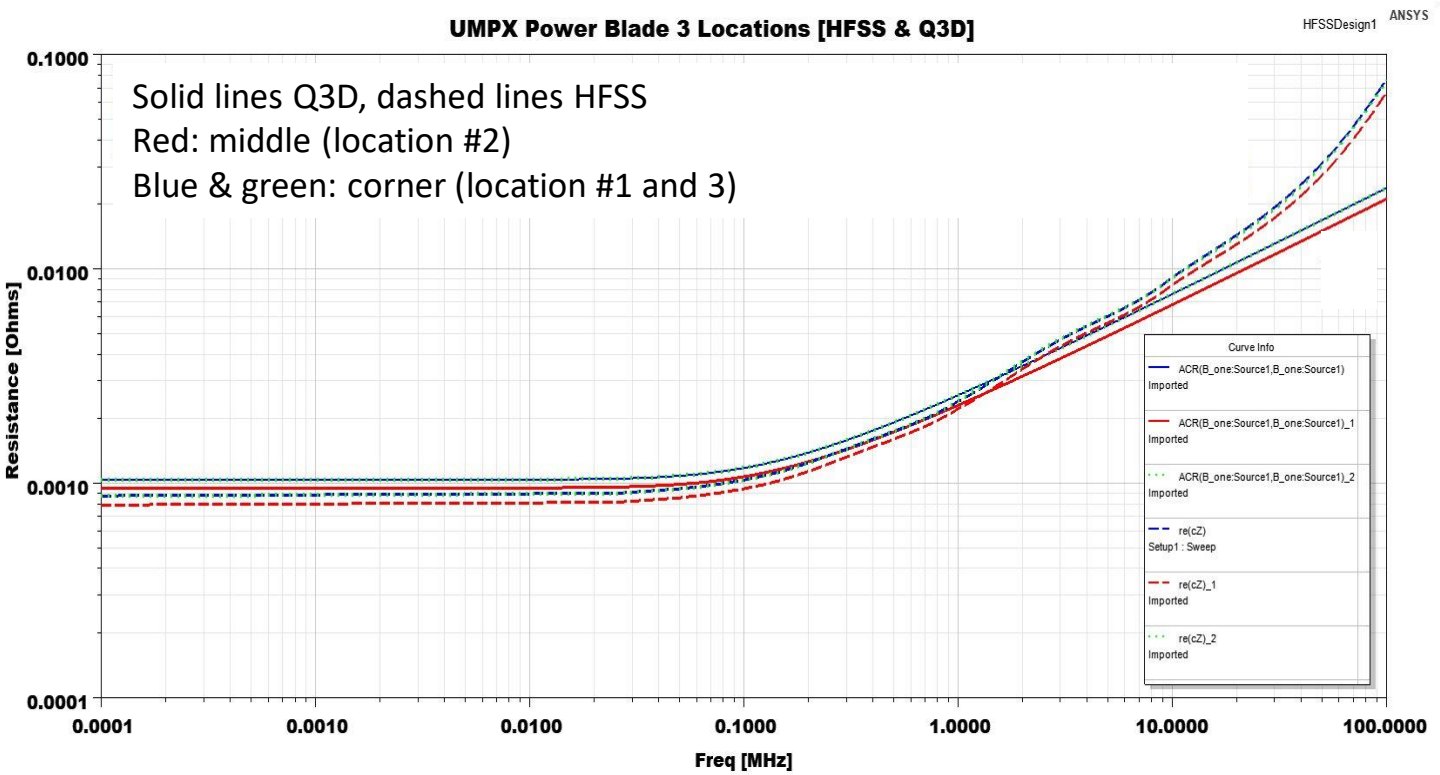

2 Blades form Series Impedance Loop




Red Dots represent 3 measurement locations

Gray plane represents shorting solder attached to bottom of blades

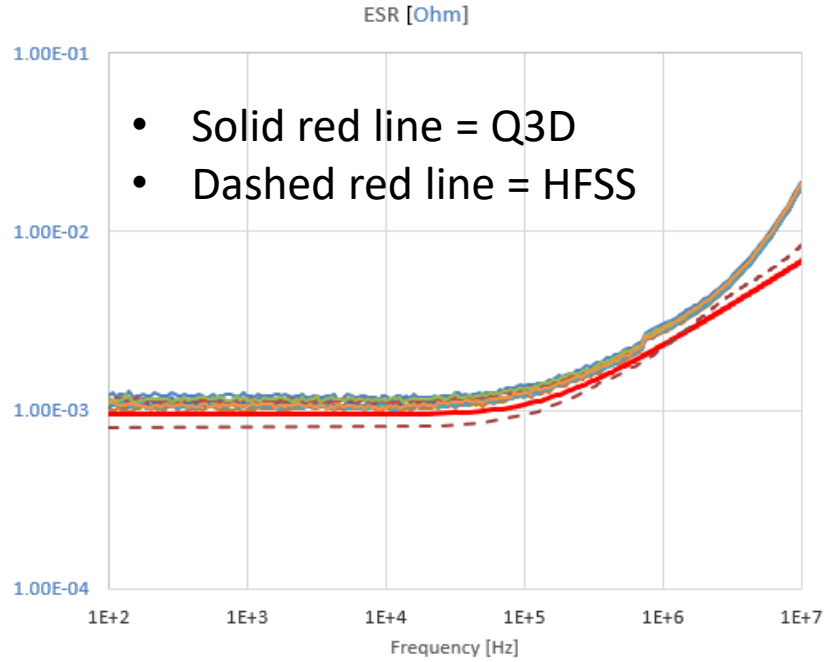
# Power Connector: Simulation Resistance Results

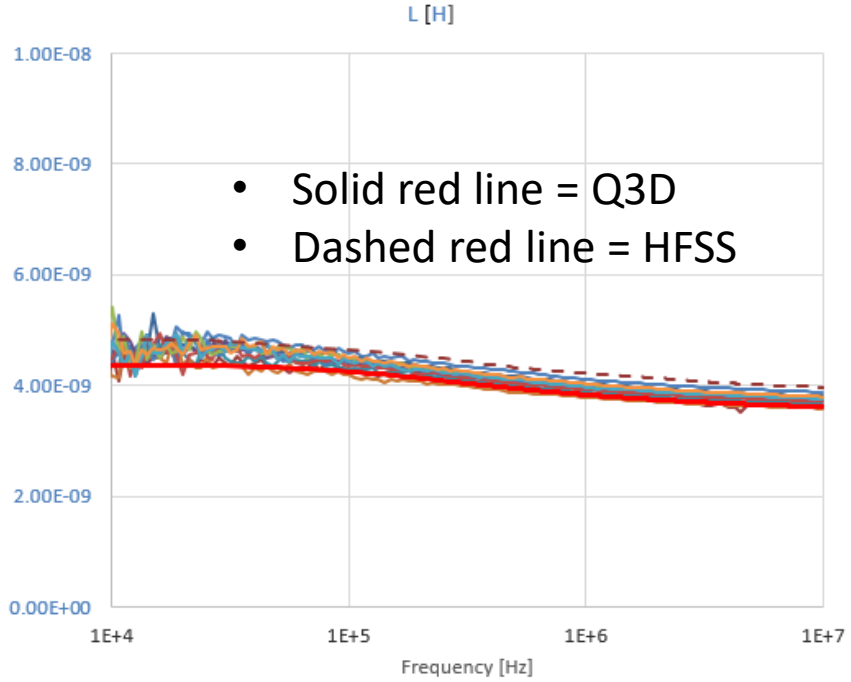



- Location #1 and #3 are symmetric, thus results should be identical
- Both tools show delta for Location #2

# Power Connector: Simulation to Measurement Correlation

- Q3D, HFSS resistance and inductance plots compared to measurements

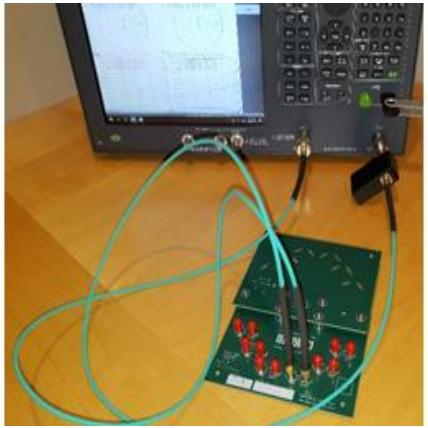


# Evaluation Board Measurement setup

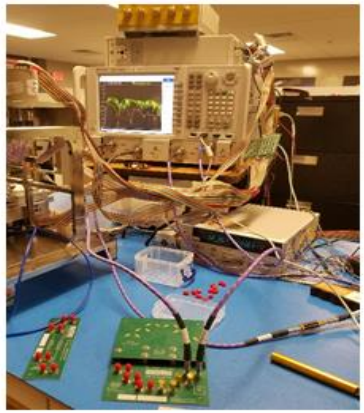
- In addition to the connector which is measured, the board contains SMA connectors, vias, and transmission lines which will be de-embedded for correlation
- Unlike high-speed interconnects, power structures must be measured down to DC. In order to extend the frequency range to high frequencies, 2 VNAs in 3 different setups were used for the frequency ranges noted below

100Hz – 1MHz

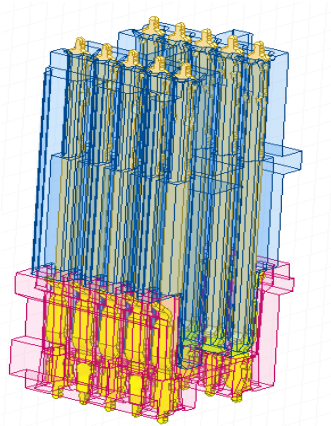


1KHz - 100MHz

10MHz – 40GHz

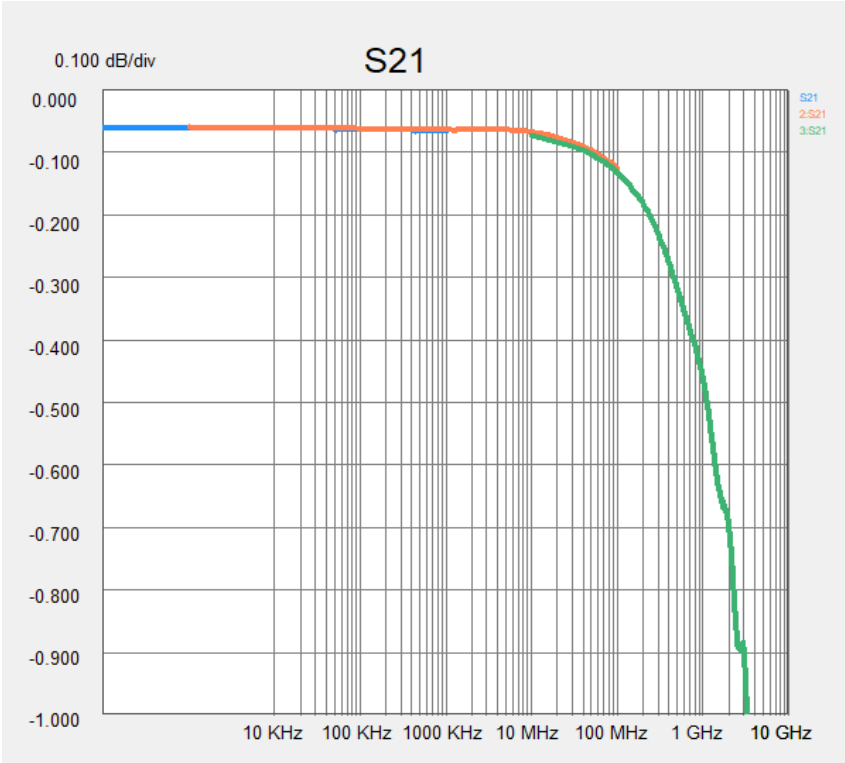


Connector 3D Model



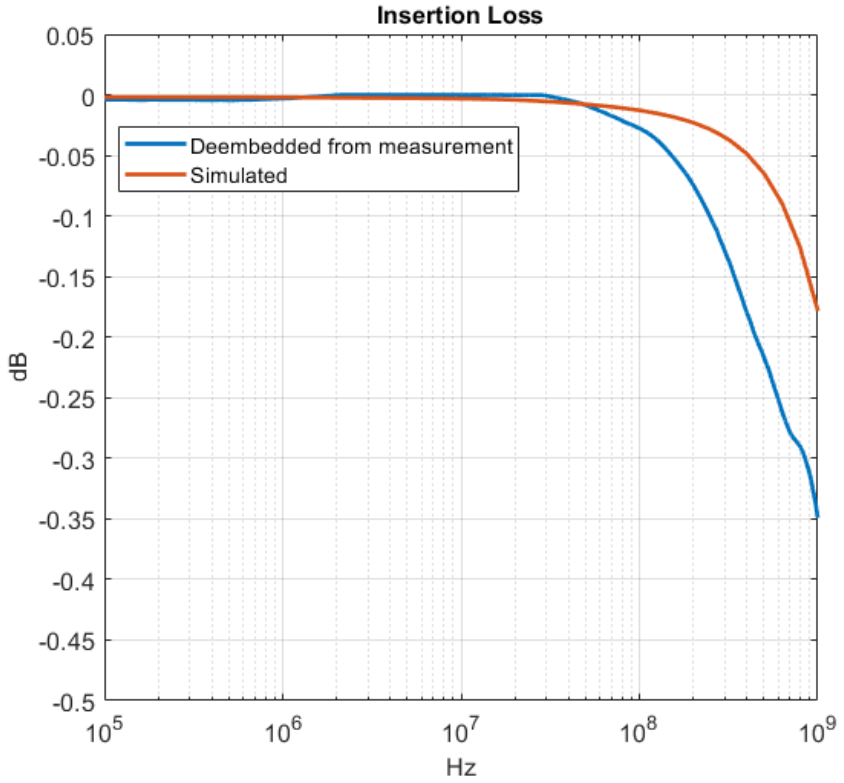
# Evaluation Board Measurement Results

- The plot shows the through measurement of the evaluation board
- The different colored line represent the results from the 3 different VNAs.
- Prior to de-embedding, the 3 VNA results were stitched together into a single curve. The data in the overlap region was weighted to create a single smooth curve across the entire frequency range.
- Separate calibration traces were also measured (and stitched together), and they were used to de-embed the connector itself.



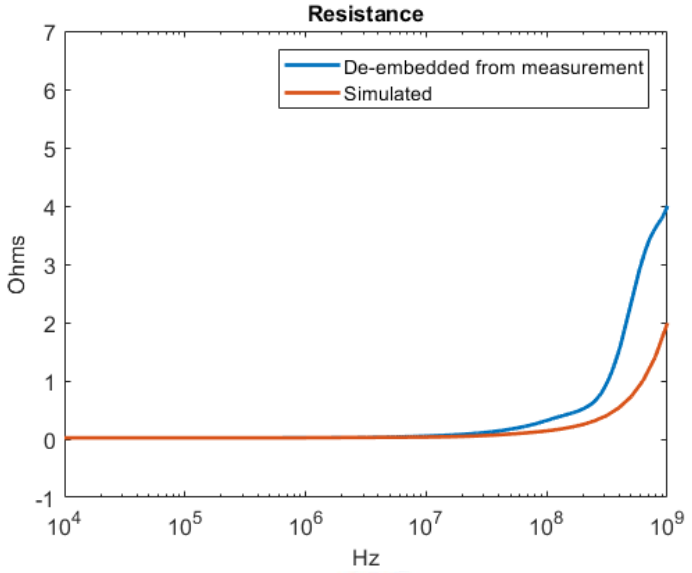
# Simulation to Measurement Correlation: Insertion Loss

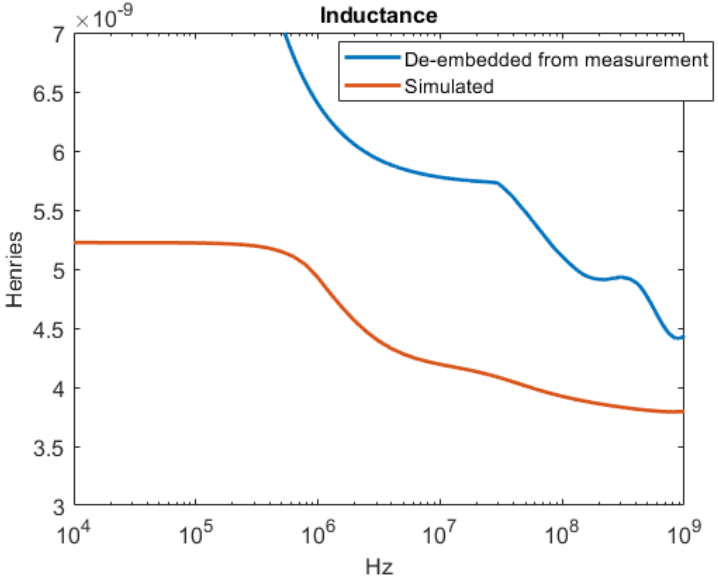
- Insertion loss correlates well up to 100MHz.
- Beyond 100MHz, the de-embedded data is more lossy but follows a similar trend vs. simulation



# Simulation to Measurement Correlation: R(f), L(f)

- The resistance correlation mirrors the insertion loss correlation shown on the previous slide. Good correlation up to 100MHz, but then the de-embedded data shows more resistance
- The de-embedded inductance is problematic below 1MHz (the region where simulations shows roughly constant inductance.) Beyond 1MHz, it shows a similar trend vs. simulation but with 0.5-1nH offset.



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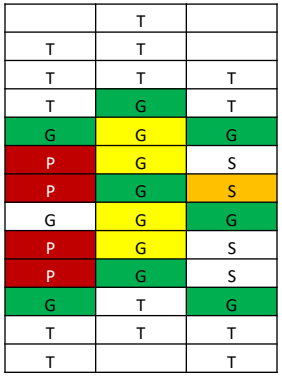
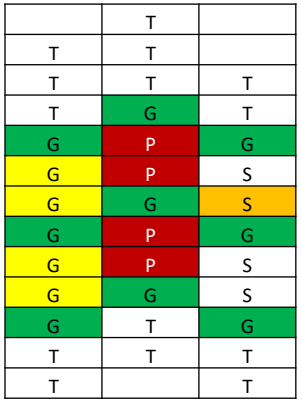
# Example: Open Pin Field Connector for Pow & Sig

- **Which is better?**



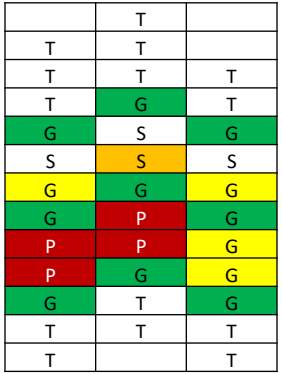

1

Pow-gnd-sig



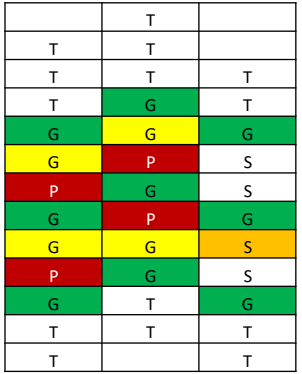

2

Gnd-pow-sig




3

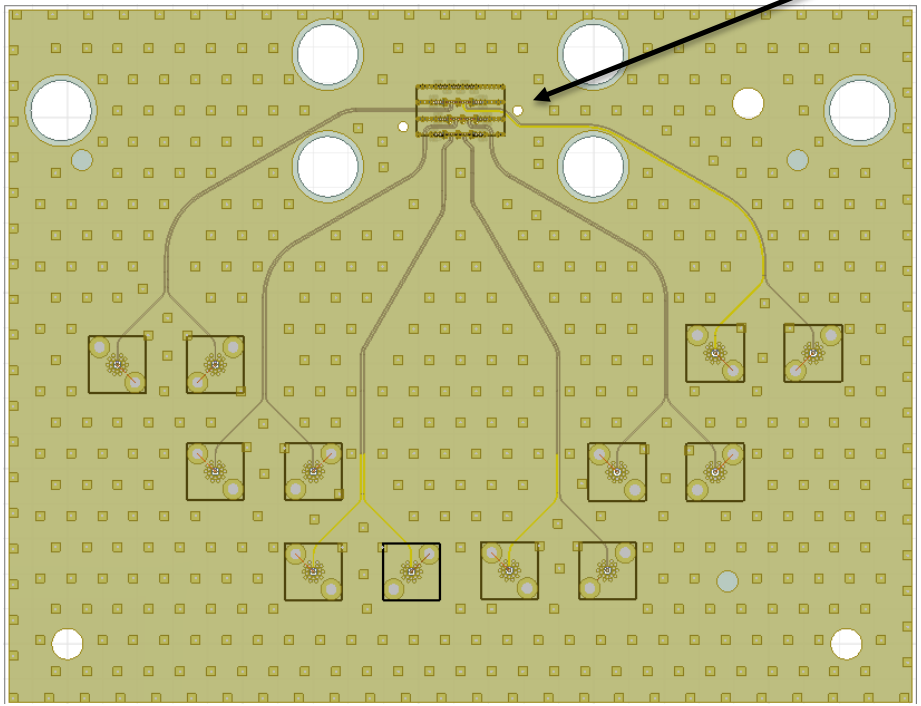
Power bundle

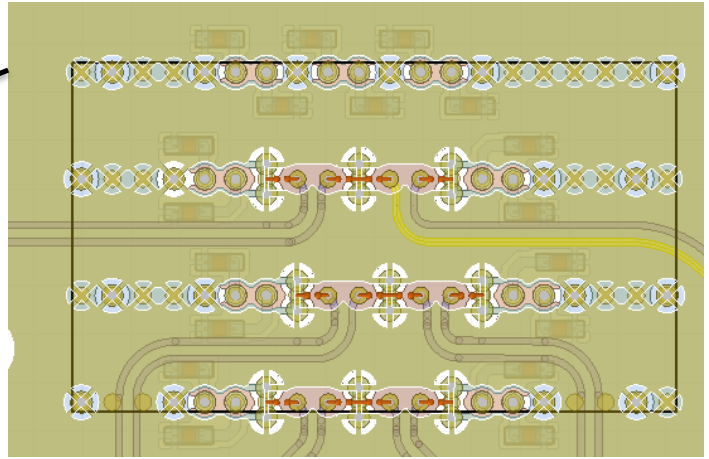



4

Pow-gnd inter-leaving

# Test Vehicle Setup

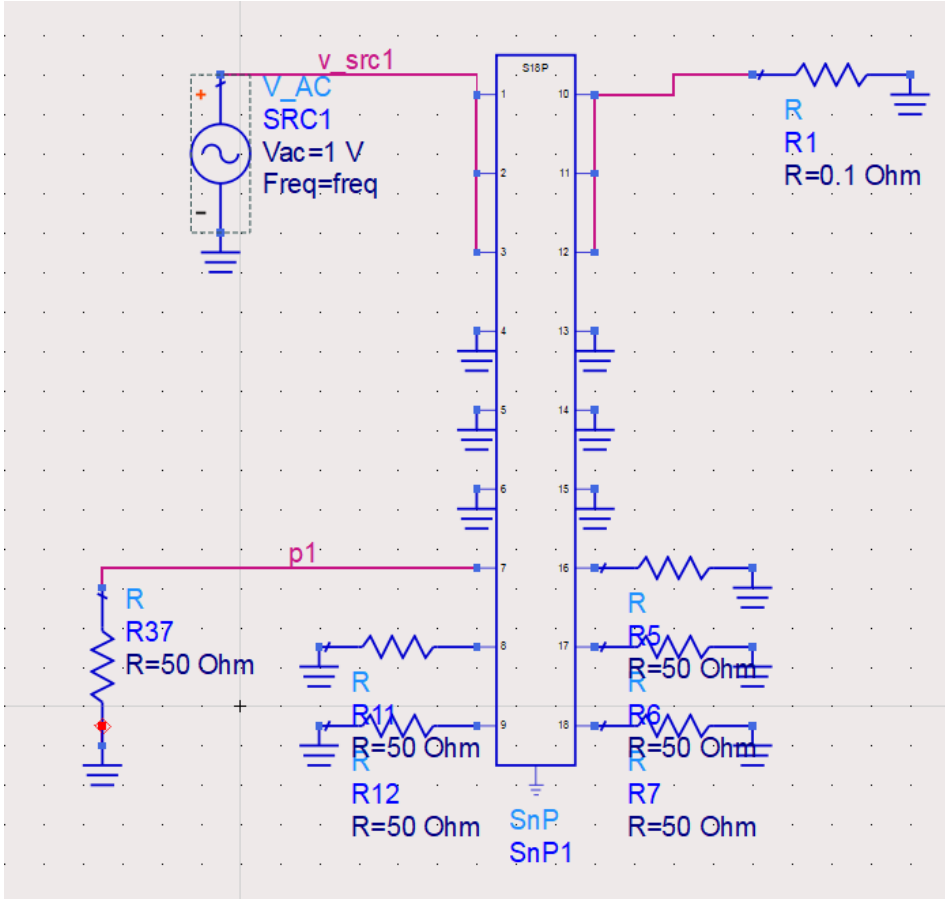




- 6 layers board .
- Blind via.
- DUT: open pin filed mezzanine connector.
- Same board as de-embedded connector measurement from earlier

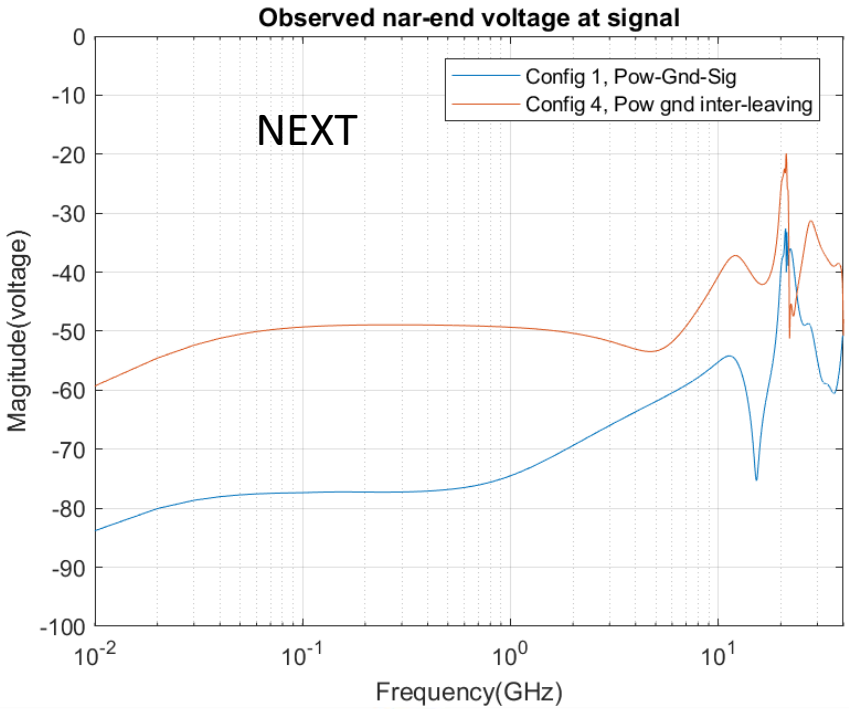
# Methodology

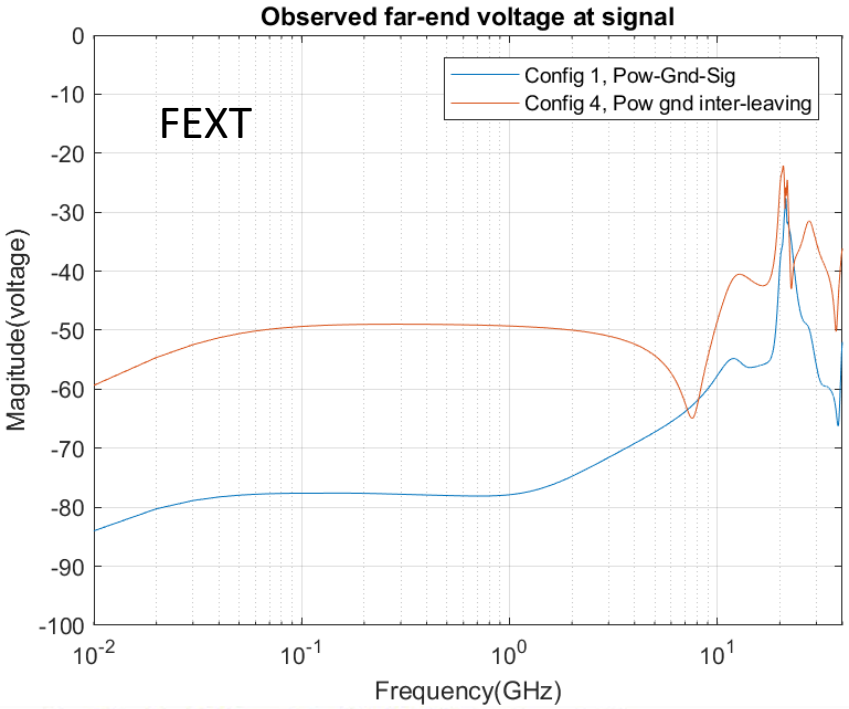
- 1V at the power pins.
- 0.1Ω as loading.
- User assigned ground are grounded.
- Signal pins are terminated by 50Ω.
- We use ADS for verification only.
- Actual simulation is done in Matlab by solving the modified nodal analysis (MNA) matrix.



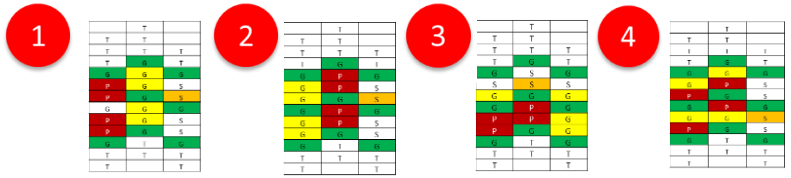
# Connector Only Crosstalk is Minimal

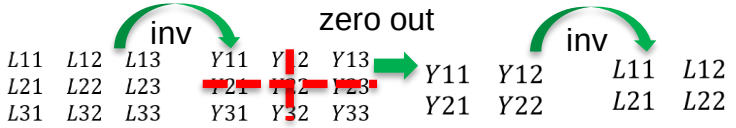
- Take config 1 (pow-gnd-sig) and config 4 (pow gnd inter-leaving) as an example.

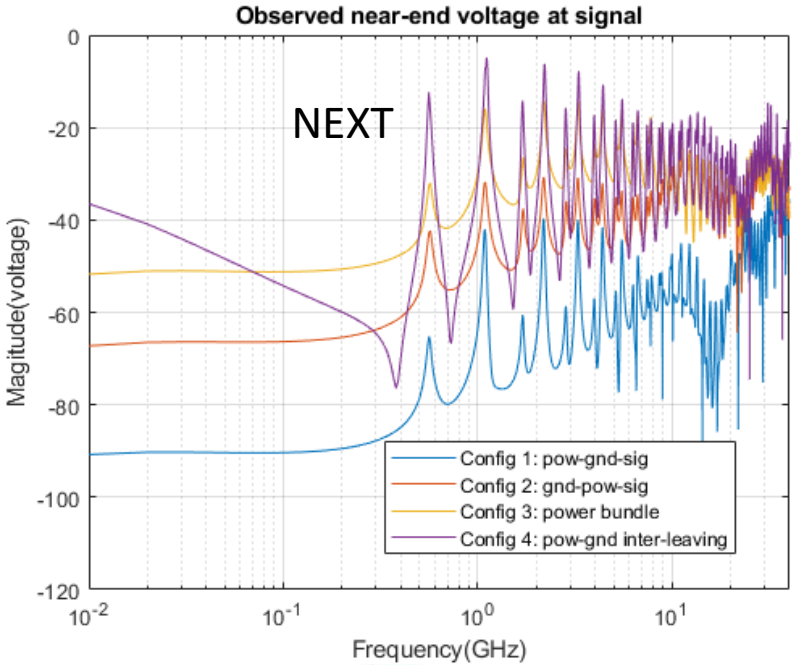


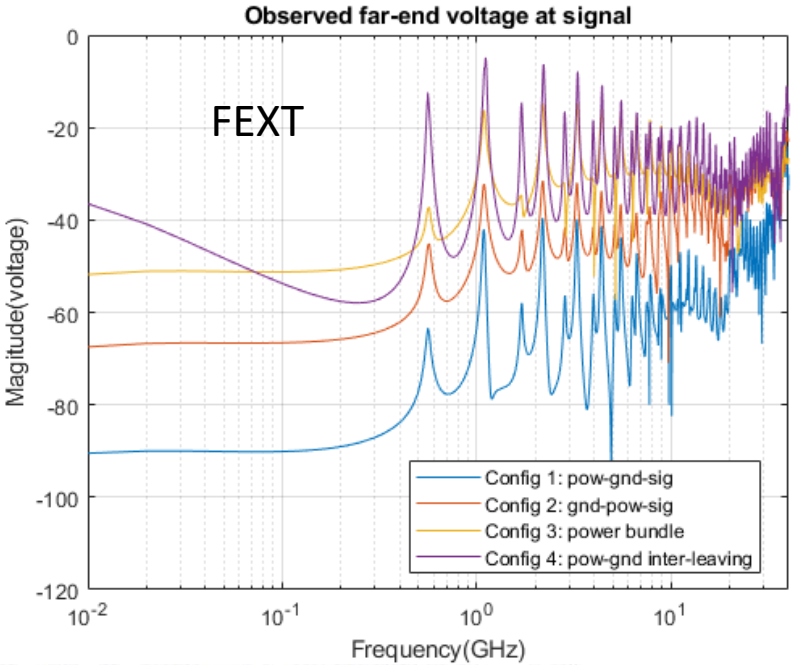
# Board + Connector + Board, Config 1 to 4



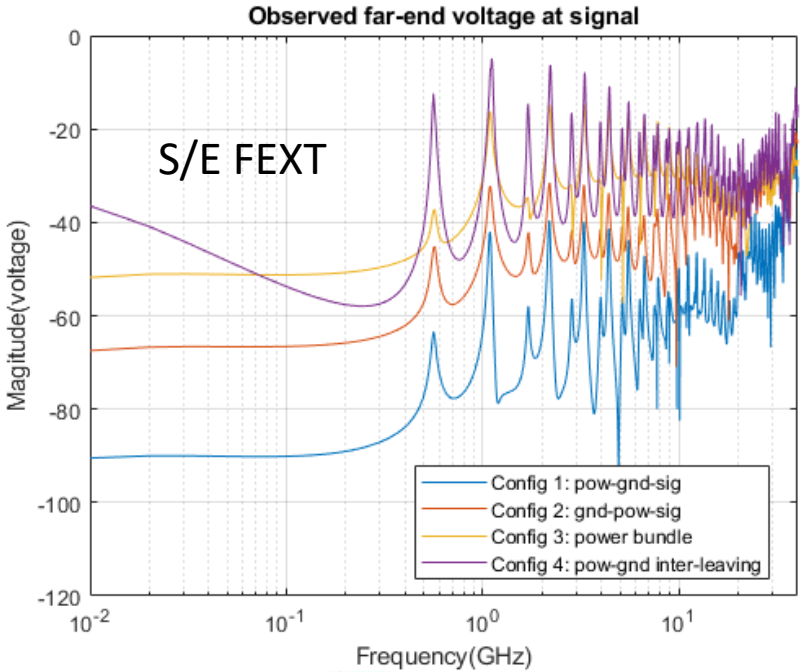



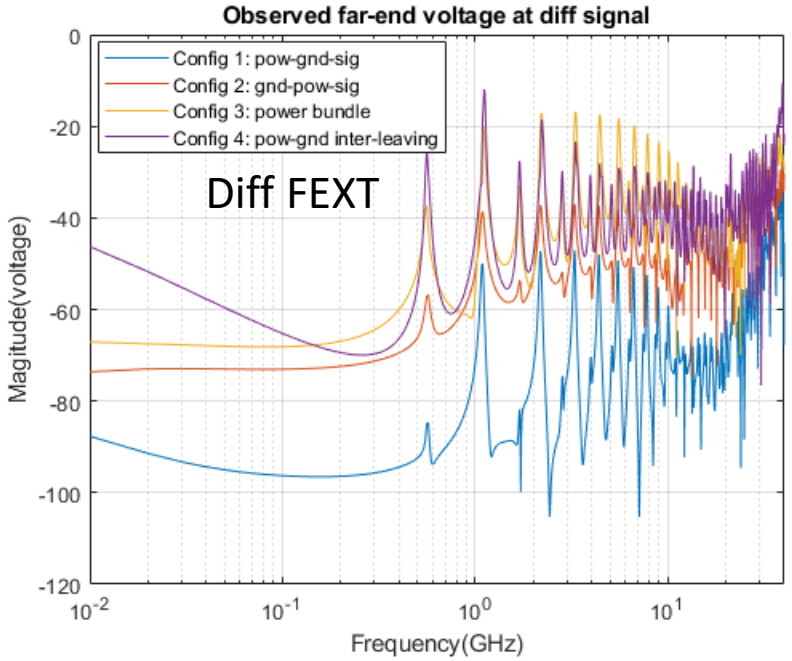

Single-ended



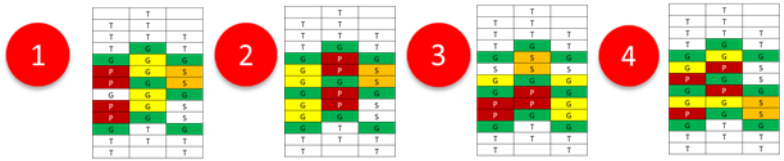
# Do Differential Signals Minimize the Crosstalk?


- **The power induced crosstalk is like a common mode noise.**

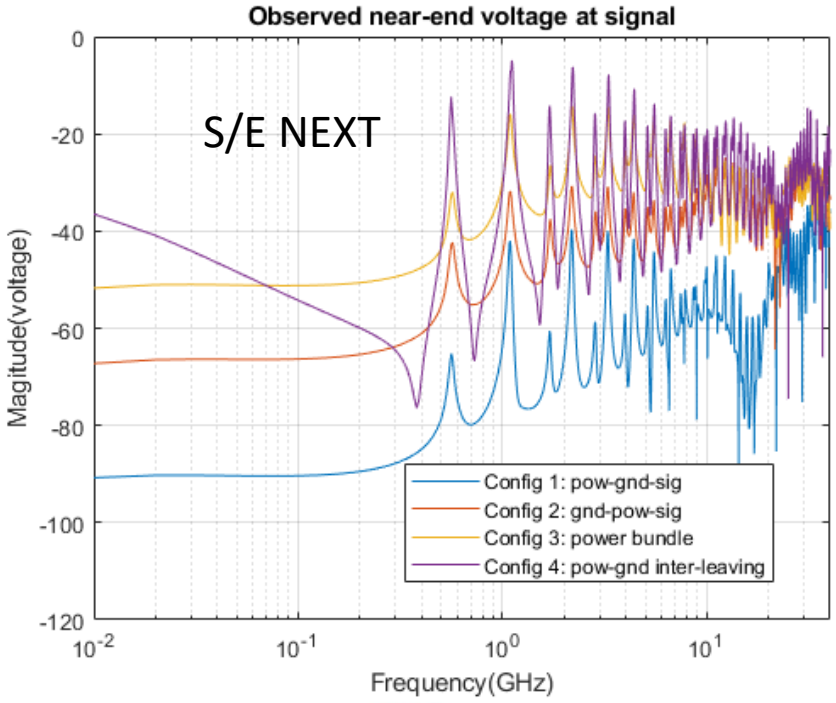


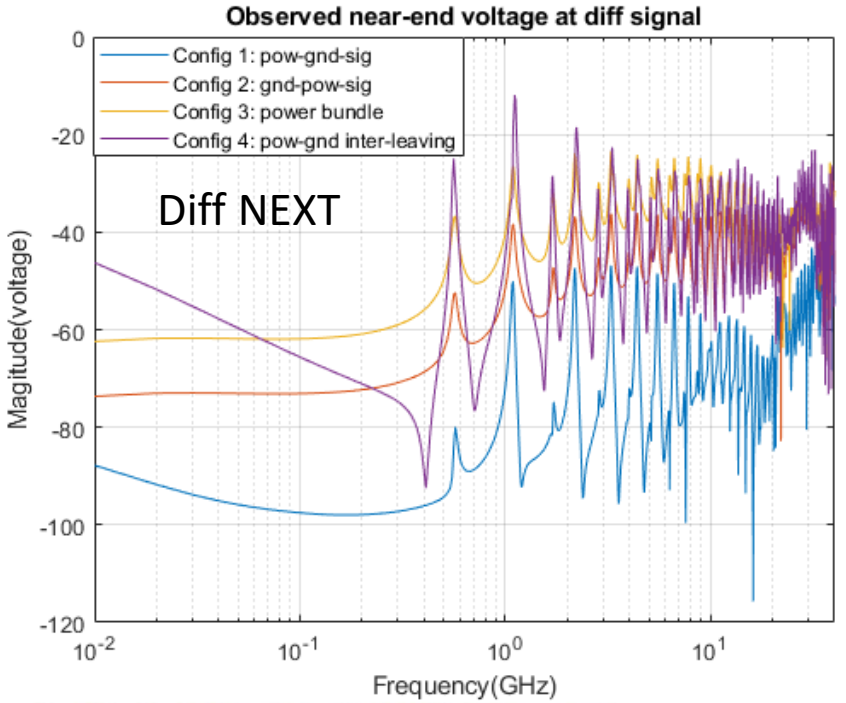



# Board + Connector + Board, Config 1 to 4



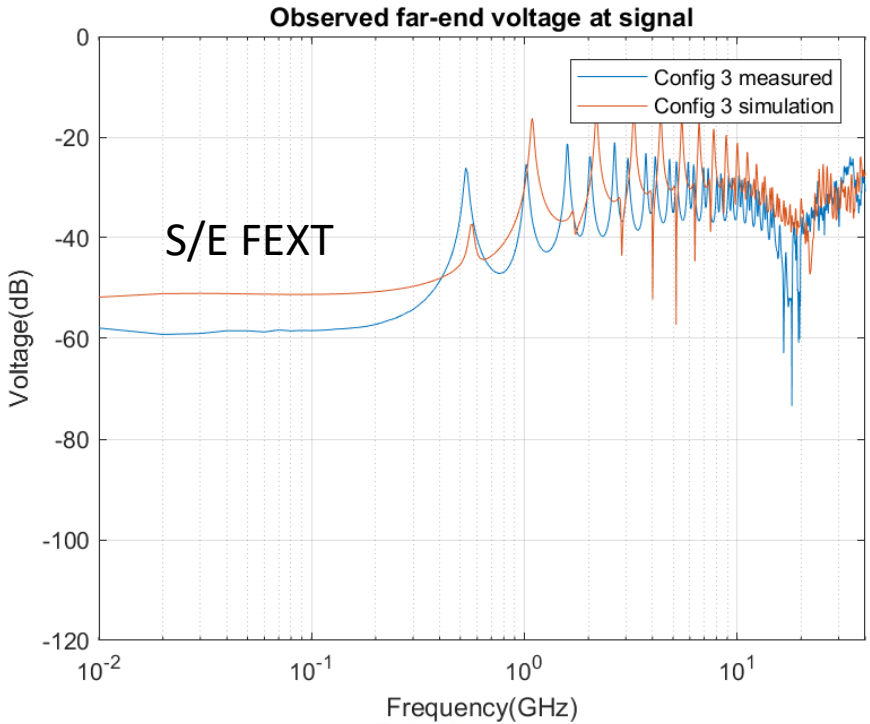

- **The power induced crosstalk is like a common mode noise.**

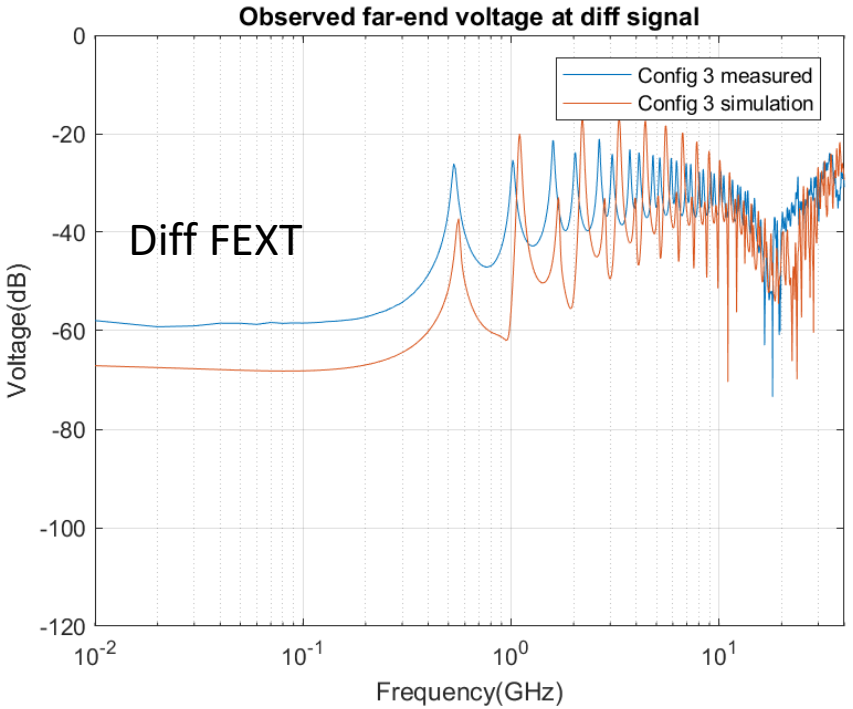


# Simulation & Measurement Correlation

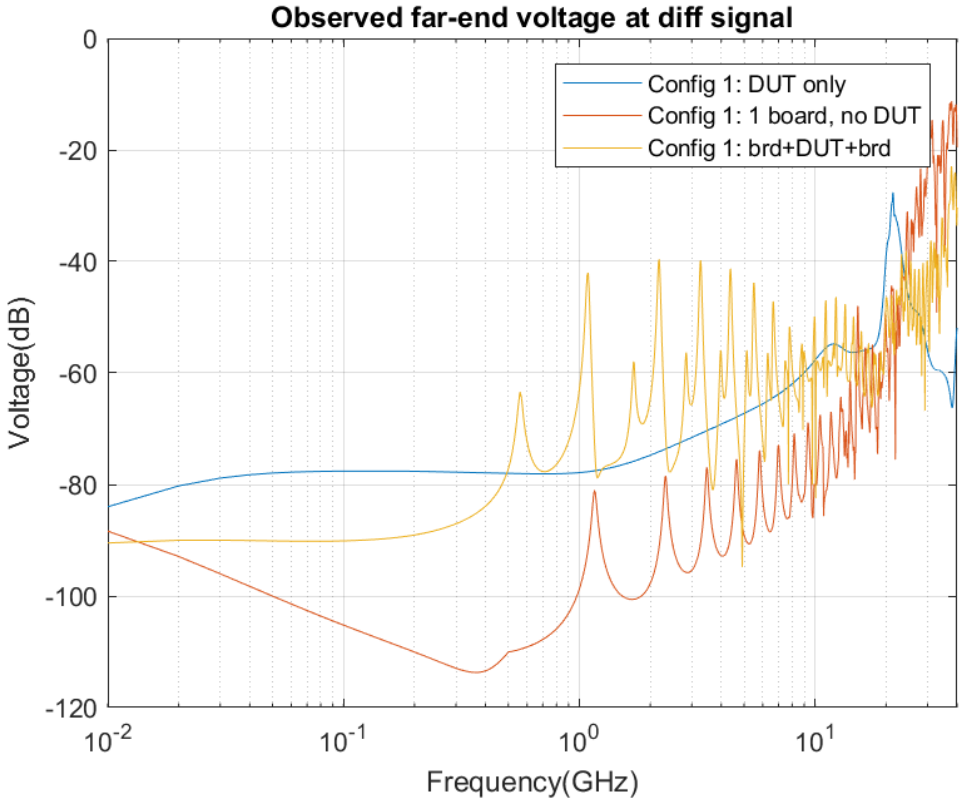
- Measured magnitude is more subdued.



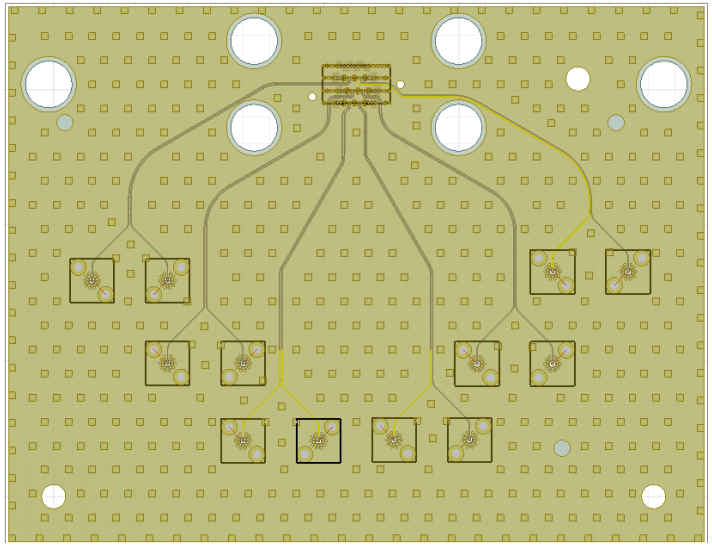



# Spikes in FEXT?

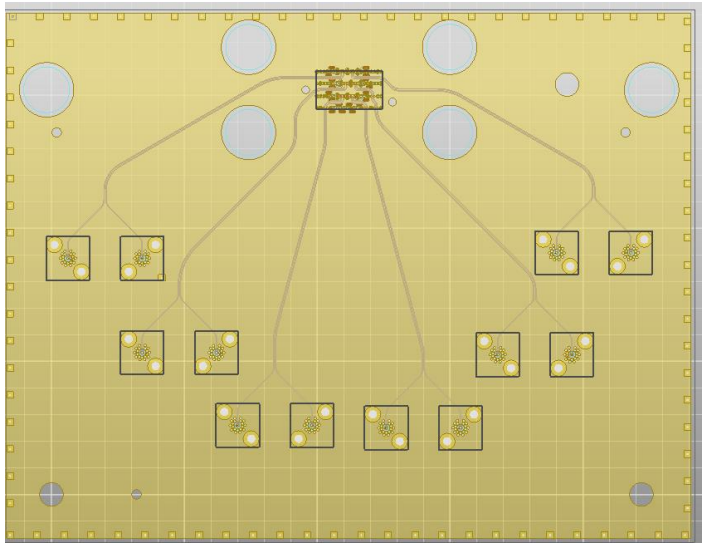
- From the board!
- With just one board, we also observe spikes in FEXT.
- With the connector, it simply shifts the curve up.



# What If Stitching Vias Are Removed?



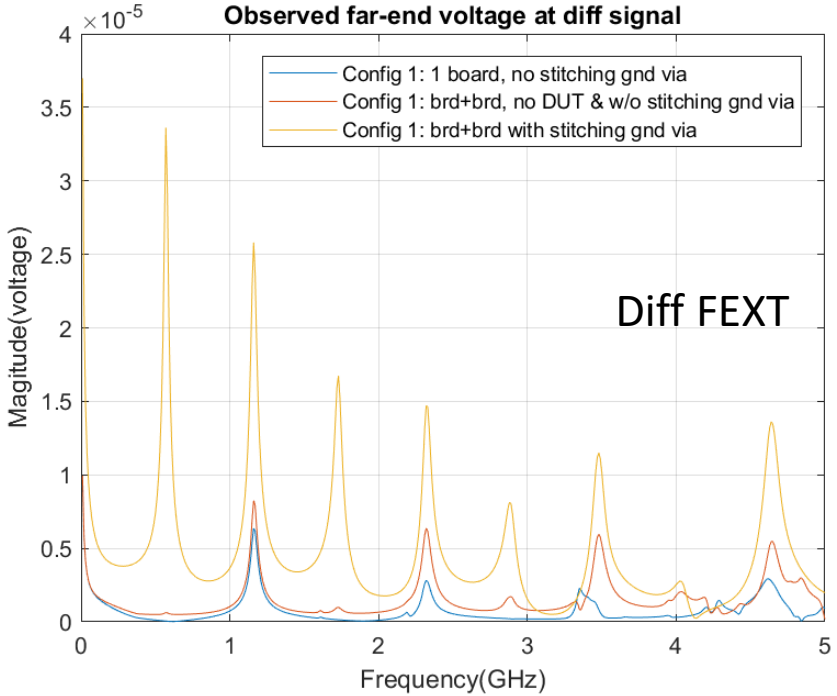
With ground stitching via

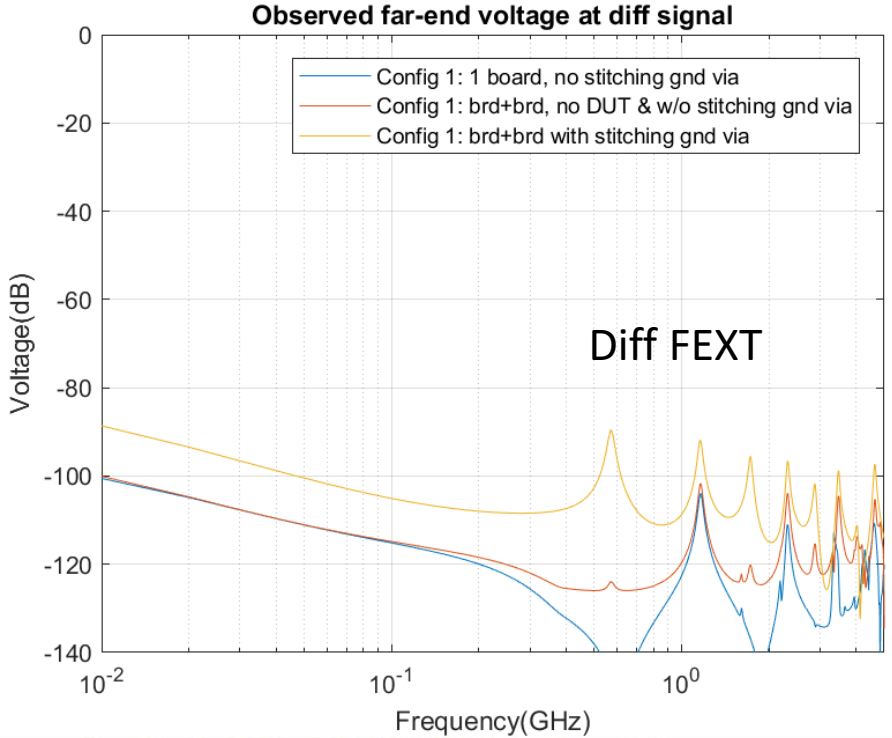


Ground stitching vias removed except at the edge

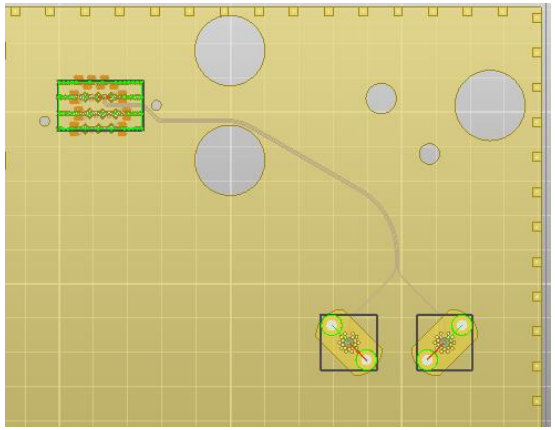
# Not From The Plane Resonance…

- With or without stitching vias, it still pick up the spikes.

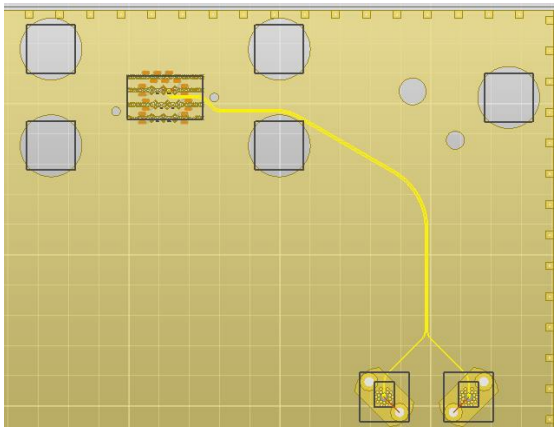


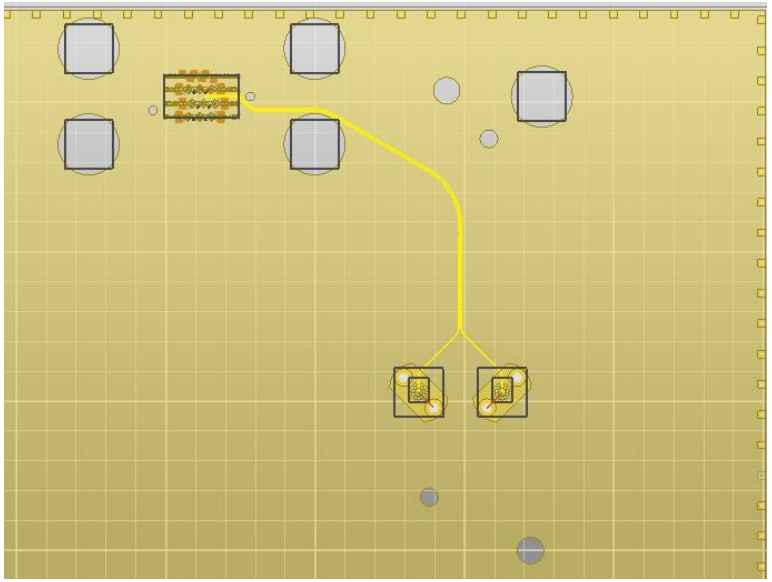
# Further Investigation With Just One Pair



Base case, 1 pair



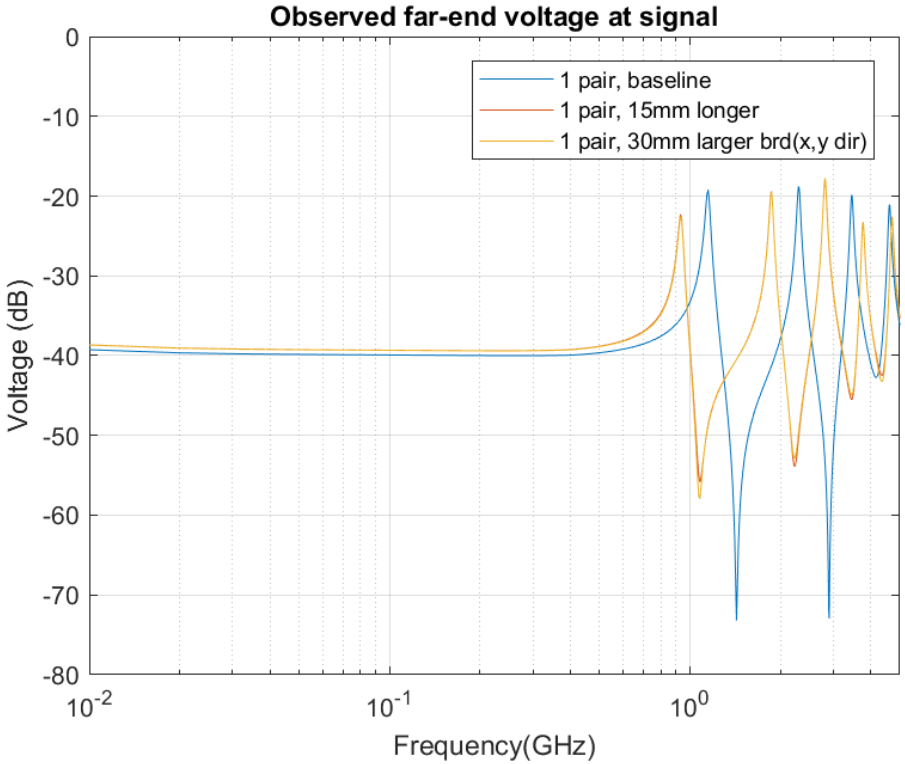
One pair + 15mm longer



One pair + 15mm longer &
board is 30mm larger in x,y dir

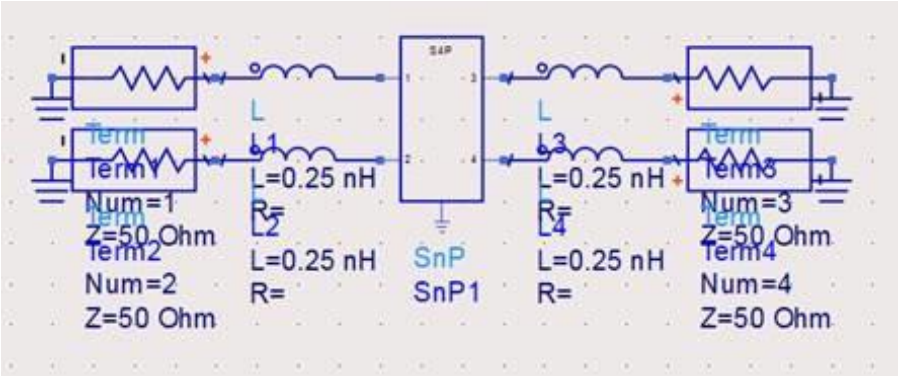
# One Pair Investigation Result

- Not from the plane.
- Longer trace shifts to lower frequency but there is still spike to begin with?

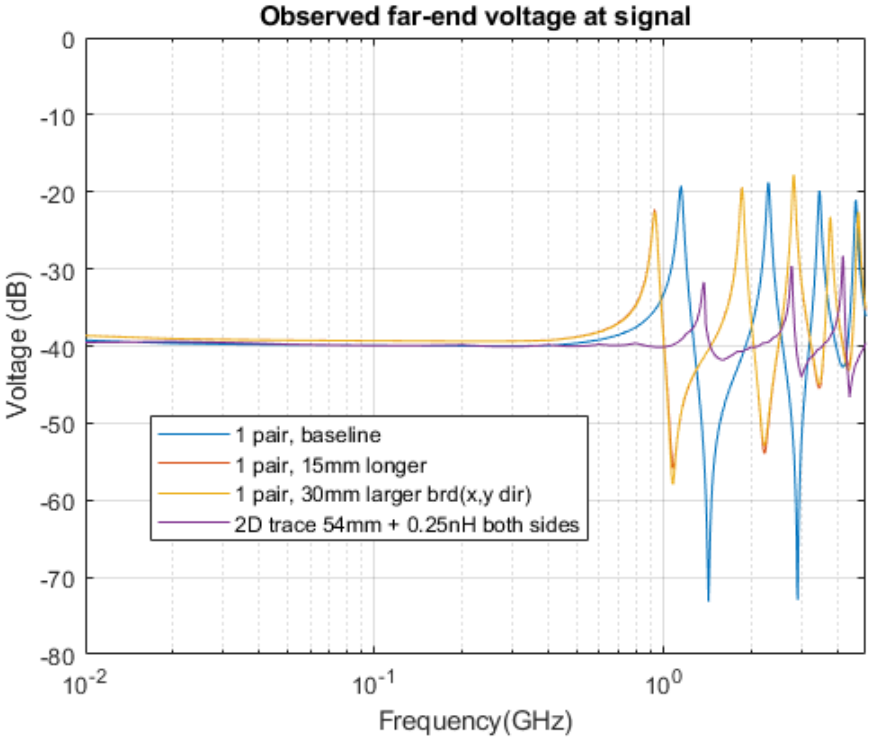


# What About Via Discontinuities?

- Adding 0.25nH to mimic the via inductance.

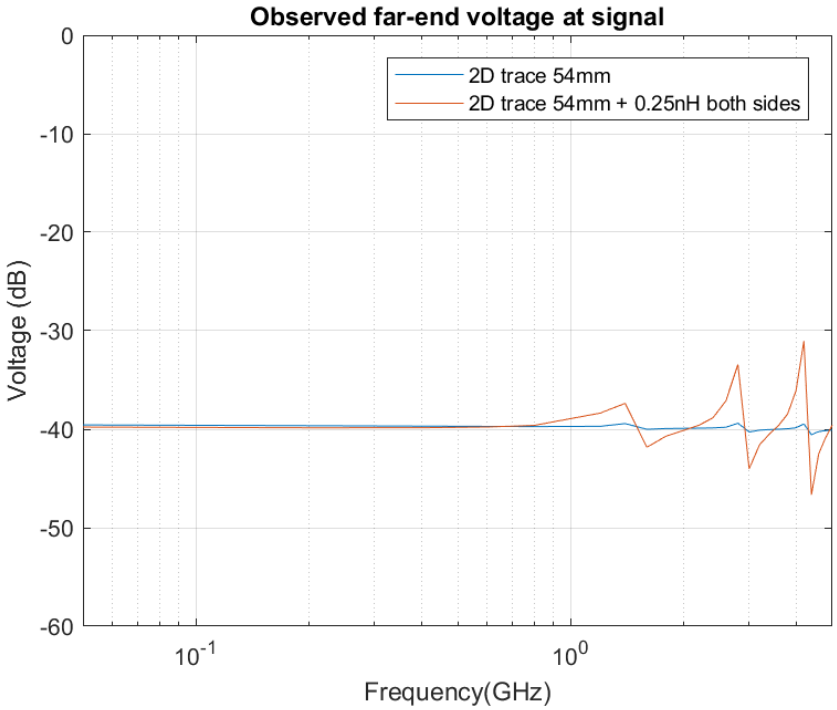


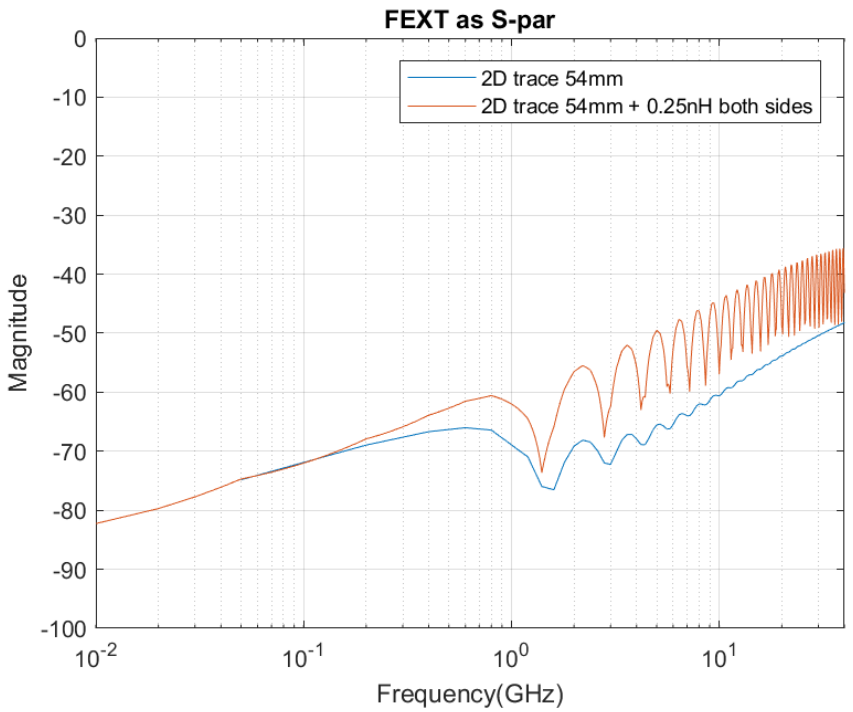

$$Lvia \approx 5.08h\left[ln\frac{4h}{d}+1\right]nH$$



# 2D Trace vs. 2D Trace + Inductance

- Adding the inductance (discontinuity) creates the spikes!



# Outline

- Introduction & Background
- Establishing Baseline
- Component Level:  DC to High Frequency Simulation to Measurement Correlation
- System Level: SI and PI Interaction
- Conclusions

# Conclusions

- Simulation tools are capable of predicting low – high frequency resistance and inductance profiles.
- Isolated connector measurements correlate well vs. simulation.
- De-embedded connector measurements show fair correlation.  Resistance is good, but de-embedded inductance was problematic at low frequency for SI test board.
- Power induced crosstalk is both board and pinout dependent.
  - Interleaved power/gnd pin assignments are not optimal for signal to power crosstalk
  - In this particular test board setup, power-gnd-signal pinout gives the minimal induced crosstalk.
- Crosstalk in the connector is accentuated by the board crosstalk.
- Minimizing reflection discontinuities is essential for resonance free crosstalk.

# Acknowledgement

The authors wish to thank

- Scott McMorrow of Samtec
- Jim DeLap of Ansys
- David Michaud of Samtec
- Jean-Remy Bonnefoy of Samtec

for their valuable comments, help and support.

# Thank you!

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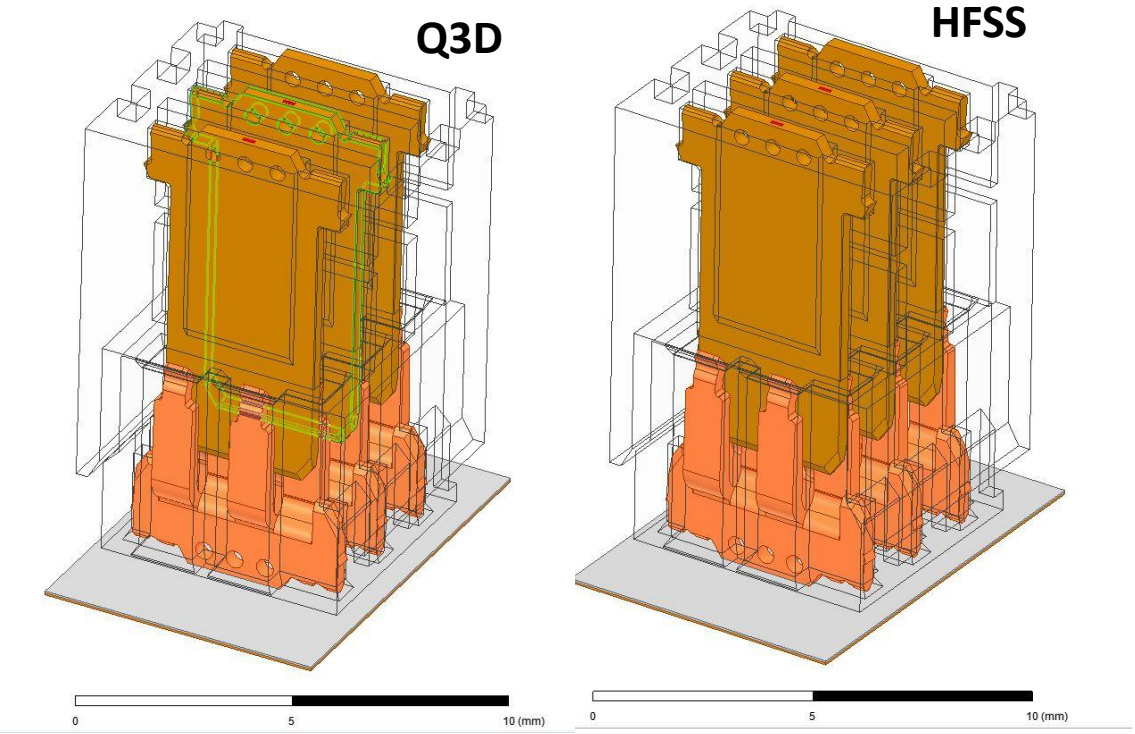
## QUESTIONS?

# Backup

# Identical CAD for Simulation Correlation

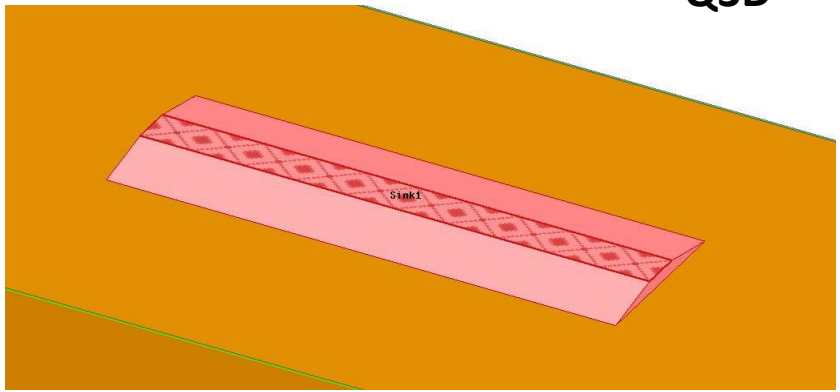
- Same exact geometry
- Same material properties
- Only difference is slightly different terminal geometry.
- Q3D … Source and Sink on faces
- HFSS … Circuit Ports on edge



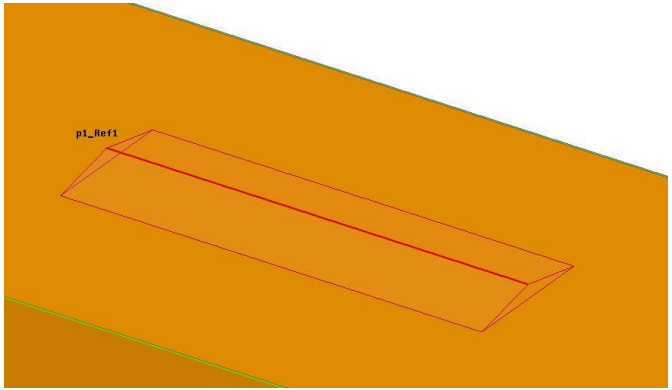
# Difference in Port Definition Geometry

- .0025 mm in shift in path length

**Q3D**




**HFSS**

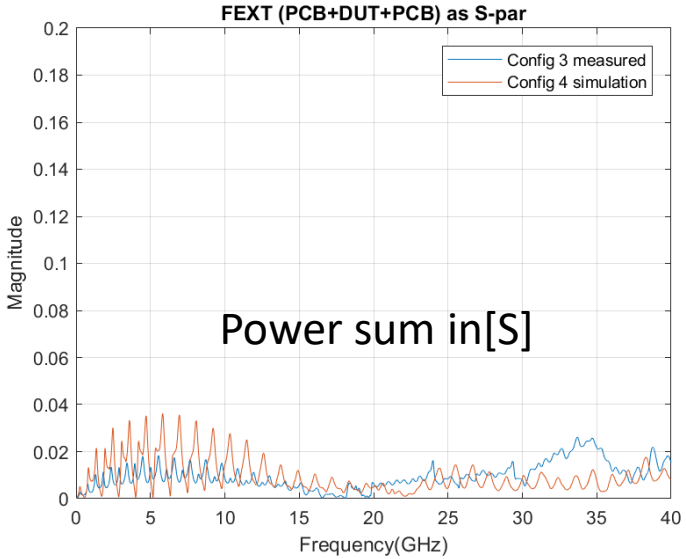


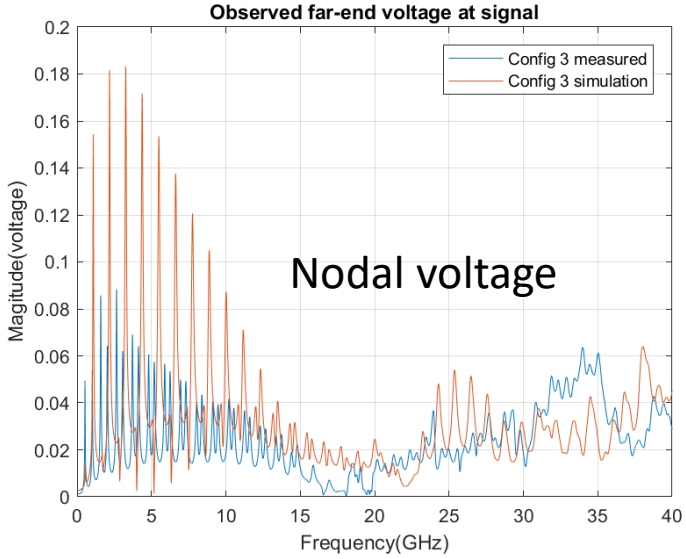
# Side Notes on the Metric

1) S-parameter assumed 50Ω at each port.

2) Another difference is due to post-processed Y matrix:

- a) combines columns (v1=v2=…, pow pins at same V)
- b) combines rows (I1+I2+.., distributed current)



# DC Resistance of Layered Metallic Cylinder

$r_i$ = inner conductor radius

$r_o$ = outer conductor radius

$\sigma_i$ = inner conductor conductivity

$\sigma_o$ =outer conductor conductivity

$$A_i = inner\ area = \pi r_i^2$$

$$R_i = inner\ resistance = \frac{1}{A_i \sigma_i}$$

$$A_o = outer\ area = \pi r_o^2 - \pi r_i^2$$

$$R_o = outer\ resistance = \frac{1}{A_o \sigma_o}$$

$$R_t = total\ resistance = \frac{R_i R_o}{R_i + R_o}$$

For the example presented earlier, the total resistance =0.2 mOhms.
This is virtually identical to the simulated results.