PCIe 32G & 64G: System Design & Test Challenges

Panel
Thursday, January 30th, 3:45 pm

Speakers

Pegah Alavi

Senior Applications Engineer

Keysight Technologies

Pegah is a Senior Applications Engineer at Keysight Technologies, where she focuses on Signal Integrity and High Speed Digital Systems and Applications. Prior to joining Keysight Technologies, Pegah worked on system level modeling of analog and mixed signal circuits in order to best predict the overall systems performance and accurately represent each component.

Rita Horner

Senior Technical Marketing Manager

Synopsys, Inc.

Rita Horner is a Senior Technical Marketing Manager at Synopsys, with more than 25 years of experience in the area of mixed signal circuit design, ESD design, test and packaging of high speed integrated circuits for consumer, computing, and high end networking products, across a broad range of semiconductor process technologies. As a technical, product and strategic manager, she has worked on defining and managing ASSP, ASIC and Fiber Optic product lines, and has been focused on High Speed Serial Interconnect IPs. She participated and presented at multiple technical conferences, consortiums, and standards bodies including ANSI T11, IEEE 802.3, OIF, PCI-SIG and many Multi Souring Agreements. She has previous experience with Avago Technologies, Exar, Agilent Technologies, Hewlett-Packard and Intel. She holds an MSEE from the University of Tennessee, has a patent in IC packaging and has a number of technical publications.

Speakers

Tim Wig

Signal Integrity Engineer, Intel

Intel

Tim Wig joined Intel in 2001, where he works as a signal integrity engineer in a pathfinding and spec development group whose charter includes PCIe and other interconnect standards. Tim coordinates the Card ElectroMechanical (CEM) Spec document for Gen 4.0 and 5.0, and has contributed many of the signal integrity enablers that allowed PCIe to reach 16 and 32 GT/s. His primary focus is passive component, PCB, and channel level modeling, measurement, and optimization for PCIe CEM, though he also supports the M.2, U.2, and OCuLink standards. He holds a PhD in Engineering Science from Washington State University; and an a MS and BS in Electrical Engineering and a BS in Engineering Physics from the University of North Dakota. He delivered a tutorial on PCIe Gen 4.0 to DevCon 2016.

Ying Li

Senior SI/PI Engineer,

NVIDIA Corporation

She works on high-speed serial interconnect and core power distribution network design for Nivdia GPU, DGX and Tegra systems. Prior to that, she was a SI engineer at Oracle Corporation focusing on Sparc system package and board high-speed signal analysis and measurements.

Speakers

Patrick Casher

Pr. Product Development Engineer

FIT-Foxconn

Patrick Casher received his BSEE and MSEE degrees in Electrical Engineering from Illinois Institute of Technology in 1991 and 2006 respectively. For his graduate work, his concentration of study was in the areas of electromagnetics, numerical methods, and high-speed circuit design. He has been working in the connector and cable interconnect industry for 18 years. Since 2018, he has been working as a Principal Product Development Engineer for Foxconn Interconnect Technology (FIT) as a member of their US R&D team. He holds a number of patents related to connectors, high-speed cable and cable assemblies..

Steve Kroowyk

New Product and Standards SI

Samtec

Steve is involved in new high-speed connector development and PCIe standards at Samtec. His 16 years of signal integrity experience has had a focus on the design, simulation, and correlation of PCIe interconnect and I/O. Previously, Steve was the PCIe tech lead for SI in Intel's data center division during Gen3 and Gen4 development. He is an author of the book High Speed Digital Design: Design of High Speed Interconnects and Signaling and holds a MS degree from the University of South Carolina.

Speakers

Dan Froelich

Director of Systems Engineering

Tektronix

Dan Froelich joined Tektronix in November 2018. For the prior 18 years Dan worked as an Intel engineer and architect focused on specification and compliance test methodology development for USB and PCI Express standards. Dan served as co-chair of the PCI-SIG electrical workgroup and technical editor for the electrical specification for the PCIe 4.0 and PCIe 5.0 specification development. Dan also served as chair of the PCI-SIG Card Electromechanical (CEM) workgroup and technical editor from 2005 to 2018 covering the PCI Express 2.0, 3.0, 4.0 and early 5.0 CEM specification development. In addition, Dan served as co-chair of the Serial Enabling (Compliance Program) workgroup from 2007 - 2018 and served as technical editor and technical lead or developer on many of the test specifications and tools used by the PCI-SIG compliance program. Dan also won an Intel Achievement Award as the overall technical lead on the USB 2.0 industry compliance program and wrote the USB 3.0 hub and isochronous protocol specifications. Dan Froelich graduated with honors and high distinction from Harvey Mudd College in 1996 with a BS in Physics. Dan holds 7 US patents with several more applications pending.

Rick Eads

Principal PCIe Program Manager

Keysight Technologies

Rick Eads is a principal program manager at Keysight Technologies with expertise in technical/industrial marketing of test and measurement tools and electronic design automation software in the computer, semi-conductor, communications, and storage industries worldwide. Rick's specialty is precision product and solution definition. He provides technical leadership in driving standards within industry organizations for PCI Express, CCIX, GenZ, OCP, NVM Express, CEI 4.0, IEEE 802.3, ExpressCard, DDR, SATA, and InfiniBand. He markets test and measurement products covering oscilloscopes and associated compliance software tools, vector network analyzers, bit error ratio testers (BERTs) and EDA tools. Rick earned a MBA from the University of Colorado and holds a BSEE from Brigham Young University with an emphasis on digital design and computer architecture. Rick actively contributes to the development of the PCIe physical layer BASE, CEM, and Test specifications and has led electrical Gold Suite testing at PCI-SIG workshops worldwide since 2004.

Agenda

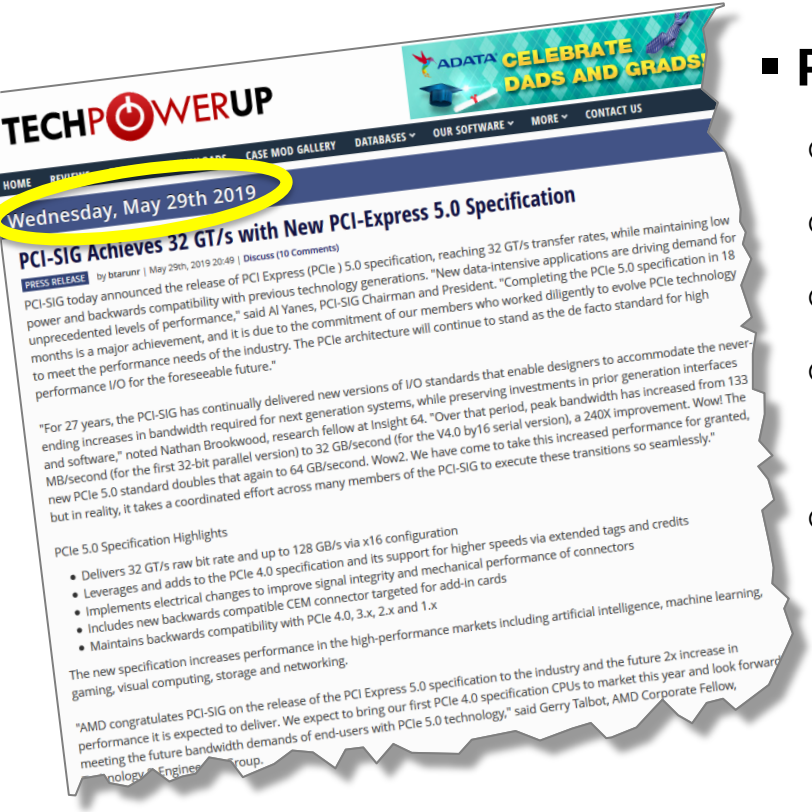
- PCI Express Migration PCIe 5.0 @ 32GT/s → PCIe 6.0 @ 64GT/s – Rita Horner
- PCIe simulation Challenges: From NRZ to PAM4 – Pegah Alavi
- Improved PCB for Connector – Tim Wig
- 32G and 64G Simulated Channels – Ying Li
- Integrated Crosstalk for Components – Patrick Casher
- Components and Cables – Steve Krooswyk
- PCIe Test Challenges – Dan Froelich
- PCIe @ 32G and 64G Test Challenges – Rick Eads

PCI Express Migration
PCIe 5.0 @ 32GT/s ➔ PCIe 6.0 @ 64GT/s

Rita Horner

Technical Marketing Manager, Synopsys

PCI Express 5.0 @ 32GT/s Specification Rev. 1.0



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Wednesday, May 29th 2019

PCI-SIG Achieves 32 GT/s with New PCI-Express 5.0 Specification

PRESS RELEASE by btarunr | May 29th, 2019 20:49 | Discuss (10 Comments)

PCI-SIG today announced the release of PCI Express (PCIe) 5.0 specification, reaching 32 GT/s transfer rates, while maintaining low power and backwards compatibility with previous technology generations. "New data-intensive applications are driving demand for unprecedented levels of performance," said Al Yanes, PCI-SIG Chairman and President. "Completing the PCIe 5.0 specification in 18 months is a major achievement, and it is due to the commitment of our members who worked diligently to evolve PCIe technology to meet the performance needs of the industry. The PCIe architecture will continue to stand as the de facto standard for high performance I/O for the foreseeable future."

"For 27 years, the PCI-SIG has continually delivered new versions of I/O standards that enable designers to accommodate the never-ending increases in bandwidth required for next generation systems, while preserving investments in prior generation interfaces and software," noted Nathan Brookwood, research fellow at Insight 64. "Over that period, peak bandwidth has increased from 133 MB/second (for the first 32-bit parallel version) to 32 GB/second (for the V4.0 by16 serial version), a 240X improvement. Wow! The new PCIe 5.0 standard doubles that again to 64 GB/second. Wow2. We have come to take this increased performance for granted, but in reality, it takes a coordinated effort across many members of the PCI-SIG to execute these transitions so seamlessly."

PCIe 5.0 Specification Highlights

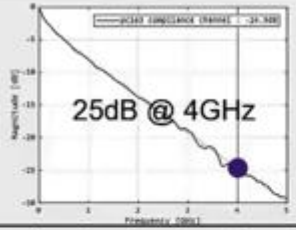
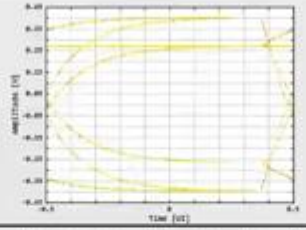
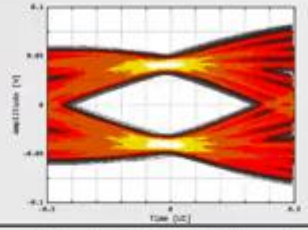
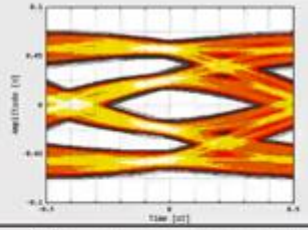
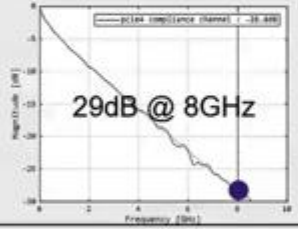
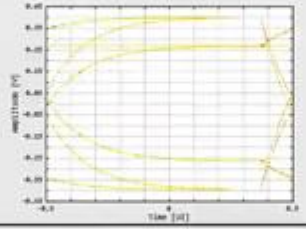
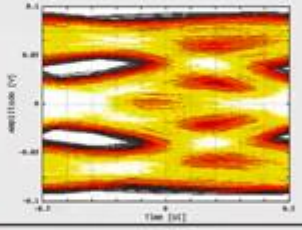
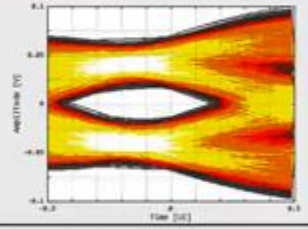
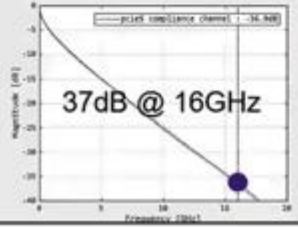
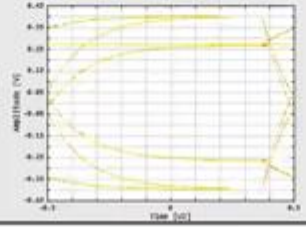
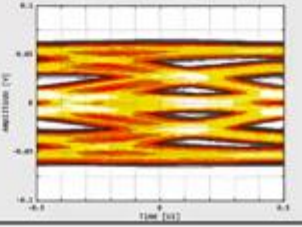
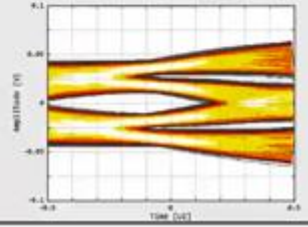
- Delivers 32 GT/s raw bit rate and up to 128 GB/s via x16 configuration
- Leverages and adds to the PCIe 4.0 specification and its support for higher speeds via extended tags and credits
- Implements electrical changes to improve signal integrity and mechanical performance of connectors
- Includes new backwards compatible CEM connector targeted for add-in cards
- Maintains backwards compatibility with PCIe 4.0, 3.x, 2.x and 1.x

The new specification increases performance in the high-performance markets including artificial intelligence, machine learning, gaming, visual computing, storage and networking.

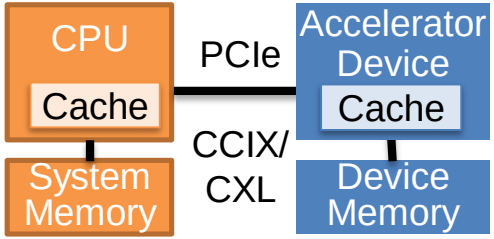
"AMD congratulates PCI-SIG on the release of the PCI Express 5.0 specification to the industry and the future 2x increase in performance it is expected to deliver. We expect to bring our first PCIe 4.0 specification CPUs to market this year and look forward meeting the future bandwidth demands of end-users with PCIe 5.0 technology," said Gerry Talbot, AMD Corporate Fellow,

- **PCI-SIG PCIe 5.0 specification**
  - Announced June 2017
  - 0.5 spec. December 2017
  - 0.7 spec. May 2018
  - 0.9 spec. November 2018
    - ➔ *1st PCIe 5.0 PHY Demo @DesignCon Jan. 2019*
  - 1.0 spec. released May 29, 2019
    - ➔ *1st Live H/W Interoperability June 2019*
    - ➔ *Across broad range of channels, connectors, cables, PCB traces, and verified w/ broad range of T&M equipment, VIP and protocol analyzers*

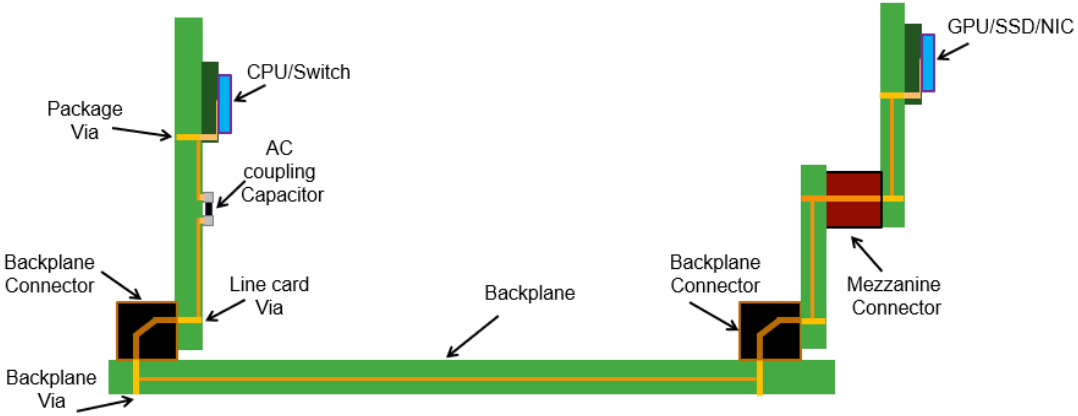
PCIe 5.0 @32GT/s is the Most Difficult NRZ Spec. Channel

	Channel	TX Eye	RX AFE Eye	RX DFE Eye
PCIe 3.0				
PCIe 4.0				
PCIe 5.0				

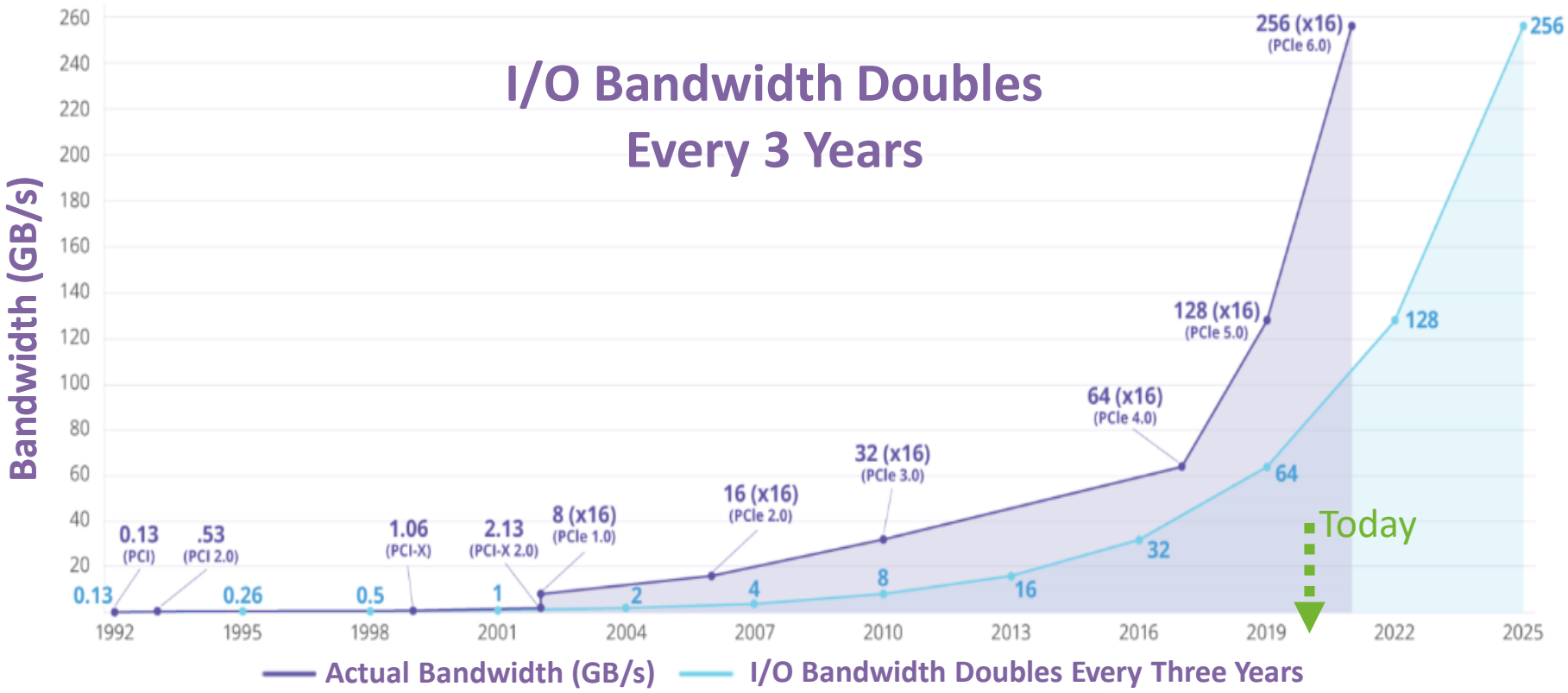
PCIe 5.0 Applications



- **Artificial Intelligence (AI) Accelerators**
- **Machine Learning (ML)**
- **Cloud computing/Visual computing** → Cache Coherency enabling low latency heterogeneous computing (CXL, CCIX, GenZ, OpenCAPI)
- **Networking/Servers**
- **Storage**
- **Automotive**
- **Gaming**
- **FPGA**



PCI-SIG Roadmap



PCI-SIG Announced PCI Express 6.0 – June 2019

Tuesday, June 18th 2019

PCI-SIG Announces PCIe 6.0 Specification

PRESS RELEASE by AleksandarK | Jun 18th, 2019 12:47 | Discuss (34 Comments)

PCI-SIG today announced that PCI Express (PCIe) 6.0 technology will double the data rate to 64 GT/s while maintaining backwards compatibility with previous generations and delivering power efficiency and cost-effective performance. The PCIe 6.0 specification is actively targeted for release in 2021.

PCIe 6.0 Specification Features

- Delivers 64 GT/s raw bit rate and up to 256 GB/s via x16 configuration
- Utilizes PAM-4 (Pulse Amplitude Modulation with 4 levels) encoding and leverages existing 56G PAM-4 in the industry
- Includes low-latency Forward Error Correction (FEC) with additional mechanisms to improve bandwidth efficiency
- Maintains backwards compatibility with all previous generations of PCIe technology

"PCI Express technology has established itself as a pervasive I/O technology by sustaining bandwidth improvements for five generations over two decades," Dennis Martin, an analyst at Principled Technologies, said. "With the PCIe 6.0 specification, PCI-SIG aims to answer the demands of such hot markets as Artificial Intelligence, Machine Learning, networking, communication systems, storage, High-Performance Computing, and more."

"Continuing the trend we set with the PCIe 5.0 specification, the PCIe 6.0 specification is on a fast timeline," Al Yanes, PCI-SIG Chairman and President, said. "Due to the continued commitment of our member companies, we are on pace to double the bandwidth yet again in a time frame that will meet industry demand for throughput

To learn more about PCI-SIG, visit www.pcisig.com.

About PCI-SIG

PCI-SIG is the consortium that owns and manages PCI specifications as open industry standards. The organization defines industry standard I/O (input/output) specifications consistent with the needs of its members. Currently, PCI-SIG is comprised of over 800 industry-leading member companies. To join PCI-SIG, and for a list of the Board of Directors, visit www.pcisig.com.

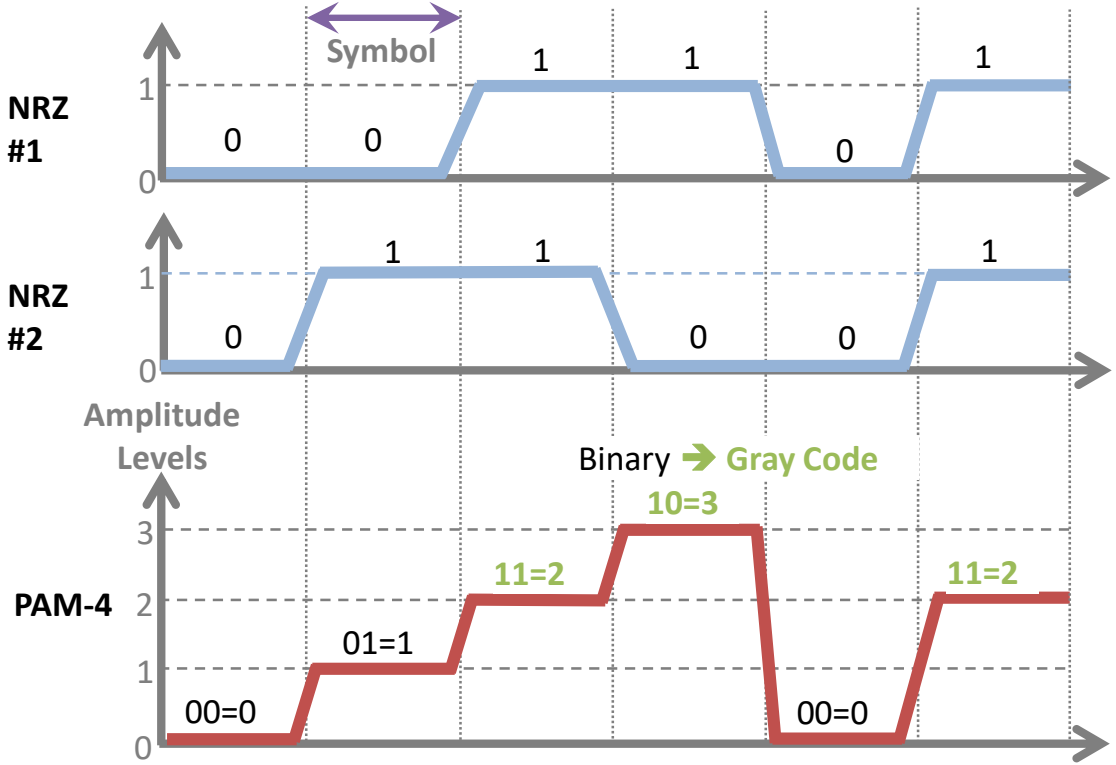
PCIe 6.0 specification features

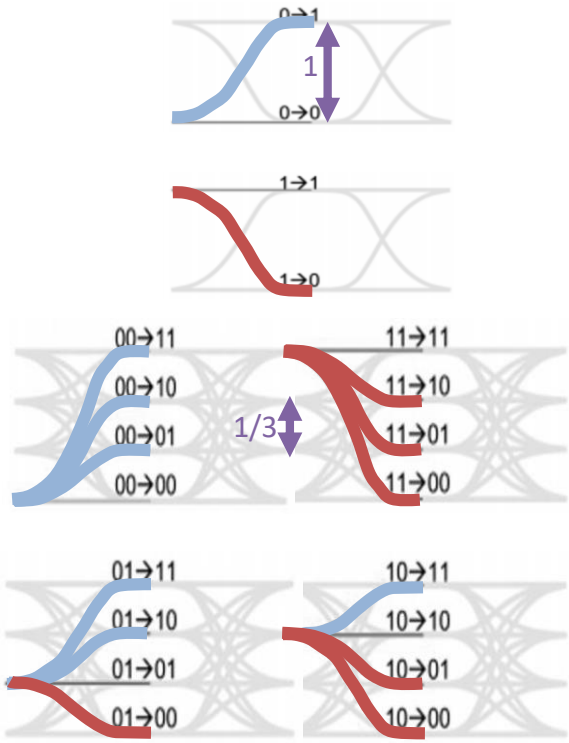
- 64 GT/s raw bit rate (double PCIe 5.0 @ 32 GT/s)
- Delivers up to 256 GB/s via x16 configuration
- Utilizes PAM4 (Pulse Amplitude Modulation vs. NRZ
- Use of low-latency FEC (Forward Error Correction)
- Maintain backward compatible with all previous generations of PCIe technology
- Targets high performance computing requirements of AI/ML & data center application

Targeted for Release in 2021

Multi-Level Signaling vs. Binary Modulation

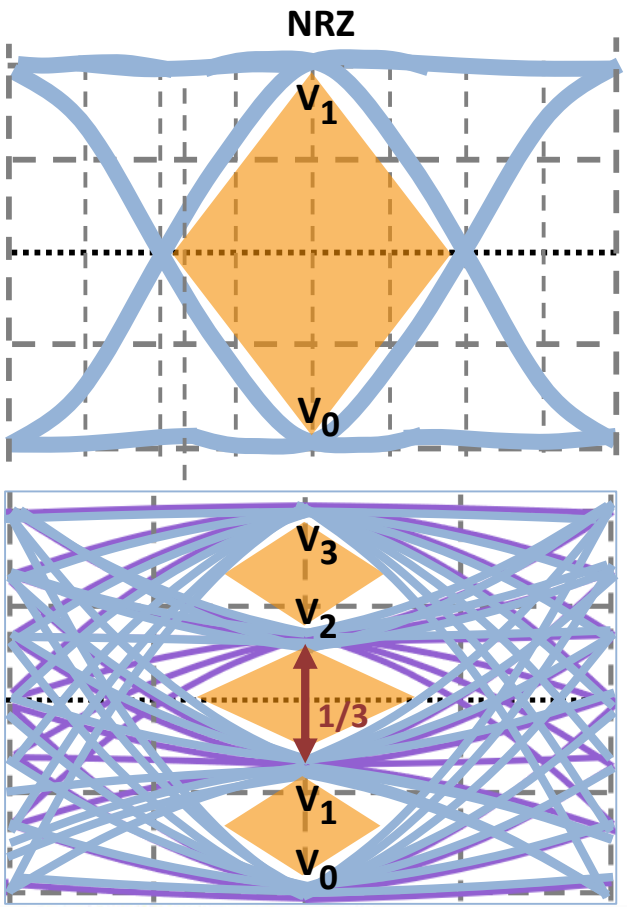
PAM-4 (4-Level Pulse Amplitude Modulation) vs. NRZ (Non Return to Zero)





Channel Impairment Impact

- Additional voltage levels reduces the eye height by a factor of 3 in PAM-4
  - Signal-to-noise ratio (SNR) degrades
- Tx output eye width ➔1/2 to 2/3 of NRZ
  - Middle eye is the most symmetrical
  - Top and bottom eyes do not match the middle eye
- Impairments impact each of the three eyes differently
- Nonlinearity can significantly impact bit error rate
- Crosstalk and reflection have greater signal degradation impact



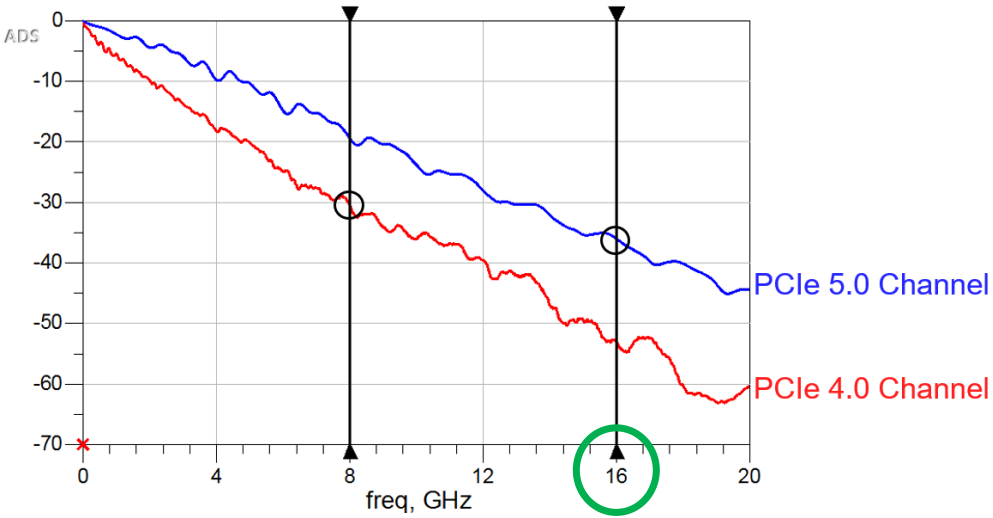
PCIe simulation Challenges: From NRZ to PAM4

Pegah Alavi

Senior Applications Engineer, Keysight Technologies

PCIe 5.0, and the path forward

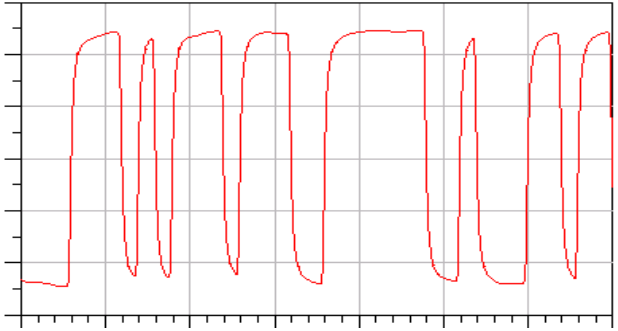
- **PCIe 5.0 total channel loss: 36 dB @ 32GT/s**
- **PCIe 5.0 is NRZ signaling**
  - 32GT/s (NRZ) ➔ 16 GHz Nyquist
- **Next generation PCIe will be using PAM-4 signaling**
- **Next gen data rate 64 GT/s (using PAM-4)**
  - 64 GT/s (PAM-4) ➔ 16 GHz Nyquist

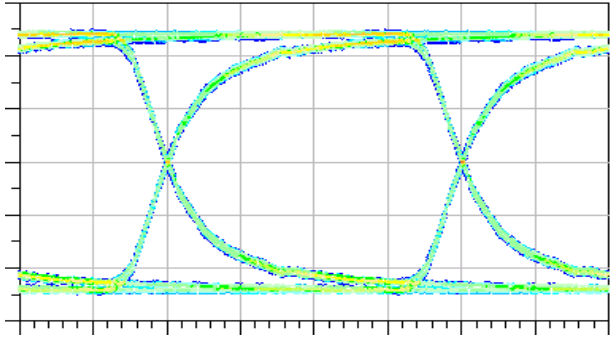


PCIe 6.0 frequency

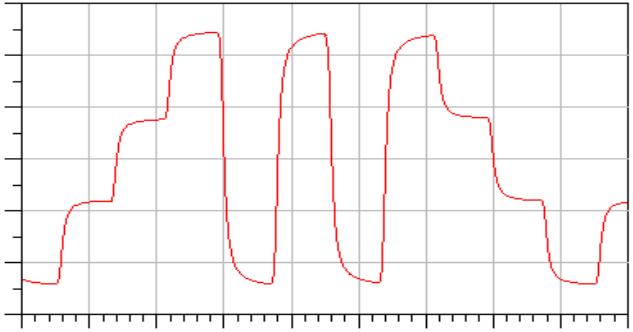
PAM-4 vs NRZ

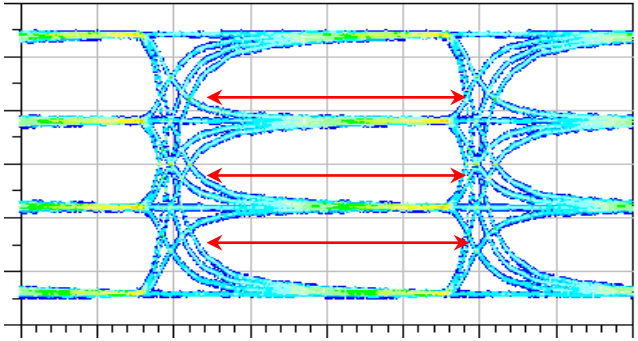
NRZ





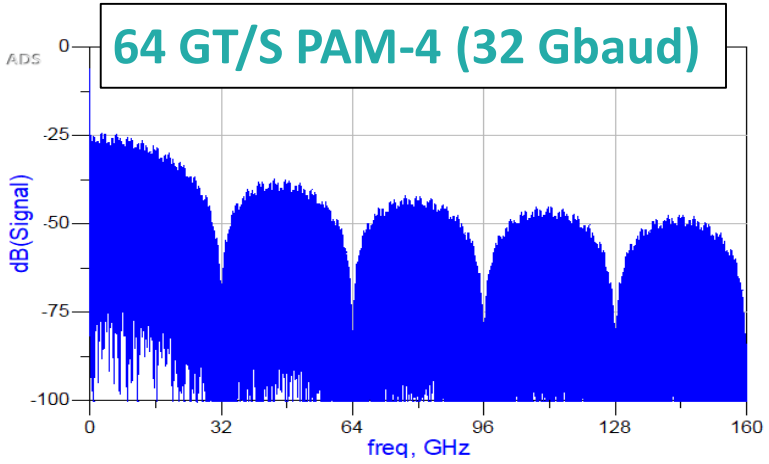
PAM-4

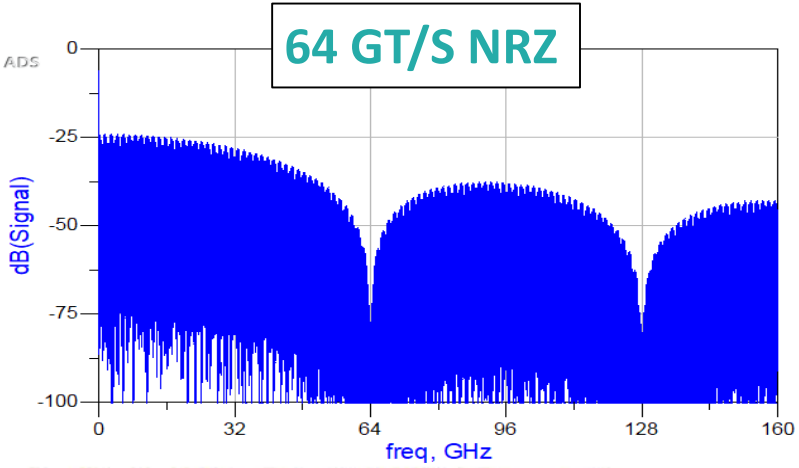




PAM-4 vs NRZ

- PAM-4 operates at ½ the baud rate, requiring less bandwidth
- PAM-4 suffers ½ the loss in dB
- PAM-4 enables higher data rates over legacy channels
- PAM-4 has 9.6dB LESS usable SNR (1/3 of the level separation)



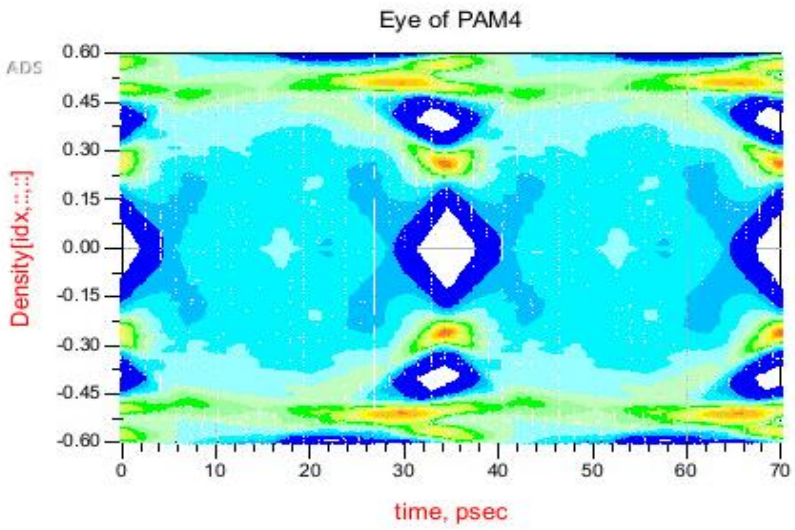


PAM-4 Design Challenges

- Nonlinearity between levels due to compression
- Lower SNR, more susceptible to jitter & noise
- CDR
- DFE
- Uses 3 slicers for symbol decision
- Slicer threshold tuning
- Timing skews between three slicers for optimal sampling
- Analog based architecture vs ADC based architecture
- More complex SerDes design, higher cost

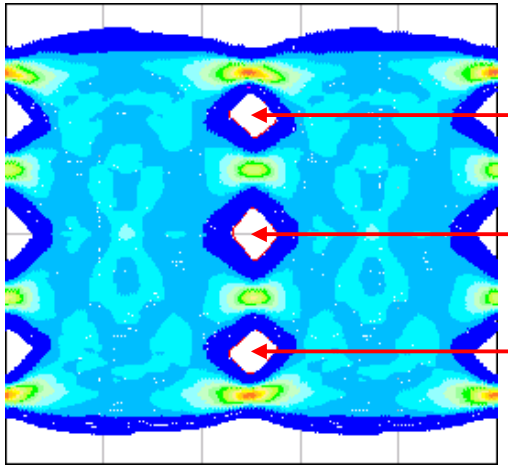
PAM-4 Design Challenges

Non-linearity Due to Gain Compression



Upper and Lower Eye impacted, center eye impact is minor

Slicer Threshold Tuning & Adaptation



PAM-4: Three slicers in PAM-4, vs 1 in NRZ

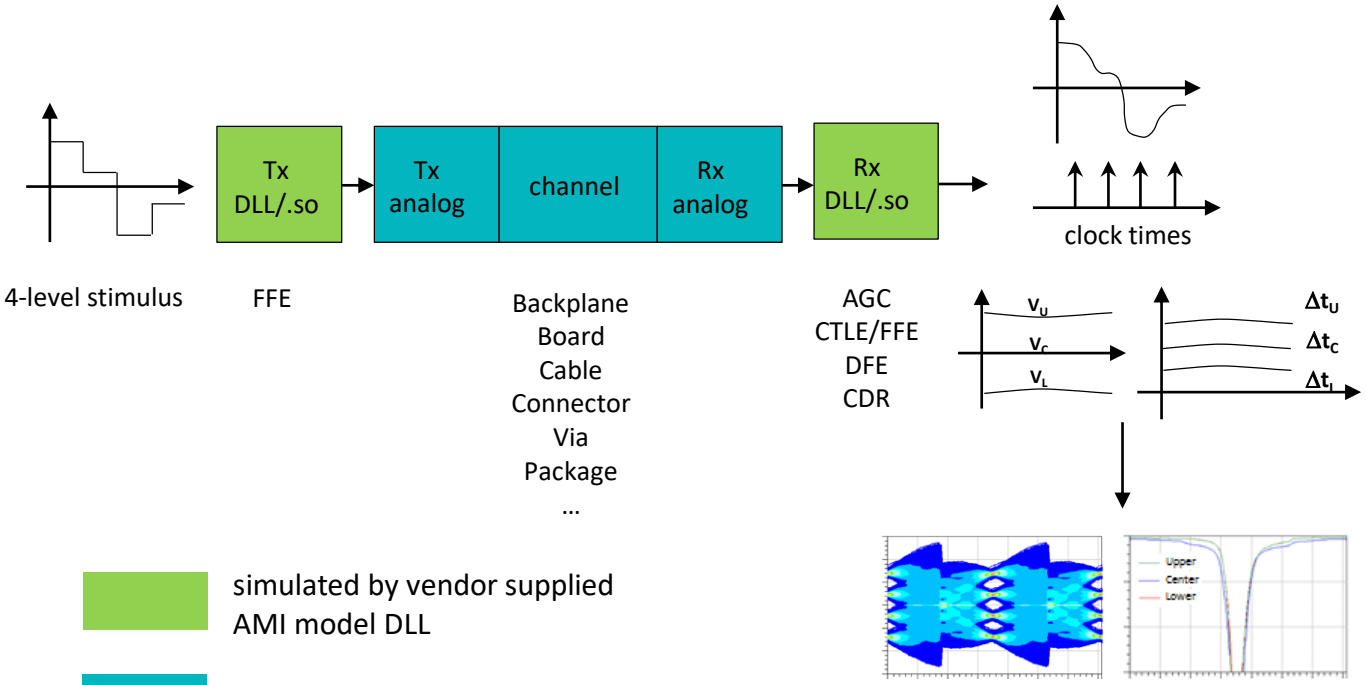
PAM-4:Thresholds must be adjusted (Value is 0 in NRZ)

PAM-4: Threshold values can change with time due to adaptation

PCIe 6.0 Design/Simulation Challenges

- SERDES design much more complex
- Cost will likely be much higher (compared to existing PCIe devices)
- Modeling of SERDES will be more challenging
- Non-linear behavior must be captured in model for accurate simulation
- Simulation time might be significantly longer (if multiple CDR/DFEs are present in each model)
- Statistical simulations may not be feasible
- The good news: IBIS-AMI already has an established methodology for PAM-4 models

PAM-4 AMI Simulation Flow



simulated by vendor supplied AMI model DLL

simulated by EDA tool

V_U, V_C, V_L: upper, center and lower eye thresholds
Δt_U, Δt_C, Δt_L: upper, center and lower eye offsets

Improved PCB for Connector

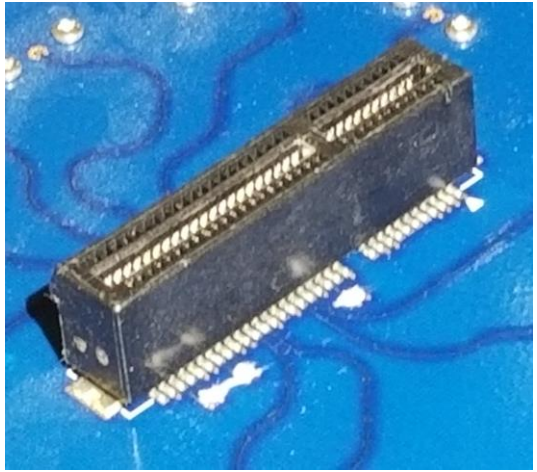
Tim Wig

Signal Integrity Engineer, Intel Corporation

PCIe 5.0 Connector Interface

The PCIe CEM connector Add-in Card interface has been updated, affecting

- **Add-in Card PCB edge finger geometry**
- **Baseboard/Host PCB contact footprint**
- **Connector performance**
- **Signal integrity engineers must closely supervise PCB layout, from pre-layout to tapeout, to ensure that all requirements are applied**



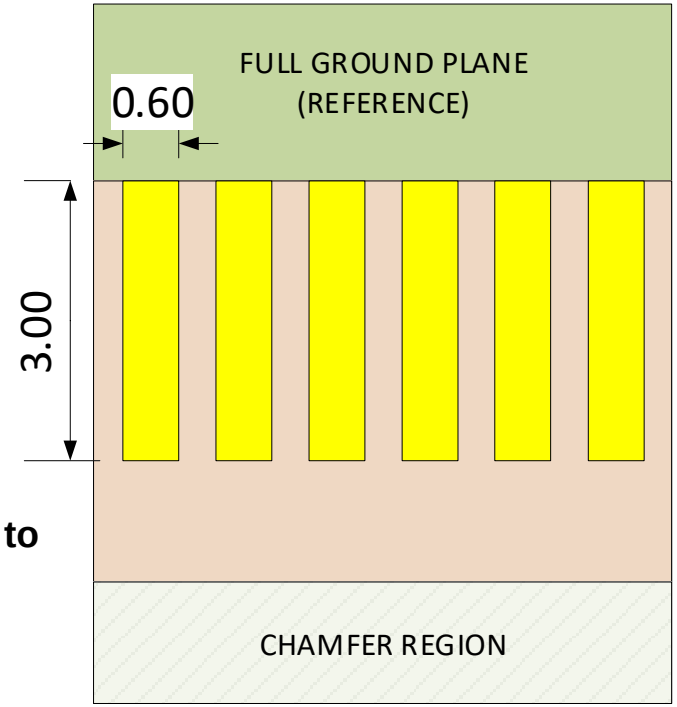
- **Only Surface Mount (SMT) PCIe CEM connectors are allowed for Gen 5.0**
- **Thru-Hole and Press-Fit connectors are <u>not permitted</u> beyond Gen 4.0**

Add-in Card Edge Finger PCB Geometry

Add-in card updates improve signal integrity

- **Gold edge fingers become <u>shorter</u> and <u>narrower</u> for PCIe 5.0**
  - **<u>0.60 mm</u> wide (was 0.70 mm in 4.0)**
  - **<u>3.00 mm</u> long (was 3.91 mm in 4.0)**

- **All edge fingers are now the same length**
  - **Previously, PRSNT1# & PRSNT2# pins were shorter to support unmanaged hot plug**
  - **<u>Unmanaged</u> hot plug is deprecated for CEM 5.0**



Add-in Card Edge Finger Shielding Planes

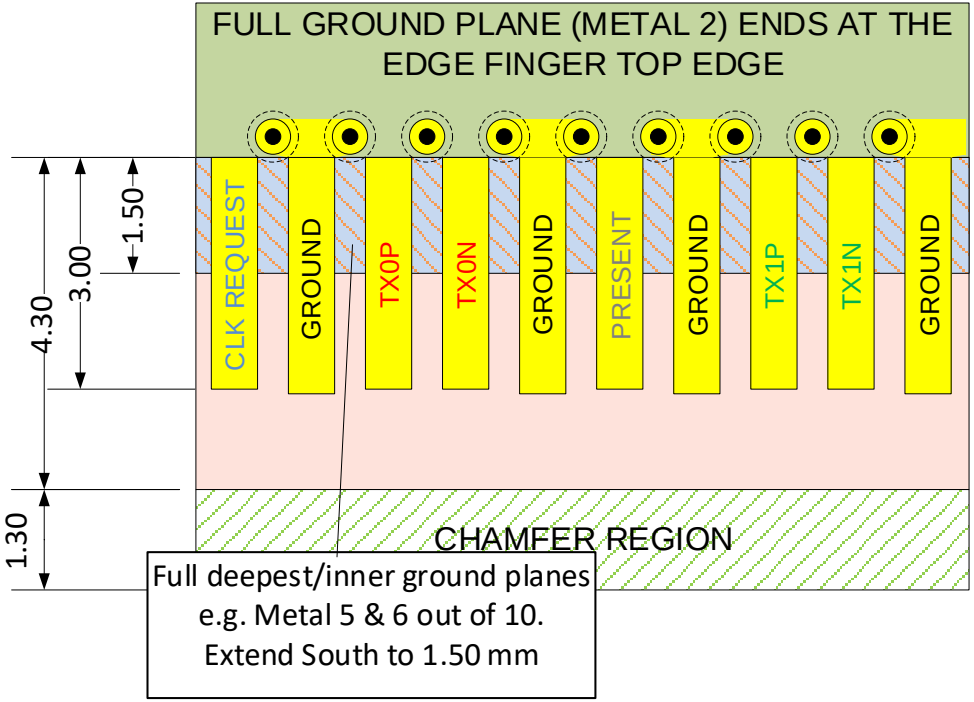
Tx-Rx NEXT was identified as the dominant signal integrity impediment

Two alternatives are being finalized for *Core Shielding Ground Planes* under the edge fingers to reduce Rx-Tx crosstalk (NEXT)

<u>Version 1:</u>

Two deep 1.50 mm long planes, cover the top half of the edge fingers

Planes lie 0.52 mm (21 mil) beneath the surface, i.e. within the middle 1/3 of the PCB



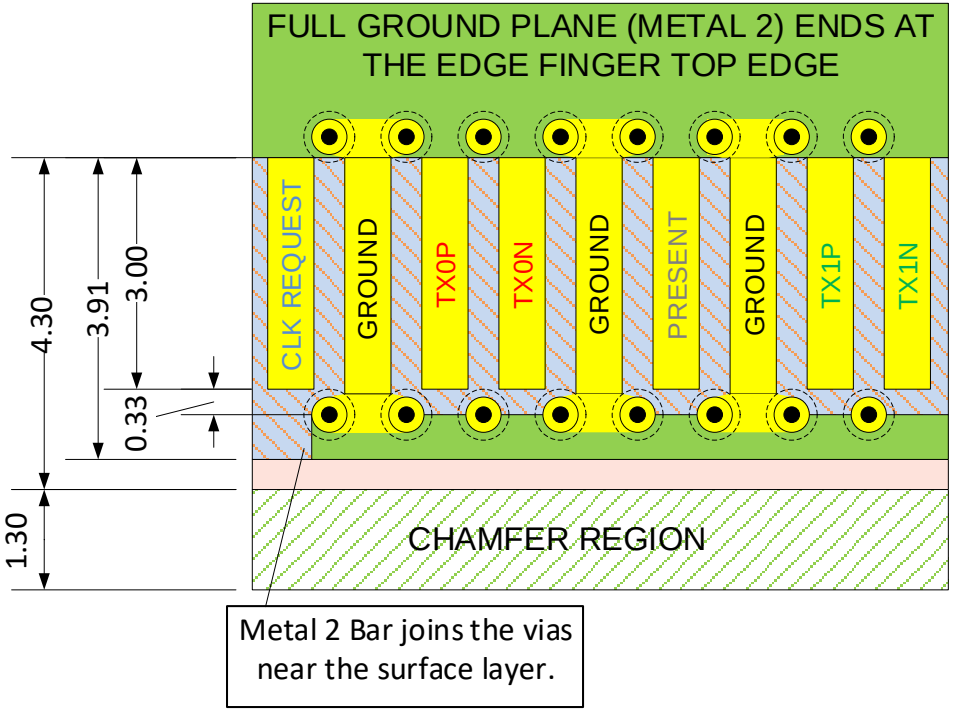
Add-in Card Edge Finger Shielding Planes

The core shielding strategy has been extended to

<u>Version 2:</u>

A second set of vias in the South side joined with a lateral bar on the first inner layer Metal 2

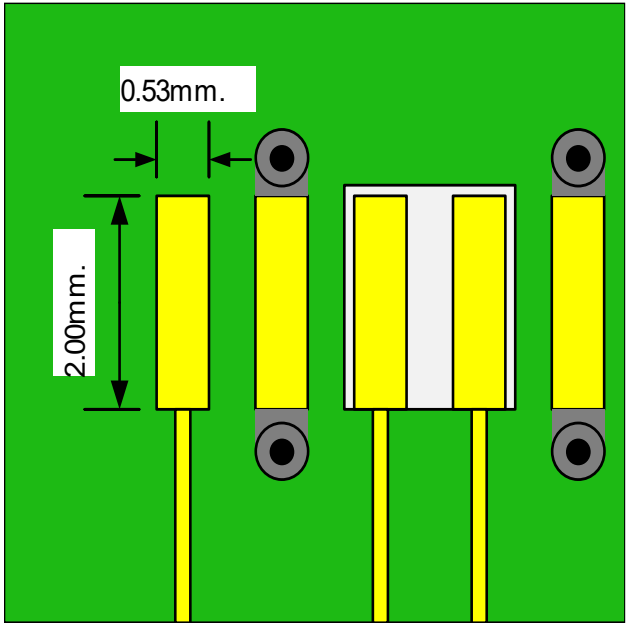
Core shielding planes extend ≈ 3.91 mm instead of 1.5 mm provide reductions in NEXT ≈ 20 dB



Baseboard PCB Connector Footprint

Baseboard/Host SMT connector footprint

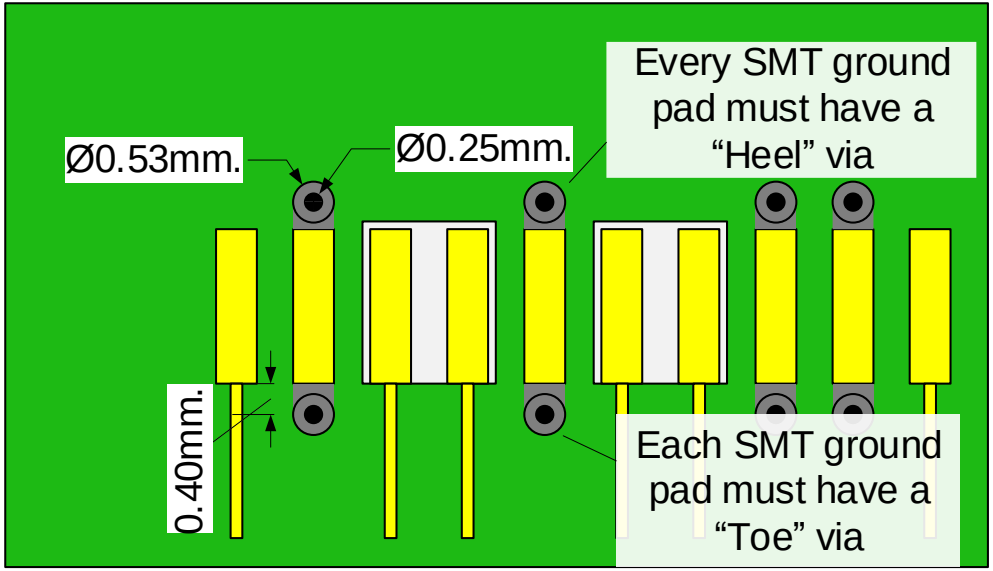
- **The baseboard SMT connector footprint solder pad width for PCIe Gen 5.0 is <u>0.53 mm</u>**
  - For comparison, PCIe CEM Gen 4.0 mandated a 0.7 mm SMT pad width
- **The connector footprint solder pad length for PCIe Gen 5.0 is <u>2.0 mm</u>**
  - This dimension is unchanged from PCIe CEM Gen 4.0



Baseboard PCB Connector Footprint

Baseboard/Host SMT Toe and Heel vias

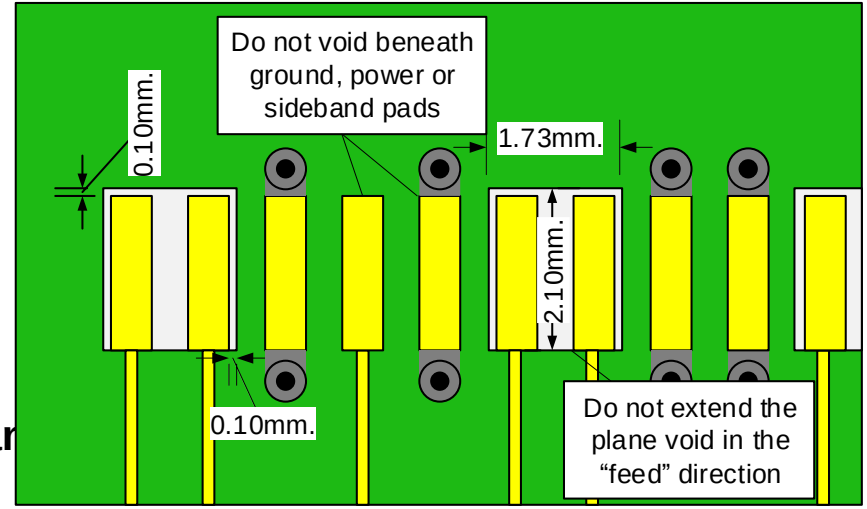
- **Every baseboard ground pad must have both <u>Toe</u> and <u>Heel</u> ground vias**
- **Place them as close as possible to the ground pads**
- **Generally useful with other SMT connector footprints, too**



Baseboard PCB Connector Footprint

SMT voiding dimensions

- **Ground plane voiding is required under the high speed pairs**
- **Do not void beneath sideband, power, or ground SMT pads**
- **Voiding on the only the adjacent ground plan is typically sufficient**
- **This specific voiding size is <u>recommended</u>**

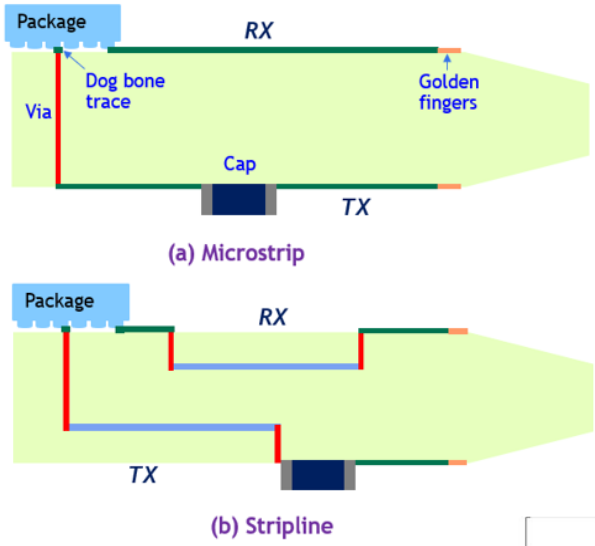


32G and 64G Simulated Channels

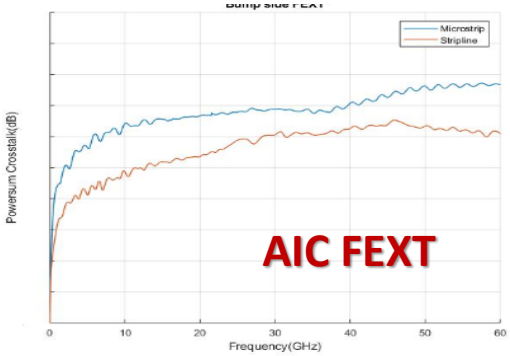
Ying Li

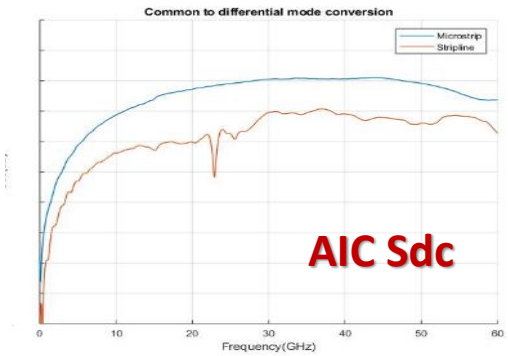
Senior SI/PI Engineer, NVIDIA Corporation

Microstrip vs Stripline at 16GHz (both for Gen5/6)

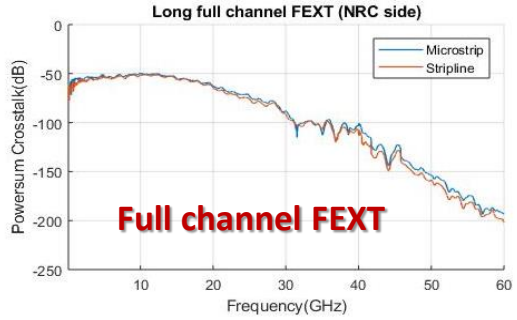


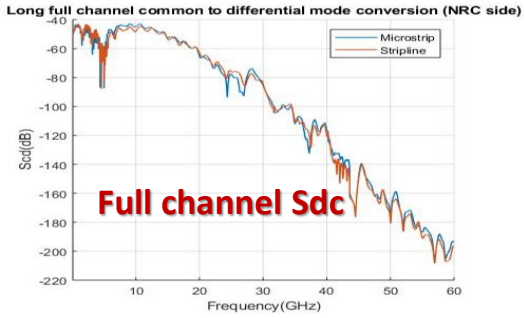
@16GHz	Microstrip	Stripline
Trace Loss	~0.5dB less loss than stripline ✔	
• Trace Width	30% wider than stripline ✔	
• Humidity sensitivity	DK increase ~2% DF increase ~40%	Almost no impact at all frequencies ✔
• Surface roughness	Up to 7um (HTE/RTF)	Better controlled (1um for HVLP) ✔
FEXT	10+dB worse than stripline	✔
Mode conversion	~20dB worse than stripline	✔

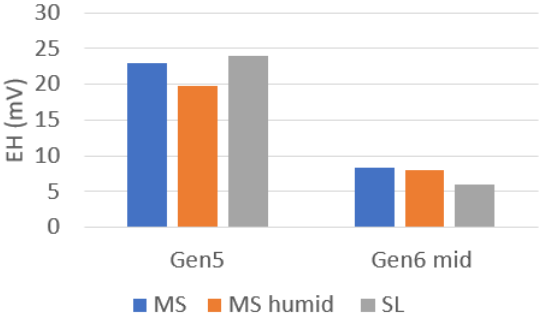


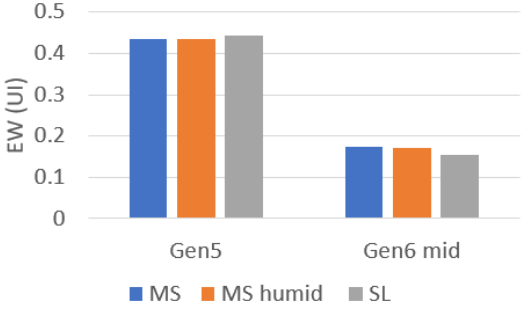


Microstrip vs Stripline impact on Full channel (worst loss)





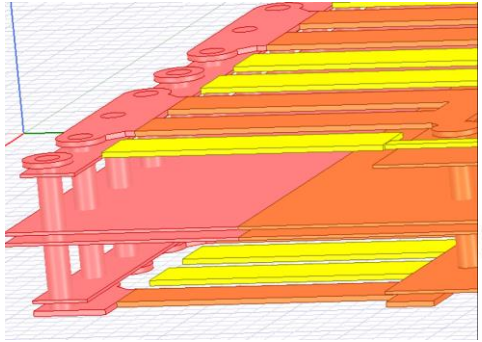


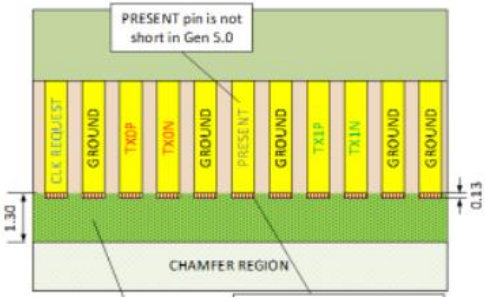


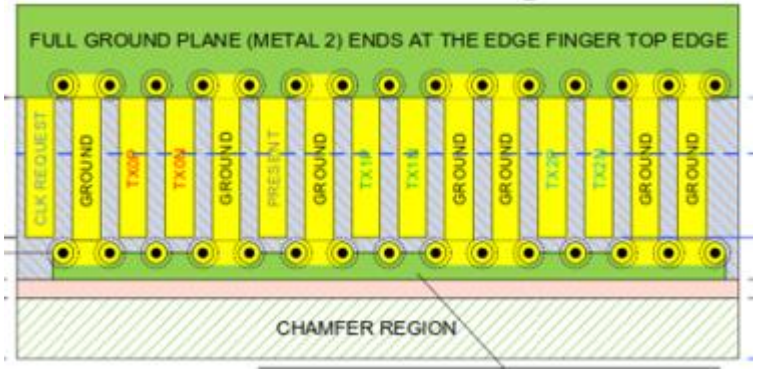
- **Full channel loss will mask the FEXT and Sdc differences**
- **Microstrip Humid 13% less margin than normal for Gen5, but only 4% for Gen6**
- **Stripline eye is only 4% better than microstrip in Gen5, but can be much 15% worse than Gen6 due to the extra via for layer transition**

South via added to AIC Golden Fingers

- **Connector NEXT largely improvement (-40dB to -60dB range)**



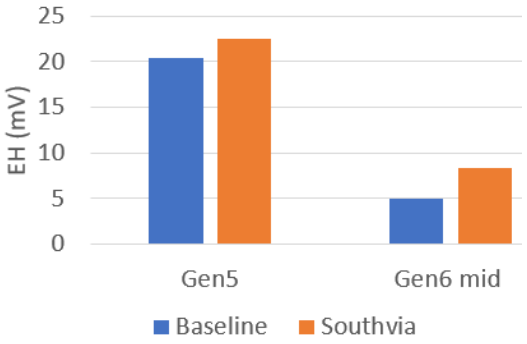


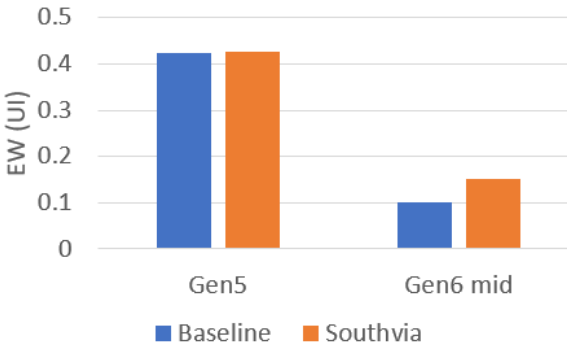


Figures from Intel &Samtec

South via added to AIC Golden Fingers-Channel Impact

- **South via added to Add-in Card Golden Fingers will improve Gen6 margin by more than 50%, but only 10% for Gen5**
- **It will need extra procedures to the golden finger area, need to check manufacturing liabilities**





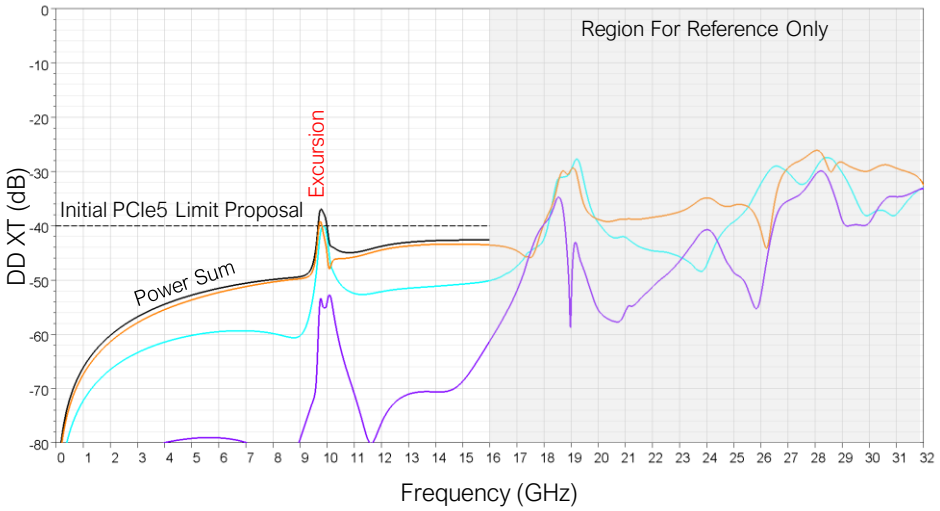
Integrated Crosstalk Noise as a Component Requirement Modifying the Weighting Function (PSD) for a Connector Only Channel Component

Patrick Casher

Pr. Product Development Engineer, Foxconn Interconnect Technology

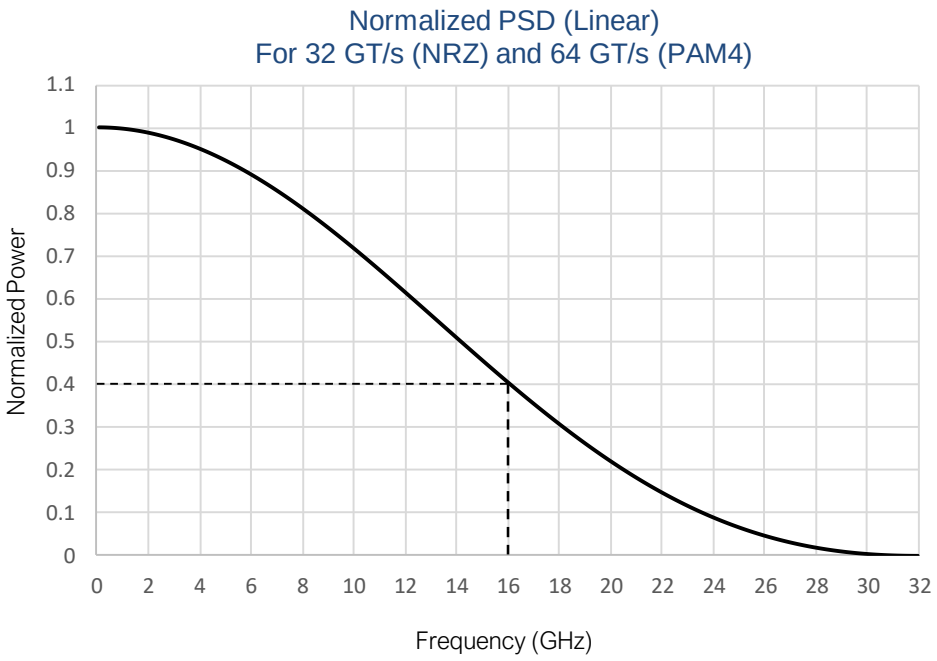
Background

- **Initial question in the PCI SIG was** *Can we allow excursions in the current proposed limit line requirement? If so, how much while maintaining functional channels?*
- **This set the stage to develop an improved, more meaningful, connector crosstalk performance requirement.**
  - The current requirement was a traditional PCIe static limit line, a constant -40 dB to 16 GHz for both Power Sum DDNEXT and DDFEXT
- **For the current 32 GT/s application and future applications 64 GT/s**



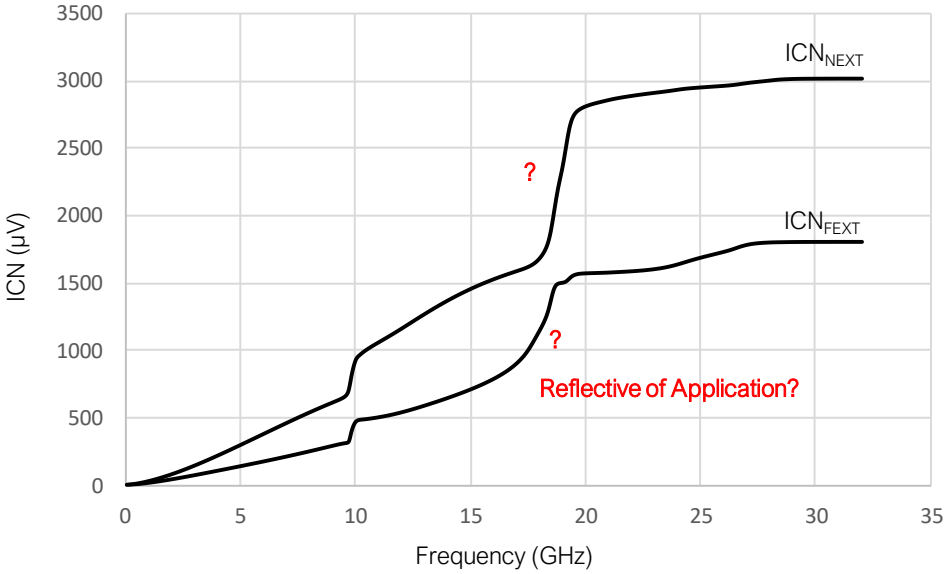
Hypothesis

- **This question can be answered by looking at the energy content of the crosstalk excursion and envelope.**
- **The power spectral energy in a random NRZ bit pattern is not constant versus frequency.**
  - Location of the excursion would also be of interest.
- **A more contemporary crosstalk constraint, ICN, is based on this power spectral density and is used in other standards.**
  - Enables a trade-off between excursion magnitude and overall crosstalk floor.



Concerns

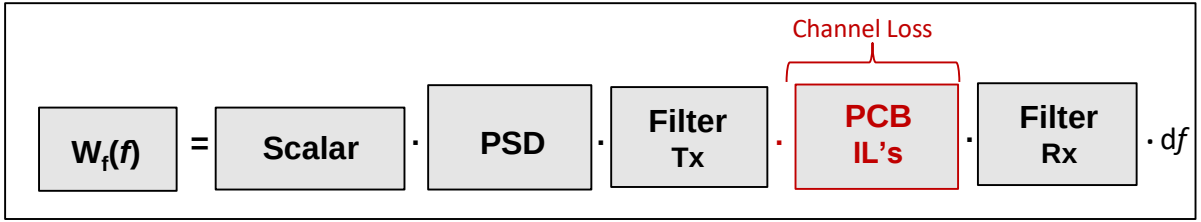
- **We initially discussed directly applying the traditional ICN formula to just the connector.**
  - Looking at the data we questioned the high frequency contribution to the final ICN value.
  - In a channel we would expect these frequencies to have additional attenuation before the reaching the connector
  - As a remedy, a proposal was made to add the channel loss to the frequency dependent weighting function.
    - *Turned out this was previously presented at DesignCon[1] as ccICN (component contribution ICN)*



ICN Integration Progress Example

ICN with Connector Embedded in Channel

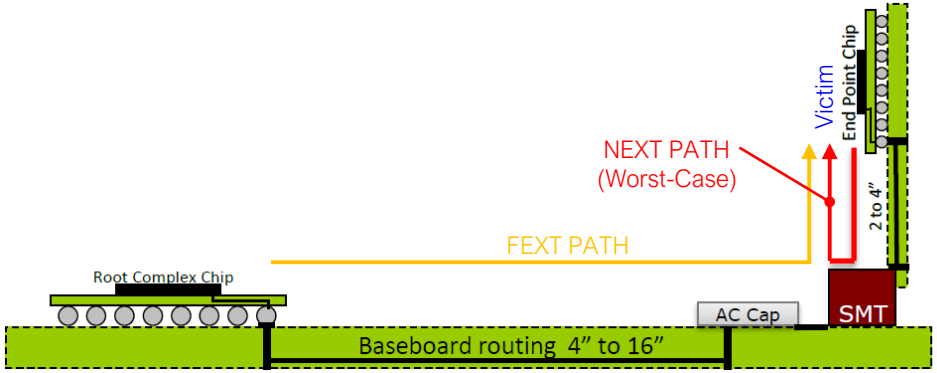
- **Weighting function modified to account for channel loss impact on power spectrum**
- **Component Contribution ICN, ccICN[1]**



Block Diagram of ICN $W_f(f)$ with Channel Loss Component

PCIe Channel Losses

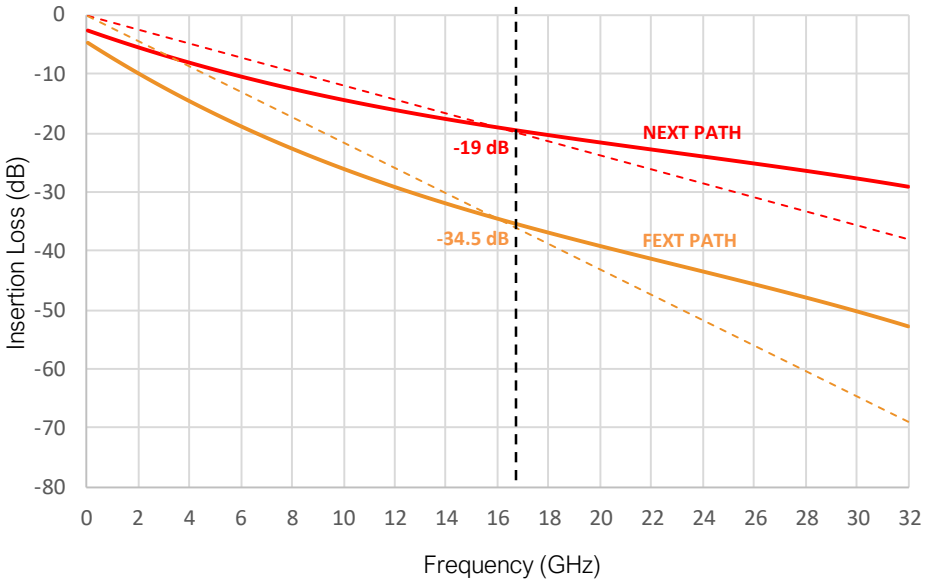
- **AIC Losses**
  - Total: 9.5 dB at 16 GHz max.
  - 2 to 4” of PCB trace, 5.5 dB at 16 GHz
    - *Micro-strip routing, Megtron 6*
  - 4 dB at 16 GHz of package loss
- **Host Losses**
  - Total: 25 dB at 16 GHz max.
  - 4” to 16”, 16 dB at 16 GHz
    - *Strip-line and a routing via incl. stub*
  - 9 dB at 16 GHz package
- **Worst Case is Near-End Channel**
  - AIC side, short aggressor transmitter to receiver victim path, least attenuation of PSD
  - Fresh Tx and attenuated Rx signal, low SNR potential
  - If channel is equalized for a long baseboard then, Tx FFE and Rx DFE will also significantly alter the PSD
    - *Exacerbating the near end crosstalk*



PCIe Channel Topology

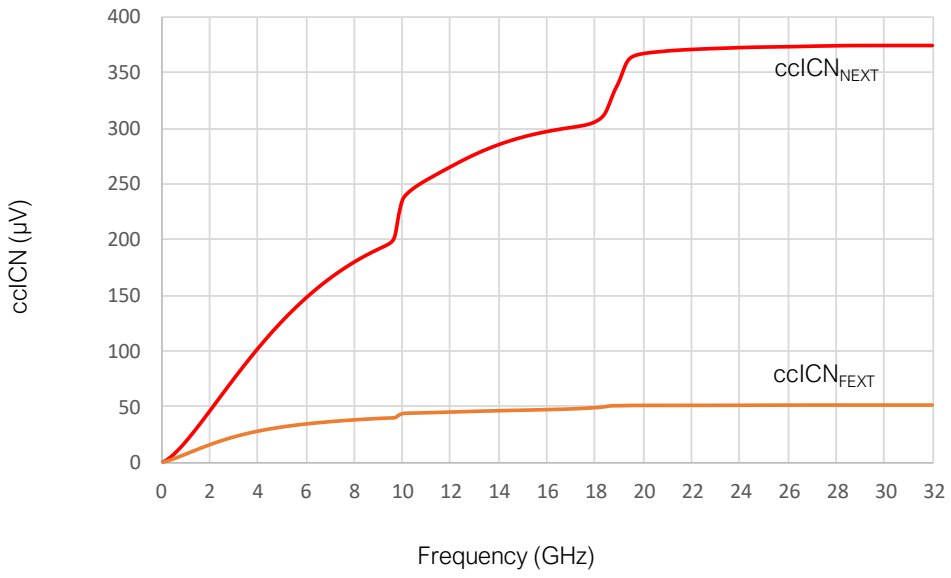
Channel Insertion Loss Plots

- **3D FEM Model (solid lines)**
  - Fitted with polynomial equation
    - *Skin/proximity affect behavior, finite conductivity*
- **Approximation**
  - $Power\ Loss\ (linear) = 10^{\left(\frac{-IL_{PCB}\cdot\frac{f}{fb}}{10}\right)}$
    - *Used for ICN Weighting function*
    - *Does not account for skin/proximity affect and finite conductivity*
  - $Power\ Loss\ (dB) = 10\cdot\log_{10}\left(10^{\left(\frac{-IL_{PCB}\cdot\frac{f}{fb}}{10}\right)}\right)$
    - *Linear approximation*



Affect

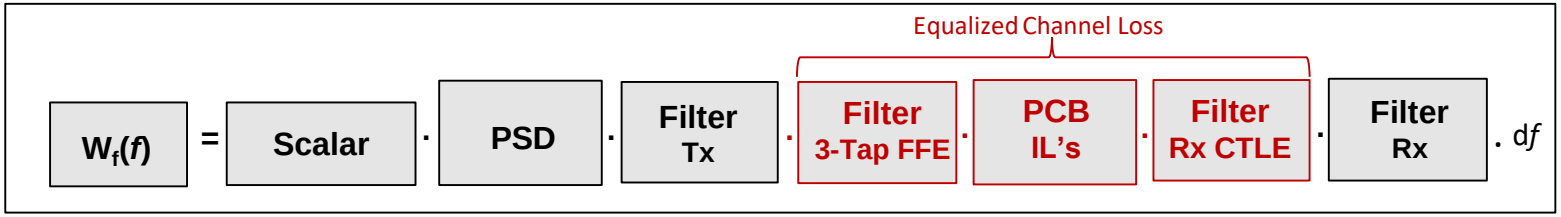
- **Observations**
  - Overall connector ICN values of both NEXT and FEXT are significantly reduced. FEXT ICN magnitude the most.
  - ICN contributions between 15 and 20 GHz are significantly reduced.
  - A different prospective is provided. It was determined that ccICN values are more representative of channel impact by eye simulations. Better correlation was observed.



ccICN Integration Progress

Integrated Crosstalk Noise, ICN

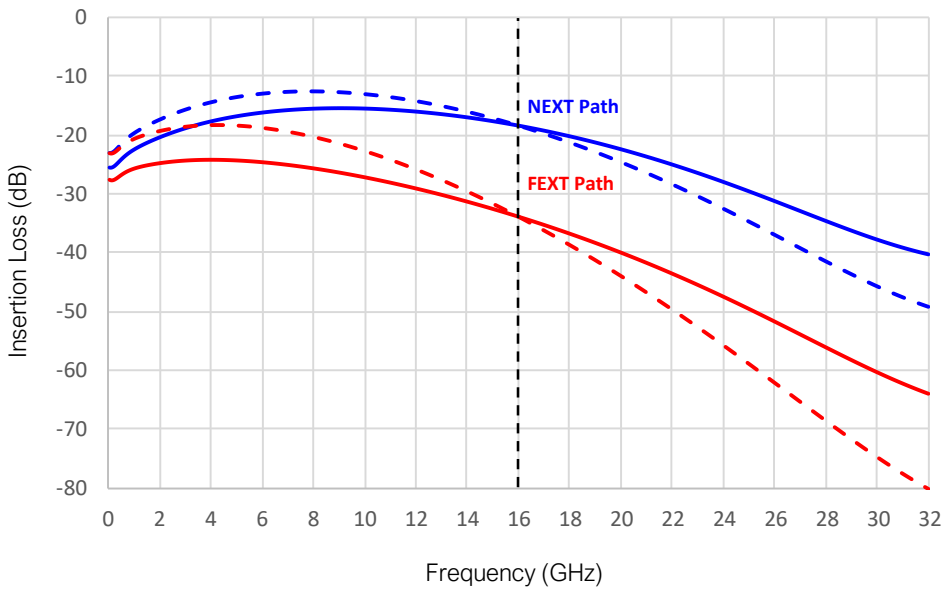
- **With the improvement of adding channel loss it was further requested to consider the affects of equalization on connector ICN.**
- **Modified to account for equalization of losses**



Block Diagram of ICN $W_f(f)$ with Equalized Channel Loss Component

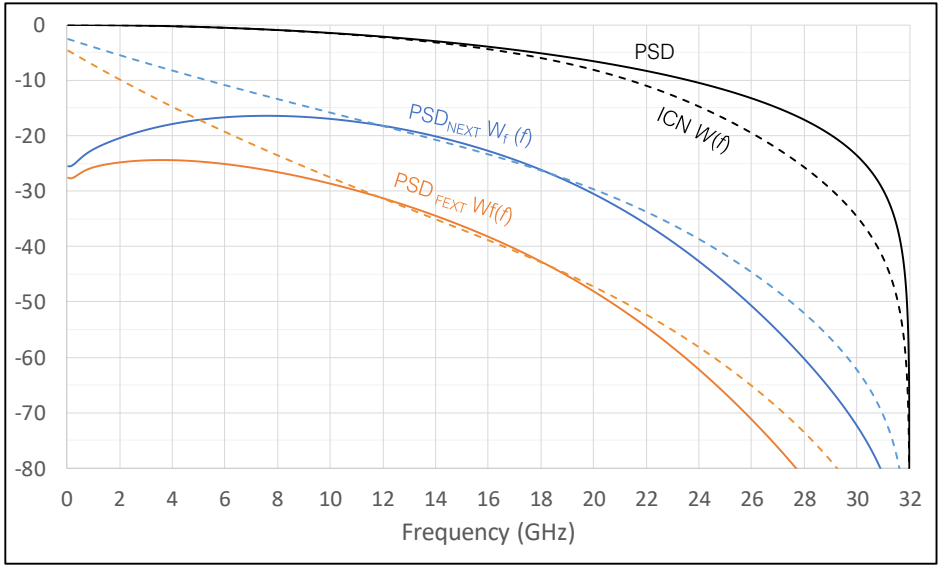
Equalized Channel Insertion Loss Plots

- **NEXT PATH**
  - Next PSD has 15.5 dB at 16 GHz more energy than FEXT at same point
- **FEXT PATH**
  - FEXT has more attenuation than NEXT
    - *15.5 dB more @ 16 GHz*
- **Polynomial curves are flatter, better equalized**
- **"Nyquist" is not the worst-case point.**
  - Other frequencies have higher contributions.
    - *NEXT peak -15.4 dB at 9 GHz*
    - *FEXT peak -24.3 at 4.25 GHz*



Comparison EQ Weighting Functions

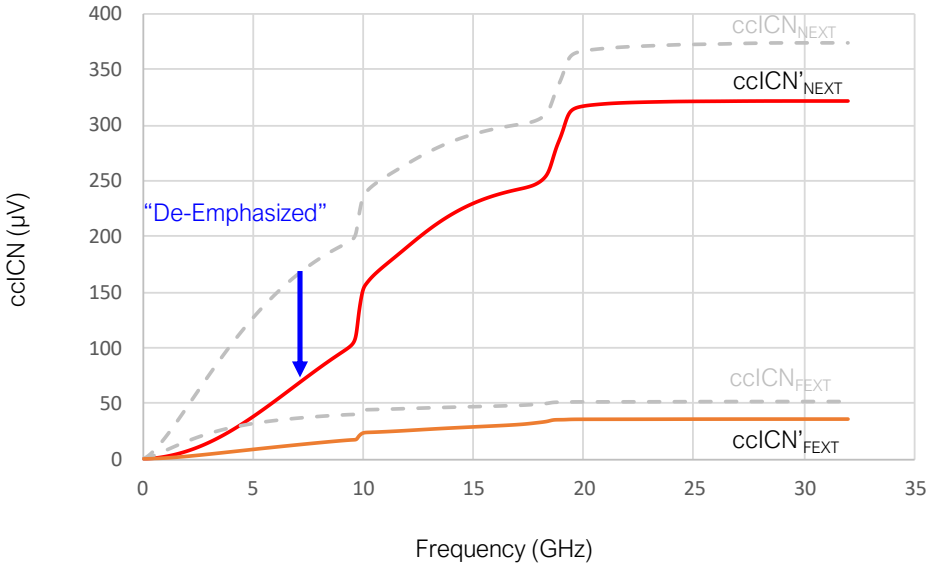
- **Comparison and observation**
  - NEXT $W_f(f)$ behaves similarly to equalized total PCB insertion loss shown earlier
    - *The power peaks at 10.15 GHz (-8.7 dB), at 16 GHz drops of 3.1 dB from peak value*
  - FEXT $W_f(f)$ similarly to an over equalized channel
    - *to much high frequency content relative to the low frequency content*
    - *It's power peaks 4.4 GHz (-23.5 dB), at 16 GHz drops of 12.3 dB from peak value*



Weighting Functions

Channel Equalization Affect on ccICN

- **ccICN versus ccICN with Equalized Channel, ccICN'**
  - Lower frequencies are attenuated, "de-emphasized", by Tx FFE and Rx CTLE



ccICN' Integration Progress

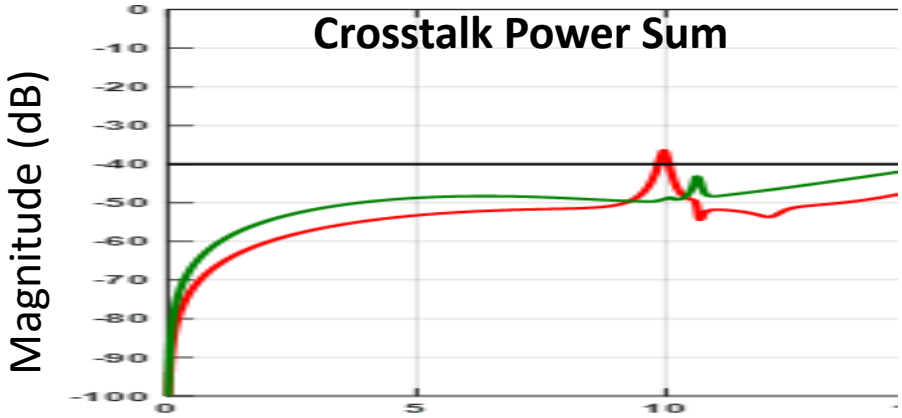
Components and Cables

Steve Krooswyk

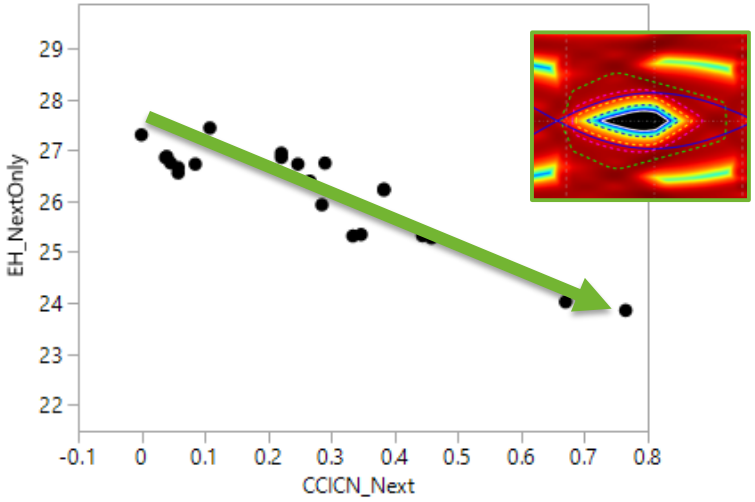
SI Design and PCIe Standards, Samtec

Connector Validation with ICN:

We select the Green component to pass compliance



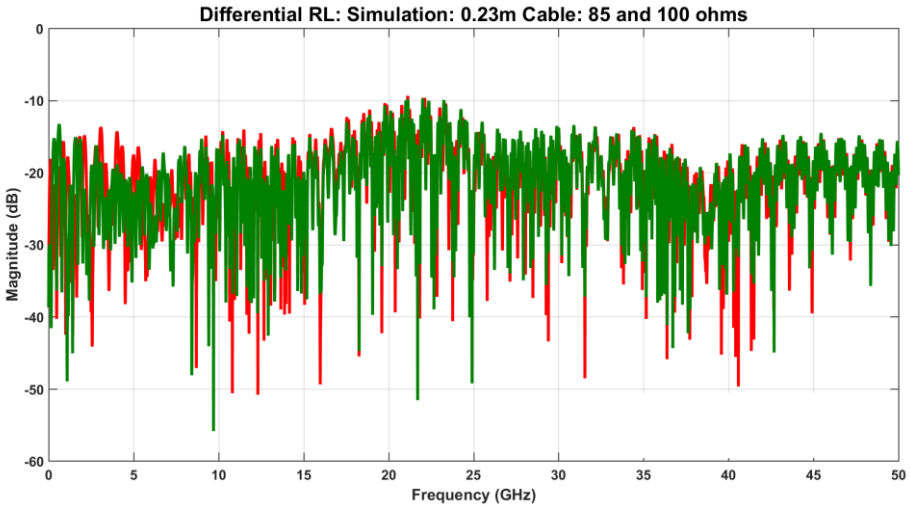
Eye Height by ICN:
Real Connector Models



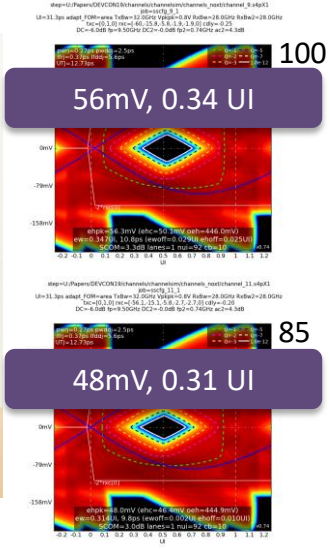
Reality: the Red component performs best in the System

System performance can be predicted with ICN

Selecting 85 or 100 Ohm Cables and Components:

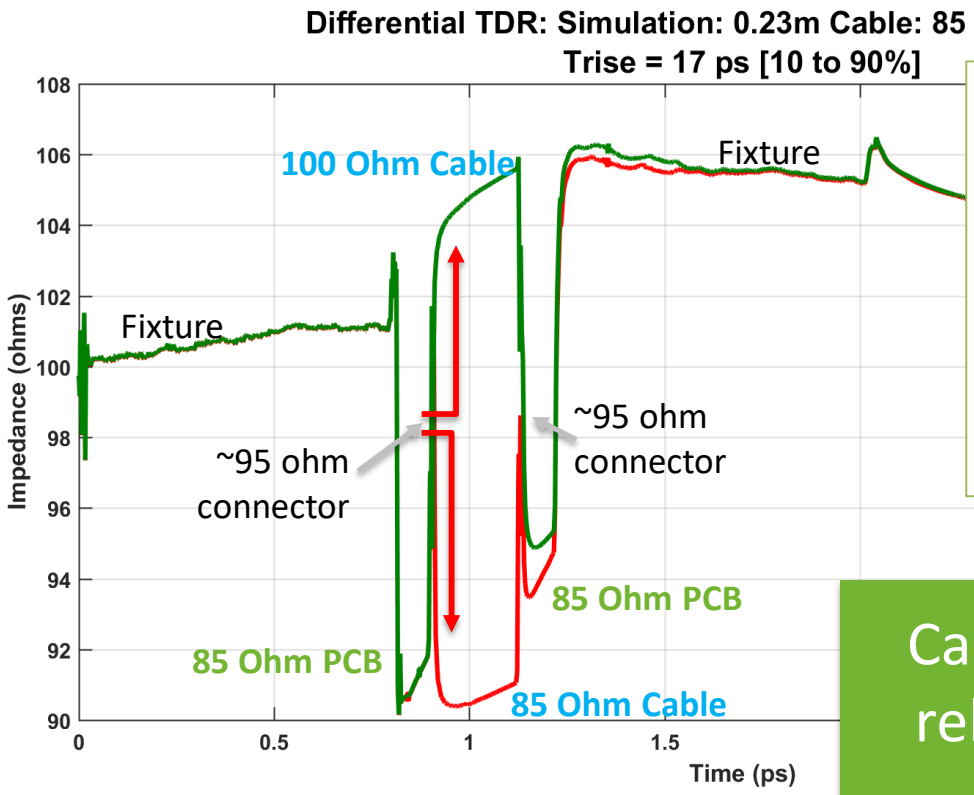


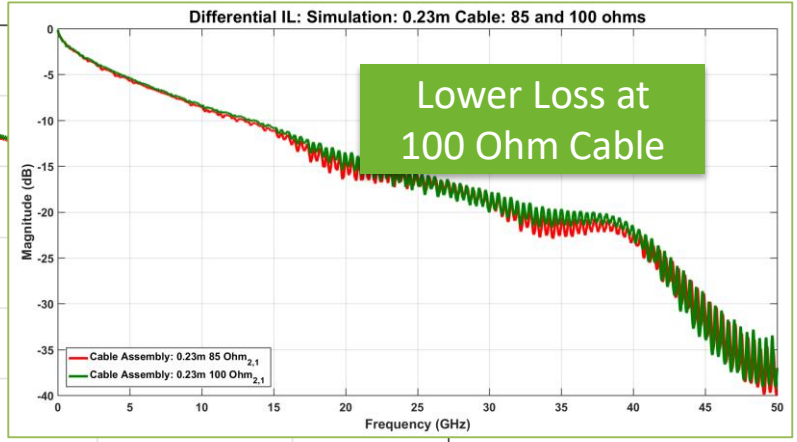
Gen5 EH\EW



Return Loss for 100 Ohm and 85 Ohm Cable:
Both Mated to 85-ohm PCB Route
Which is Which?!

Selecting Impedance: A Closer Look





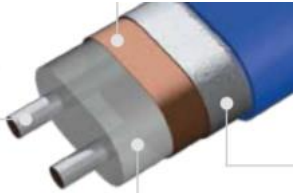
Lower Loss at 100 Ohm Cable

Cable's reflection magnitude related to mating connector

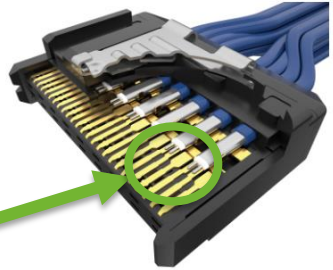
(Here, 92 ohm is perhaps best)

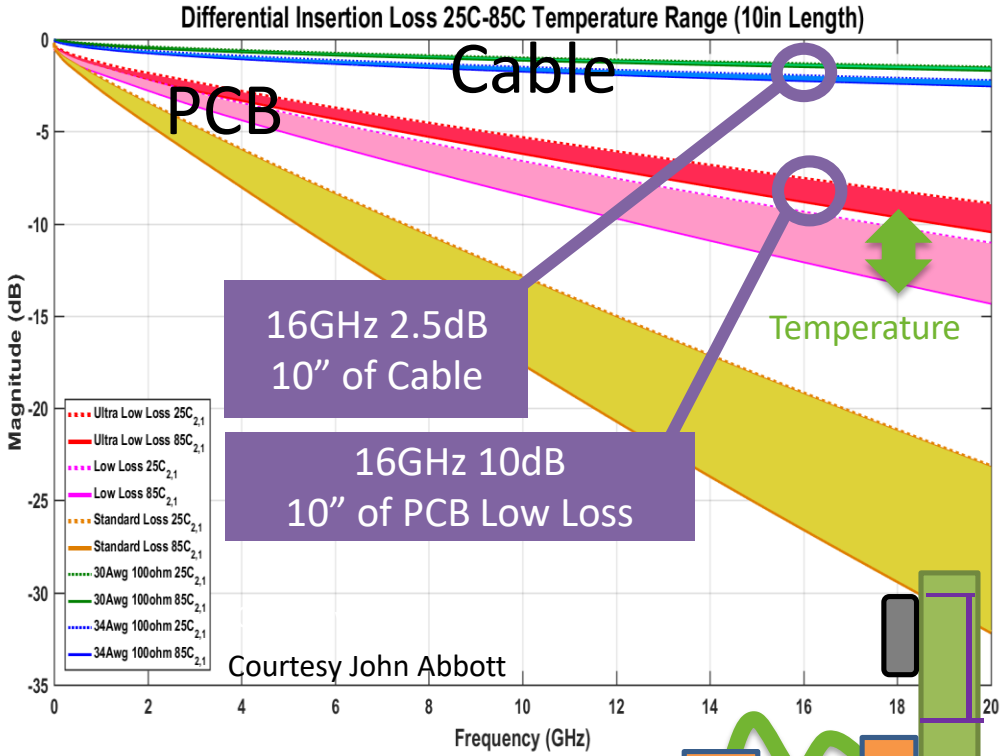
32 and 64G Cable Enablers

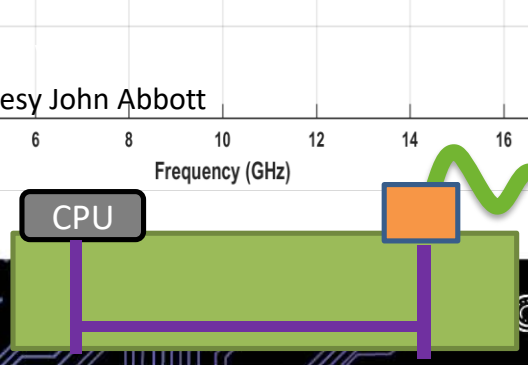
- **Manage intra-pair skew**
  - Single extrusion for uniformity
  - Desire <= 3.5ps intra-pair skew
- **Reduce Loss**
  - Minimize air\mixed modes
  - Consider 100 ohms
- **Reduce RL**
  - Direct Attach
  - Avoid PCBs



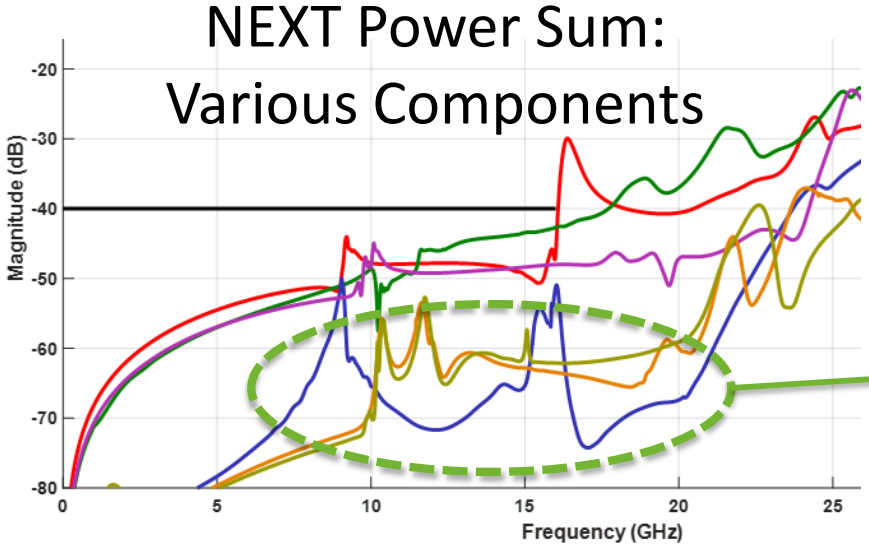
Low Dk FEP Dielectric
Co-extruded Technology
for Dimensional Consistency

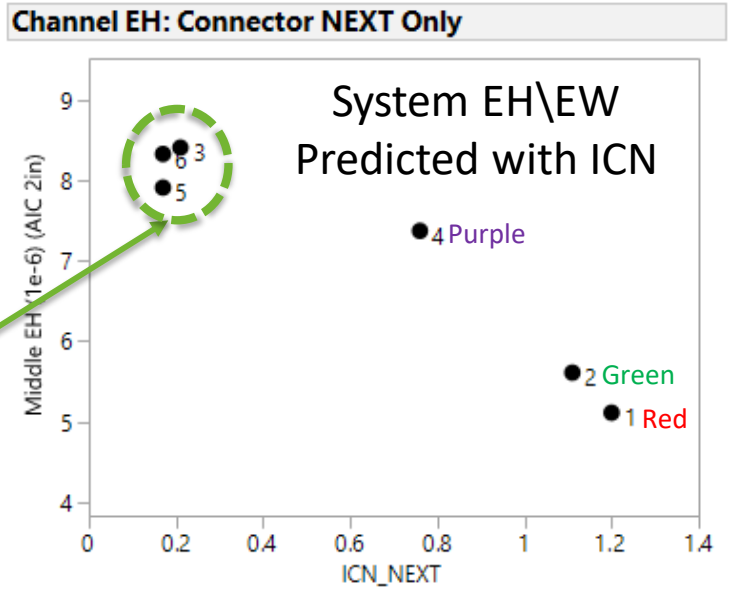






Gen6 64G-PAM4 NEXT Connector\Cable Crosstalk:





Near 60dB likely necessary, and some exceptions are OK

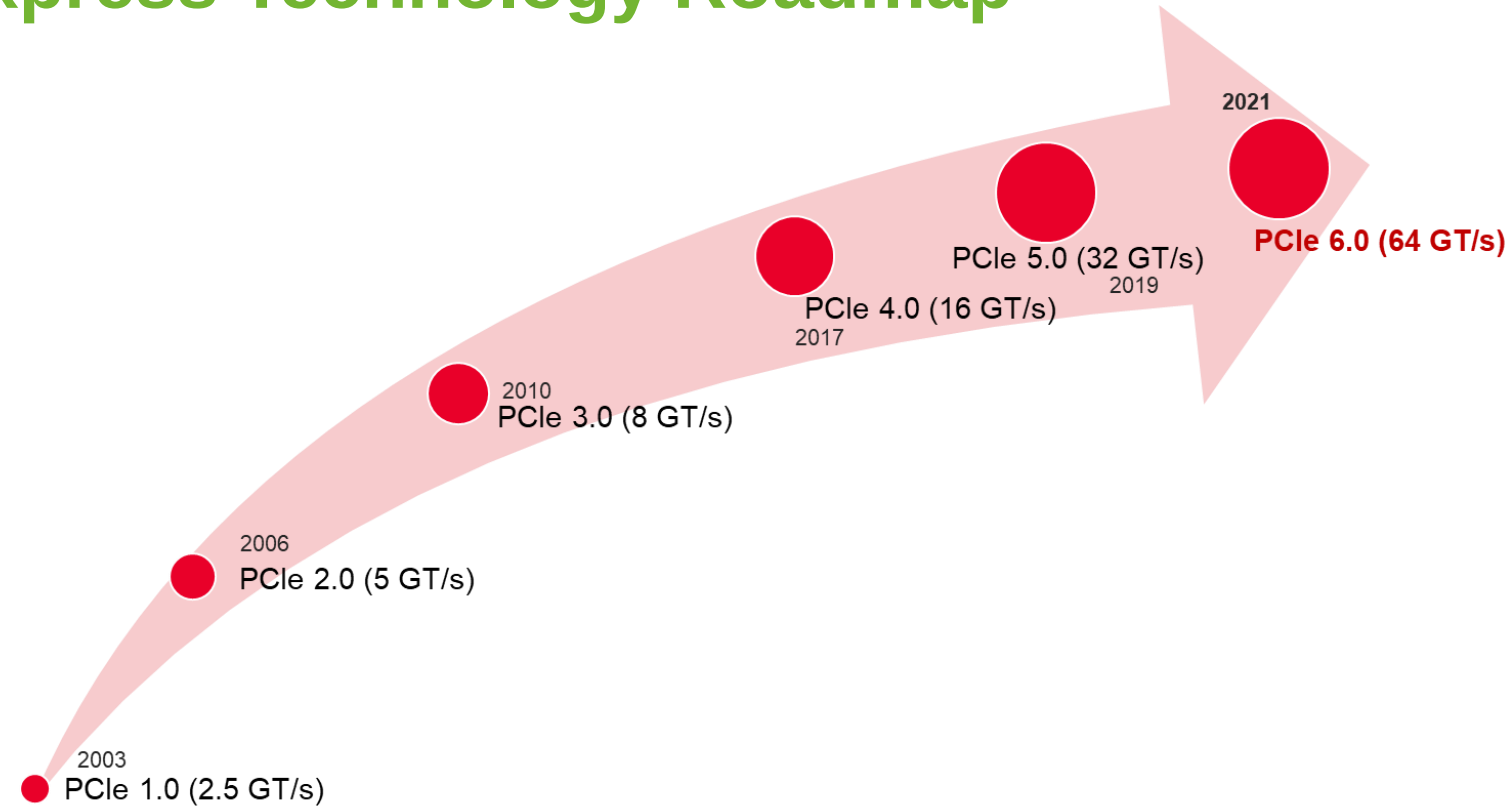
Component selection with single number

PCIe @ 32G and 64G Test Challenges

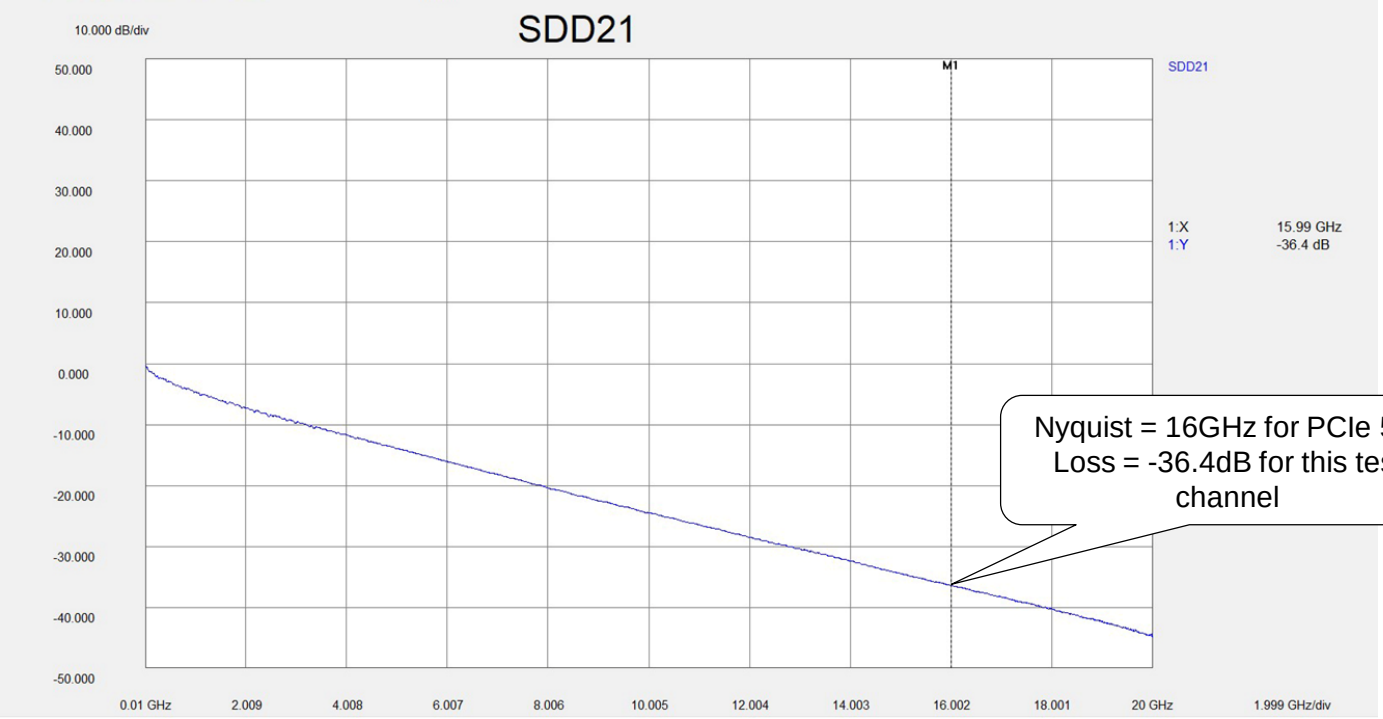
Rick Eads

Principal PCIe Program Manager, Keysight Technologies

PCI Express Technology Roadmap



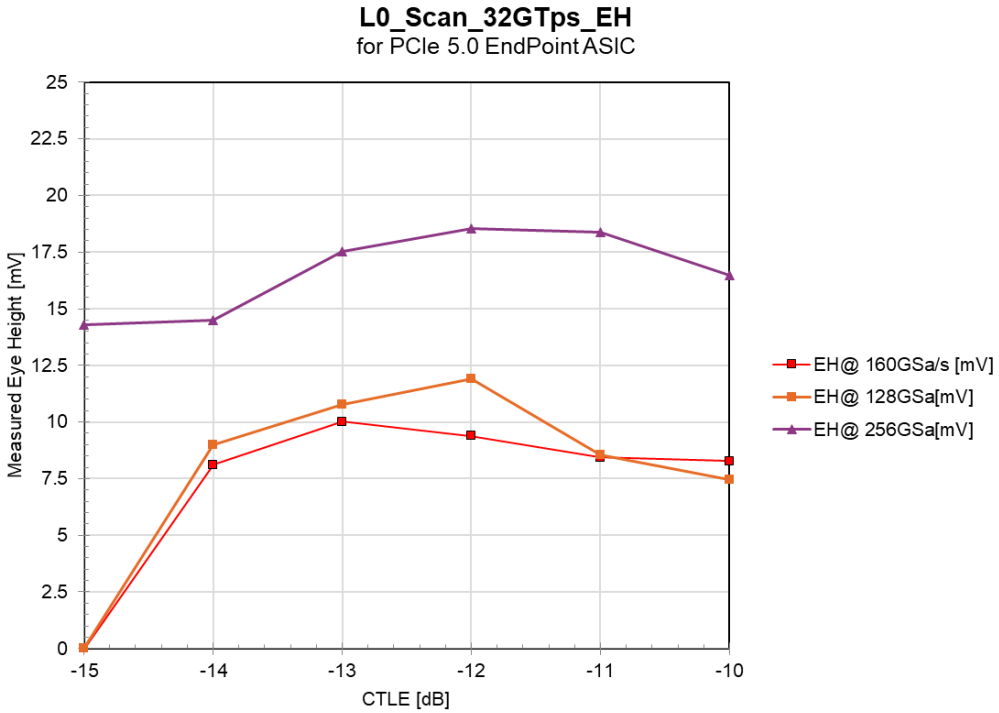
PCI Express 5.0 and 6.0 Channel Characteristics



Nyquist = 16GHz for PCIe 5/6
Loss = -36.4dB for this test channel

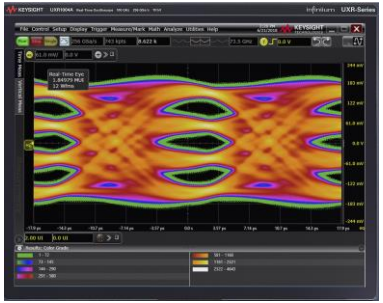
Instrument Noise Impact to Eye Height @32Gb/s NRZ

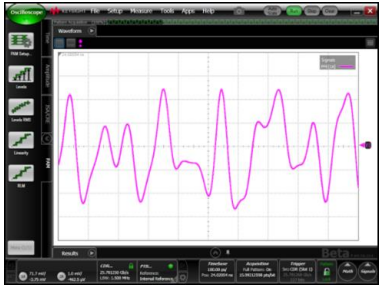
- **Data Rate = 32 Gb/s**
- **Composite Eye measured**
  - 2M UI
  - CTLE applied -10dB to -15dB
- **Channel -36dB @ 16GHz**
- **Generator**
  - TX preset P5
  - 800mV Launch
  - DMSI=10mV
  - CMSI=0mV
  - RJ-0.5ps
  - SJ=3.125ps@100MHz

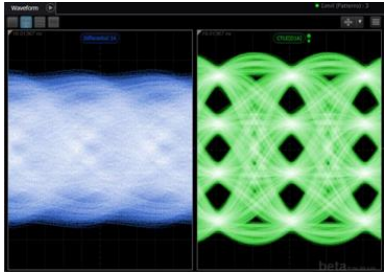


Clock Recovery for PAM4 Designs

- **Clock recovery (CR)**
  - Recovers a clock for the Rx to use in real systems
  - Standards require scopes to emulate most basic CR used in real Rx (track out low-frequency jitter, trigger the scope)
- **PAM4 adds complexity**
  - Transitions no longer only at 0V diff
  - CR Loop BW reduced from 10 MHz to ~ 4 MHz (IEEE 802.3bs/cd and CEI-56G-PAM4, same for proposed “112G” standards)
  - 1st Order PLL (no peaking, 20 dB/decade roll-off)
- **Instrument clock recovery**
  - Real-time oscilloscopes use software CR
  - Equivalent-time oscilloscopes (aka Sampling scopes) use hardware CR
  - CR needs to be able to lock onto “closed eyes”



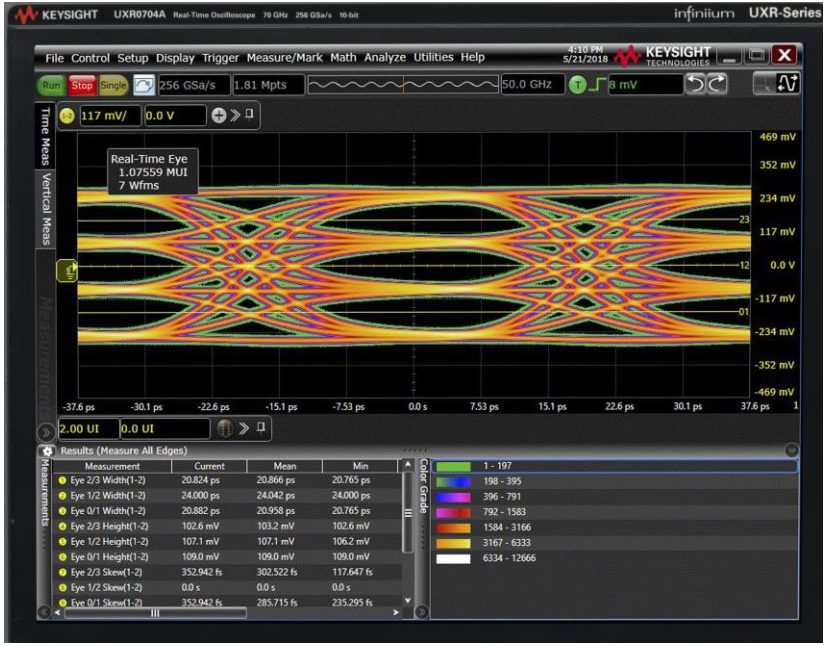




New TX and RX Measurements for PAM4

- **Multiple Eye Width & Eye Height Computations**
- **Eye Symmetry Mask Width (ESMW)**
- **Transmitter Linearity**
- **TX Output Jitter**
  - JRMS
  - J3u, J4u
  - Even-Odd Jitter (EOJ)

measured very differently compared to legacy NRZ signals



Measurement Challenges for PCIe 6.0

- What can be leveraged from test parameters and test methods developed for PAM-4 Signals established to-date by IEEE and OIF-CEI
- Choice of CDR model may be critical (higher PLL BW and Peaking could cause difficulty)
- Ensuring that measurements are performed at test points that have been equalized to achieve an open eye may be necessary
- SSC (Spread Spectrum Clocking) adds another layer of complexity
- FEC Performance and Native BER will be critical

Thank you!

QUESTIONS?

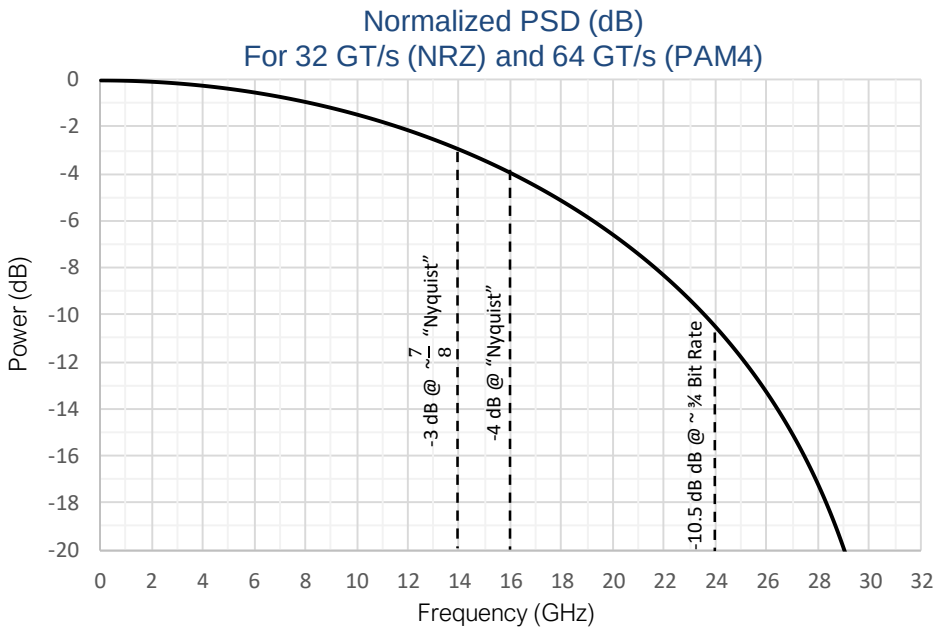
Back Up Slides to Support Q&A

References

- ***A method for calculating component level crosstalk contributions to Channel Crosstalk*, DesignCon2018, C.-P. Kao, B. Rothermel, J. Stephens**

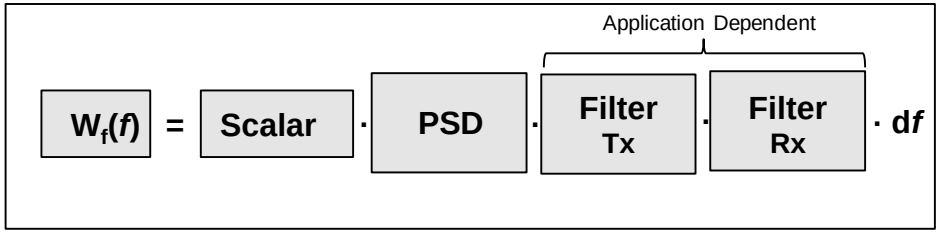
Power Spectral Density

- **Equation:**
  - $PSD = T_b \cdot \mathrm{sinc}^2(T_b \cdot f) = \frac{1}{f_b} \cdot \mathrm{sinc}^2(\frac{f}{f_b})$
- PSD is the fundamental weighting term in ICN.
- Essentially the same PSD for 32 GT/s NRZ and 64 GT/s PAM4 signaling.
- Taken alone, this suggests there is up to 4 dB more energy available for crosstalk at low frequencies than at the “Nyquist”
  - Counter to a constant, static, limit line that constrains all frequencies equally.
  - What happens when channel losses, limited Tx rise-times and Rx bandwidths, and/or channel equalization is considered.
    - *We will see.*



Integrated Crosstalk Noise, ICN

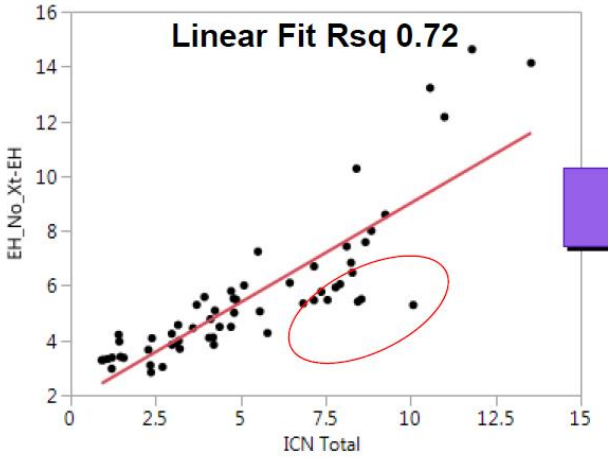
- **In ICN, a weighting function is used to weight the importance of the crosstalk magnitude at each frequency point.**
- **Terms in Weighting Function are based on powers**
  - *Scalar: A^2 ,where A = signal amplitude*
    - *In PCIe's based on pk-to-pk voltage*
      - $\left(\frac{A}{2}\right)^2 = \frac{1}{4}A^2$
  - *PSD: Power Spectral Density*
  - $TX\ Filter$: $|H(f_n)|^2 = \left[\frac{1}{1+(f_n/f_{nt})^4}\right]$, $f_{nt} = 0.2365/t_{rise}$
  - $Rx\ Filter$: $|H(f_n)|^2 = \left[\frac{1}{1+(f_n/f_r)^8}\right]$, f_r = ¾(data rate)
- $W(f) = \left(\frac{A^2}{4}\right) \cdot \left[\frac{1}{f_b} \cdot \mathrm{sinc}^2\left(\frac{f}{f_b}\right)\right] \cdot \left[\frac{1}{1+(f_n/f_{nt})^4}\right] \cdot \left[\frac{1}{1+(f_n/f_r)^8}\right] \cdot df$



Block Diagram of ICN $W_f(f)$

ICN Correlation to Eye Height

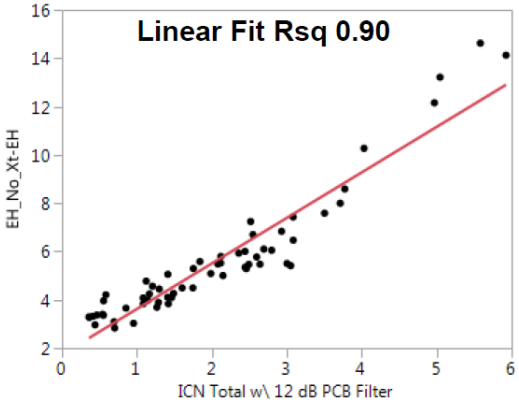
- **Trend demonstrates that Eye Closure Increases as ccICN increases**
  - Would including a channel loss term in ICN provide better correlation



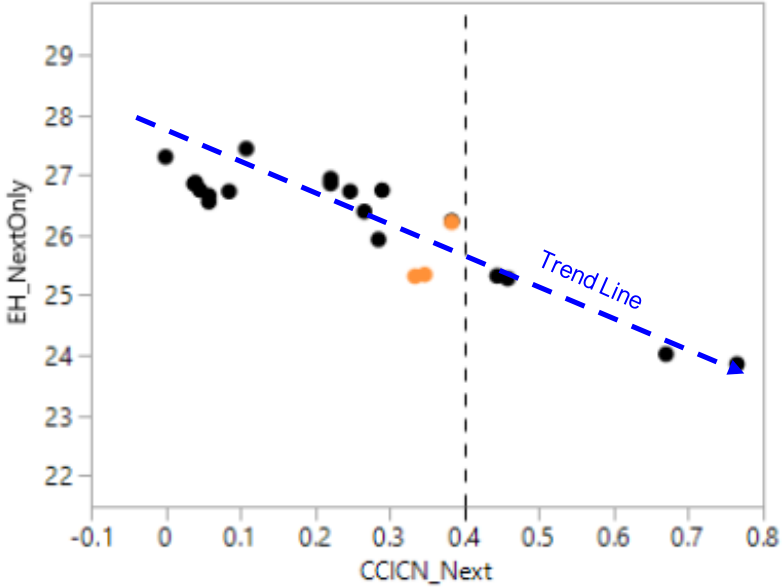
Eye Closure vs. ccICN

ccICN Correlation to Eye Height

- **Improved correlation to Eye Height**
  - ~ -4 mV / 0.8 mV, slope of 5:1



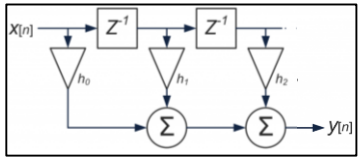
Eye Closure vs. ccICN



Eye Height vs. ccICN

Equalizer Filter, Tx 3-Tap FFE

- **Background**
  - Based on PCIe Specification
    - *However, if needed more taps can be added*
  - Converted from digital domain to frequency domain
    - $H(z) = \sum_{k=0}^{n\,taps} h_k z^{-k}, where\ h_k\ are\ the\ tap\ values$
    - $H(e^{j\omega}) = \sum_{k=0}^{n\,taps} h_k e^{-j\omega k}\ , i.e.\ H(e^{j\omega}) = -0.1 + 0.7e^{-j\omega} - 0.2e^{-j2\omega}\ , for\ preset\ P7$
    - Where $e^{j\omega t} = \cos(\omega) + j\sin(\omega), Euler's\ formula$



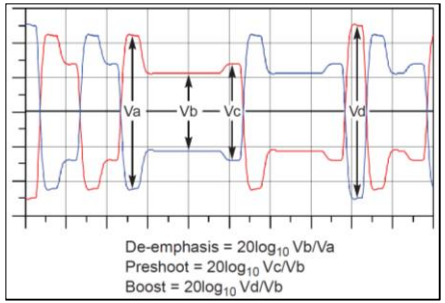
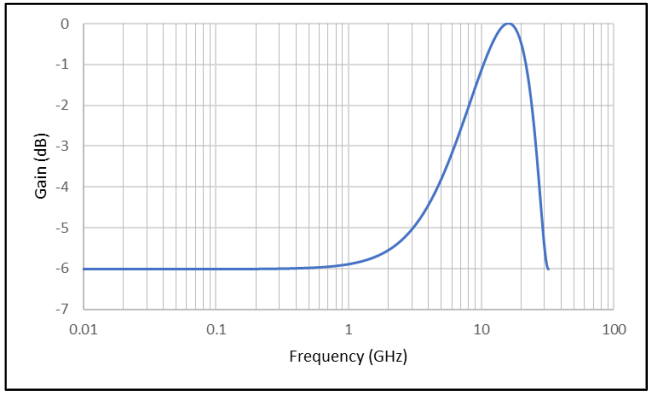


Table 8-1 Tx Preset Ratios and Corresponding Coefficient Values

Preset #	Preshoot (dB)	De-emphasis (dB)	C-1	C+1	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	Note 2.	0.000	Note 2.	1.000	Note 2.	Note 2.



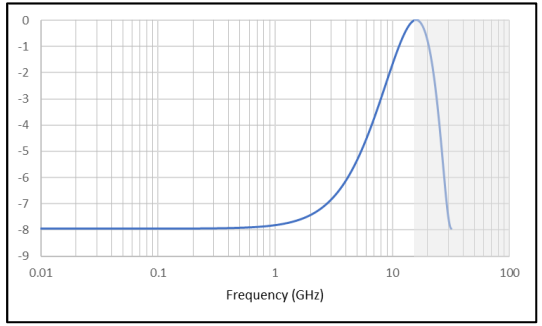
Tx 3-Tap DFE in dB (P0)

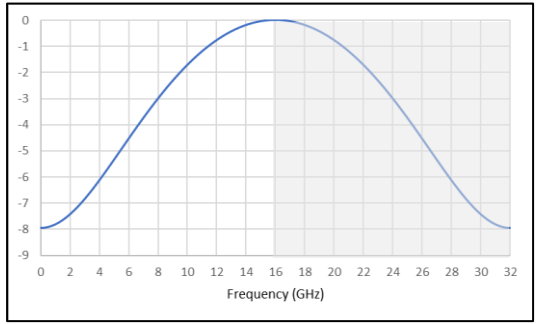
Equalizer Filter, Tx 3-Tap FFE

Addition Information

- Provided for reference only, gain (dB) based on P7
- Equation

$$Tx\ FFE:\ |H(f_n)|^2 = |h_0 + \sum_{k=1}^{\#\,taps-1} h_k(\cos\left(k \cdot 2\pi \frac{f_n}{f_b}\right) + jsin\left(k \cdot 2\pi \frac{f_n}{f_b}\right))\,|^2$$





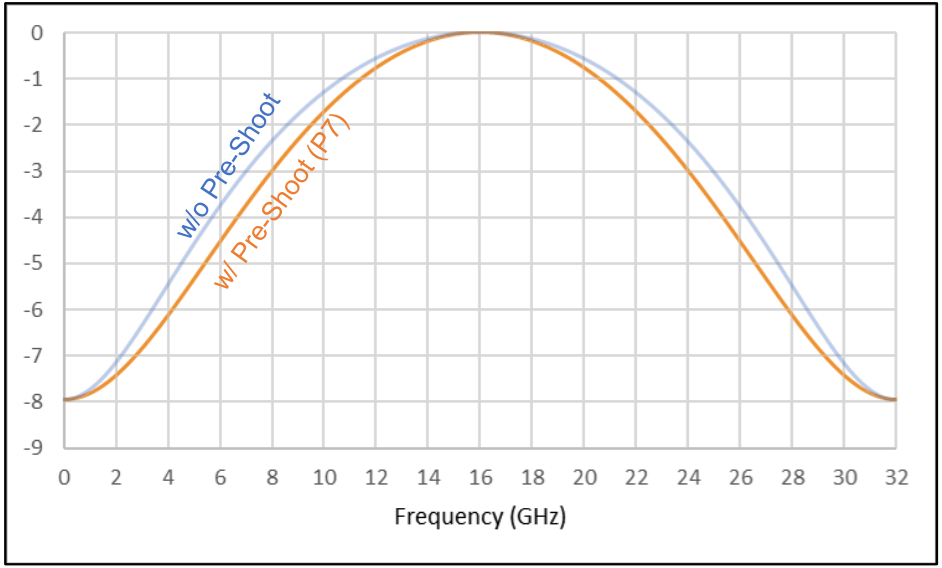
32 GT/s, Log and Linear x-axes

Equalizer Filter, Tx 3-Tap FFE

Addition Information

- Affect of pre-shoot on normalized power spectrum (dB)

w/ Pre-shoot (p7)		
De-emphasis		6.0 dB
Pre-shoot		3.5 dB
Boost		8.0 dB
w/o Pre-shoot		
De-emphasis	8.0 dB	
Pre-shoot	0.0 dB	
Boost	8.0 dB	



Comparing w & w/o Pre-Shoot Same Boost

Equalizer Filter, Rx CTLE

Background

- Based on PCIe Specification
  - Provides formula in *s* domain, converted to *f* domain
  - *Reference steps from -5.0 to -15.0 dB, 1.0 dB increments*
  - Formulas and graphs provided for reference and comparison

$$|H(f)|^2 = 10^{\frac{G_{DC\,dB}}{10}} \cdot \left[\frac{\left(1+\left(\frac{f_n}{f_{z1}}\right)^2\right)\cdot\left(1+\left(\frac{f_n}{f_{z2}}\right)^2\right)}{\left(1+\left(\frac{f_n}{f_{p1}}\right)^2\right)\cdot\left(1+\left(\frac{f_n}{f_{p2}}\right)^2\right)\cdot\left(1+\left(\frac{f_n}{f_{p3}}\right)^2\right)\cdot\left(1+\left(\frac{f_n}{f_{p4}}\right)^2\right)} \right]$$

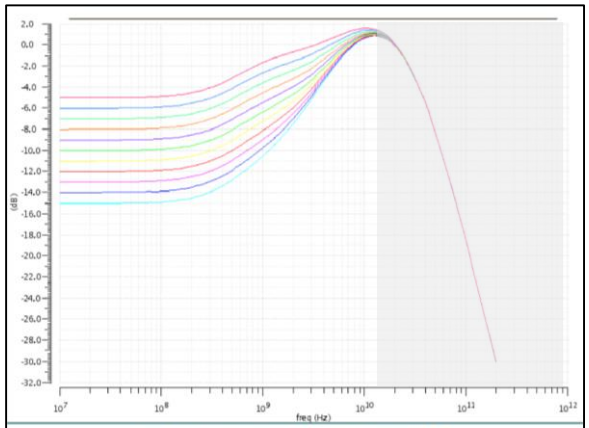


Figure 8-33 Loss Curves for 32.0 GT/s Behavioral CTLE

$$H(s) = \frac{\omega_{P1} \times \omega_{P3} \times \omega_{P4}}{\omega_{Z1}} \times \frac{(s+\omega_{Z1})(s+\omega_{P2} \times A_{DC})}{(s+\omega_{P1})(s+\omega_{P2})(s+\omega_{P3})(s+\omega_{P4})}$$

$\omega_x = 2\pi \times F_x$

$F_{P1} = 1.65 \times F_{Z1}$

$F_{P2} = 9.5$ GHz

$F_{P3} = 28$ GHz

$F_{P4} = 28$ GHz

$F_{Z1} = 450$ MHz

$F_{Z2} = \text{mag(DC gain)} \times F_{P2}$

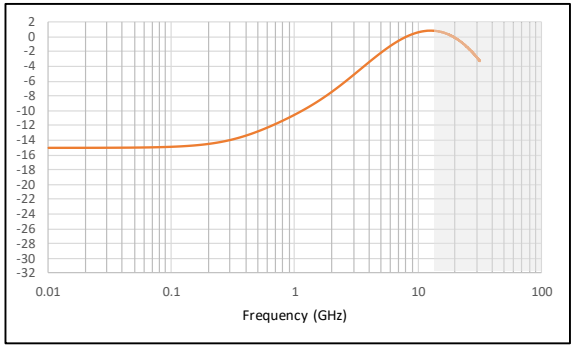
Equation 8-7 Behavioral CTLE at 32.0 GT/s

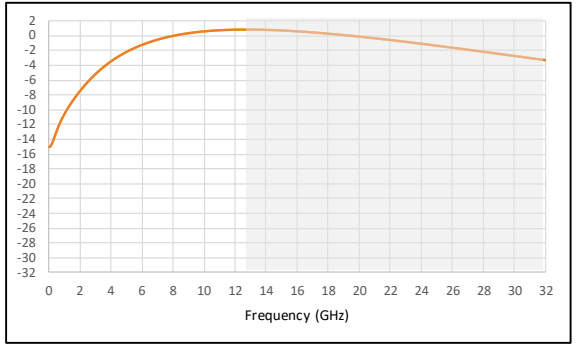
PCIe Gen 5 Base Specification Formula

Equalizer Filter, Rx CTLE

Additional Information

- Provided for reference only
- Rx CTLE equalization bandwidth to 11 GHz





32 GT/s NRZ , Log and Linear Y-Axis2

Comparison EQ Weighting Functions

- **Comparison and observation**
  - Un-equalized vs. Equalized
    - *Un-equalized curves over-weight lower frequencies, << 16GHz*
    - *Un-equalized curves over-weight higher frequencies, >> 16 GHz*